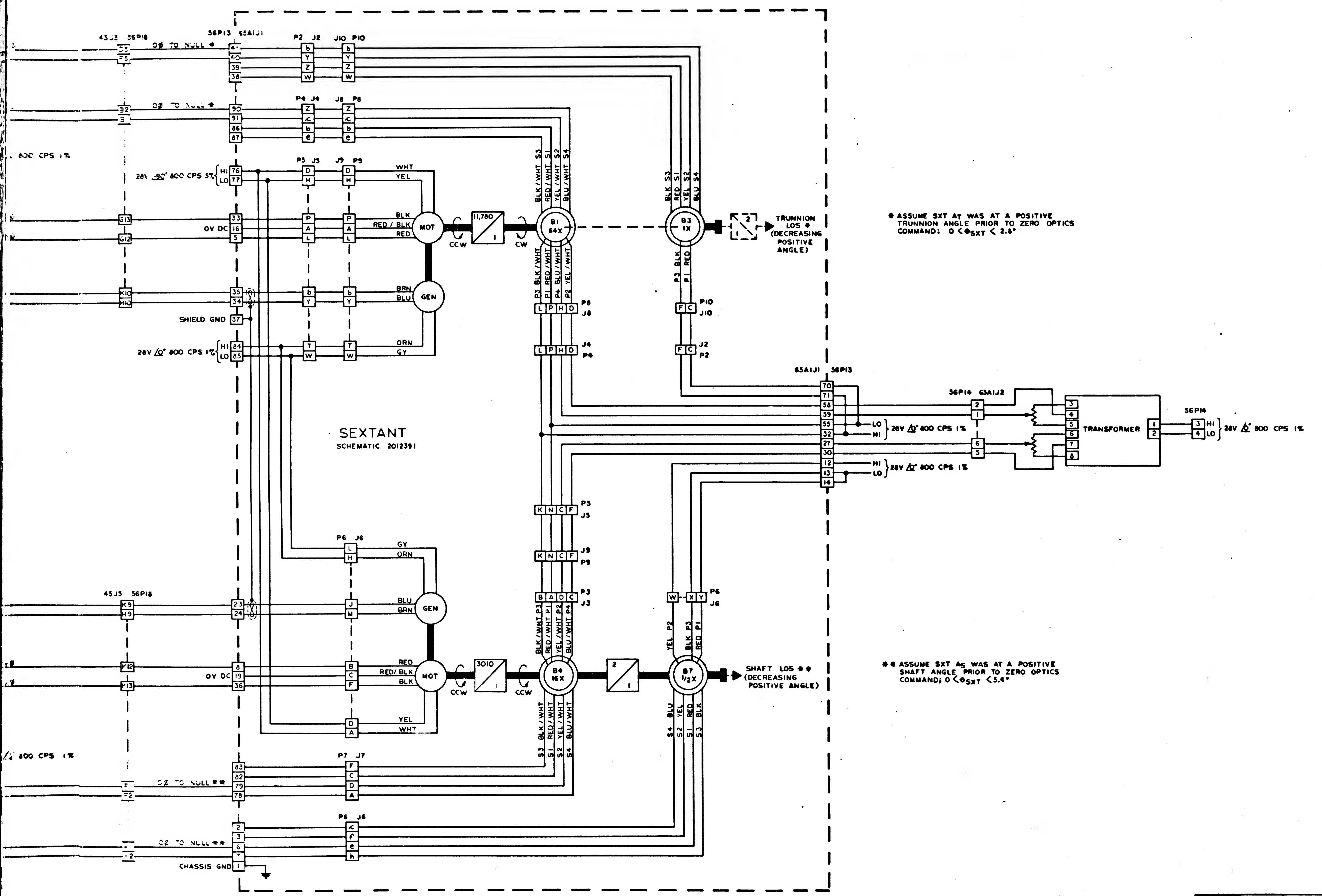


* ASSUME SXT A_T WAS AT A POSITIVE TRUNNION ANGLE PRIOR TO ZERO OPTICS COMMAND: $0 < \theta_{SXT} < 2.8°$

** ASSUME SXT A_S WAS AT A POSITIVE SHAFT ANGLE PRIOR TO ZERO OPTICS COMMAND; $0 < \theta_{SXT} < 5.6°$

REVISIONS

SYM	ZONE	DESCRIPTION	DR	CHK	DATE	APPROVED

NEXT ASSY | USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
CAPACITOR VALUES ARE IN μf
RESISTOR VALUES ARE IN OHMS
TOLERANCES ON
FRACTIONS ± — DECIMALS ± — ANGLES ± —
DO NOT SCALE THIS DRAWING

MATERIAL —

MIT
INSTRUMENTATION LAB
CAMBRIDGE MASS

DRAWN Wandawhid 1-17-66
CHECKED
APPROVED E. A. Young 1-20-66
APPROVED 1-29-66
APPROVED MIT W G Murley 1-25-66
A. G. Mc FADDEN
APPROVED MSC
DATE

MANNED SPACECRAFT CENTER
HOUSTON, TEXAS

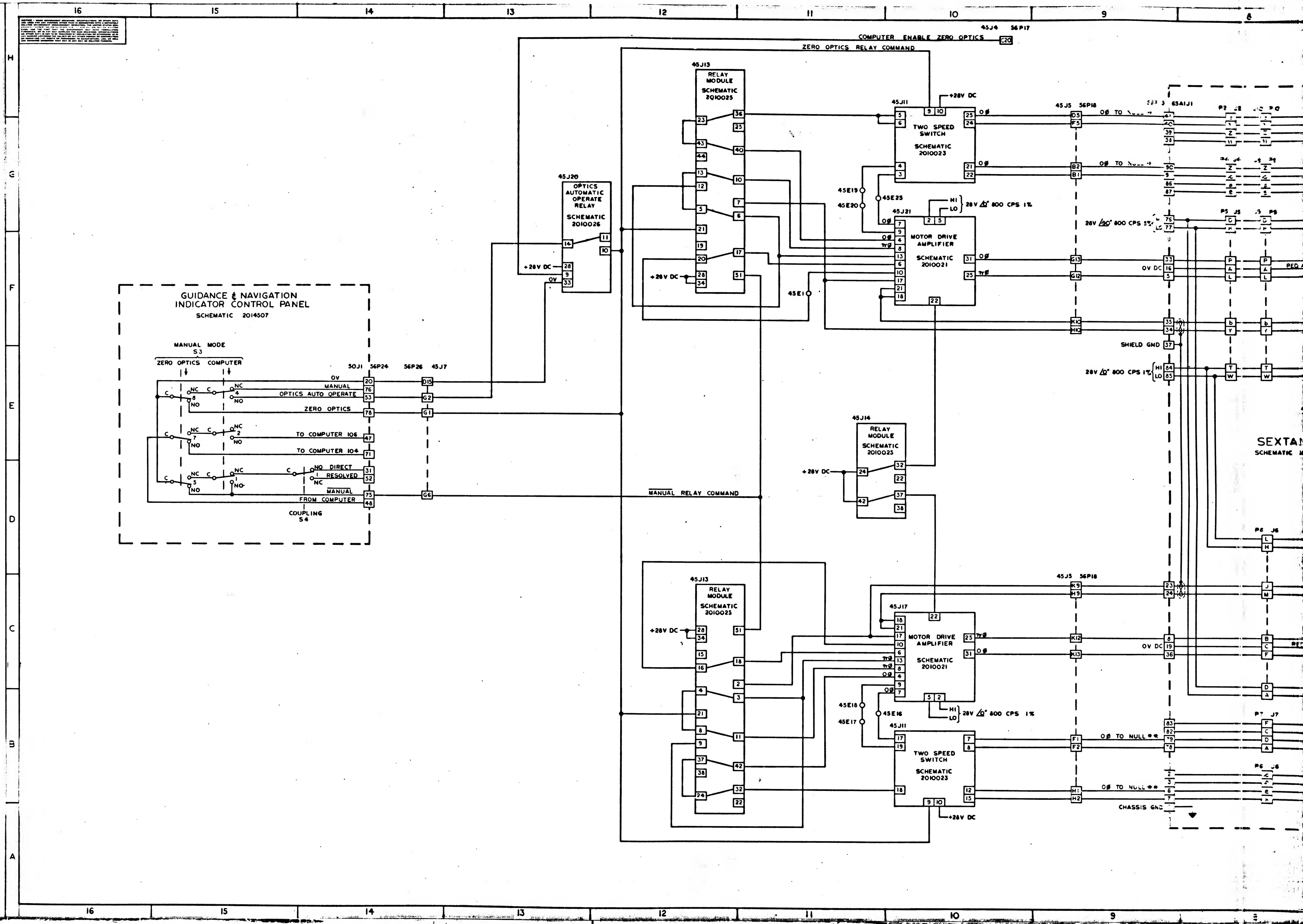
ZERO OPTICS MODE
BLOCK II

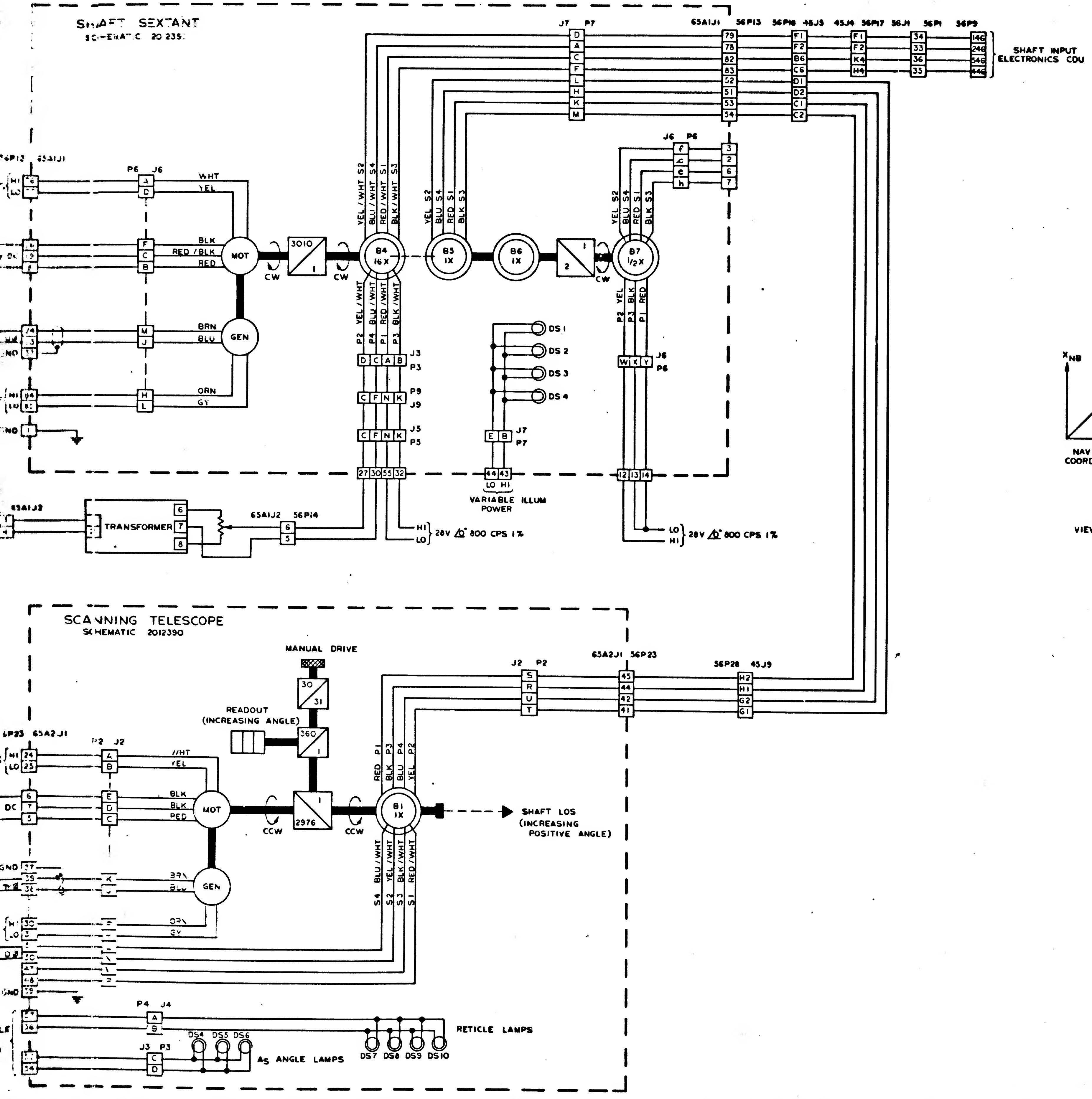
CODE IDENT NO. | SIZE J | DRAWING NO. 2015502

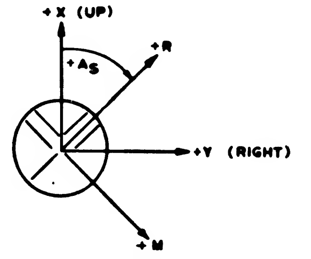
SCALE — | SHEET 1 OF 1

MASTER

2015502

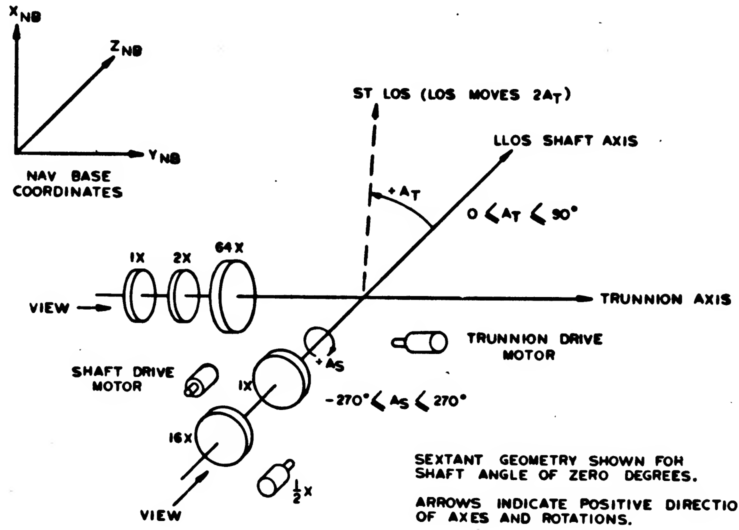

GUIDANCE & NAVIGATION INDICATOR CONTROL PANEL
SCHEMATIC 2014507
MANUAL MODE S3
ZERO OPTICS
COMPUTER
COUPLING S4
OV
MANUAL
OPTICS AUTO OPERATE
ZERO OPTICS
TO COMPUTER 106
TO COMPUTER 104
DIRECT
RESOLVED
MANUAL
FROM COMPUTER
50J1
56P24
56P26
45J7
45J20
OPTICS AUTOMATIC OPERATE RELAY
SCHEMATIC 2010026
+28V DC
45J13
RELAY MODULE
SCHEMATIC 2010025
45J14
RELAY MODULE
SCHEMATIC 2010025
45J11
TWO SPEED SWITCH
SCHEMATIC 2010023
45J21
MOTOR DRIVE AMPLIFIER
SCHEMATIC 2010021
45J17
MOTOR DRIVE AMPLIFIER
SCHEMATIC 2010021
45E19
45E20
45E25
45E1
45E18
45E17
45E16
28V ∠0° 800 CPS 1%
HI
LO
45J4
56P17
COMPUTER ENABLE ZERO OPTICS
ZERO OPTICS RELAY COMMAND
MANUAL RELAY COMMAND
45J5
56P18
0Ø TO NULL
0Ø TO NULL **
65A1J1
28V ∠90° 800 CPS 5%
0V DC
SHIELD GND
CHASSIS GND
SEXTAN
SCHEMATIC
16
15
14
13
12
11
10
9
8
H
G
F
E
D
C
B
A





DIRECTION OF IMAGE MOTION AS VIEWED THRU SEXTANT EYEPIECE

CONTROLLER MOTION	SEXTANT SHAFT ANGLE	DIRECT MODE APPARENT IMAGE MOTION
RIGHT	INCREASE	- M
LEFT	DECREASE	+ M



SEXTANT GEOMETRY SHOWN FOR SHAFT ANGLE OF ZERO DEGREES.

ARROWS INDICATE POSITIVE DIRECTIONS OF AXES AND ROTATIONS.

ROTATING COMPONENTS

SXT SHAFT FOR INCREASING SHAFT ANGLE IN A POSITIVE DIRECTION

1. MOTOR TACH ROTATES CW WHEN LOOKING AT THE SHAFT END.
2. 1/2 X RESOLVER ROTATES CW WHEN LOOKING AT SHAFT END.
3. 16X & 1X RESOLVERS ROTATE CW WHEN LOOKING IN DIRECTION OF ARROW.

MASTER

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
CAPACITOR VALUES ARE IN µf
RESISTOR VALUES ARE IN OHMS
TOLERANCES ON
FRACTIONS ± — DECIMALS ± — ANGLES ± —
DO NOT SCALE THIS DRAWING
MATERIAL —

MIT
INSTRUMENTATION LAB
CAMBRIDGE, MASS

DRAWN [illegible] 1-13-66
CHECKED
APPROVED E. B. Young 1-24-66
APPROVED [illegible] 1-24-66
APPROVED MIT [illegible] 1-25-66
APPROVED MSC A. C. METZGER
DATE

MANNED SPACECRAFT CENTER
HOUSTON, TEXAS

SHAFT MANUAL MODE BLOCK II

CODE IDENT NO.
SIZE J
DRAWING NO. 2015503
SCALE —
SHEET 1 OF 1

REVISIONS
SYM ZONE DESCRIPTION DR CHK DATE APPROVED

2015503

3H

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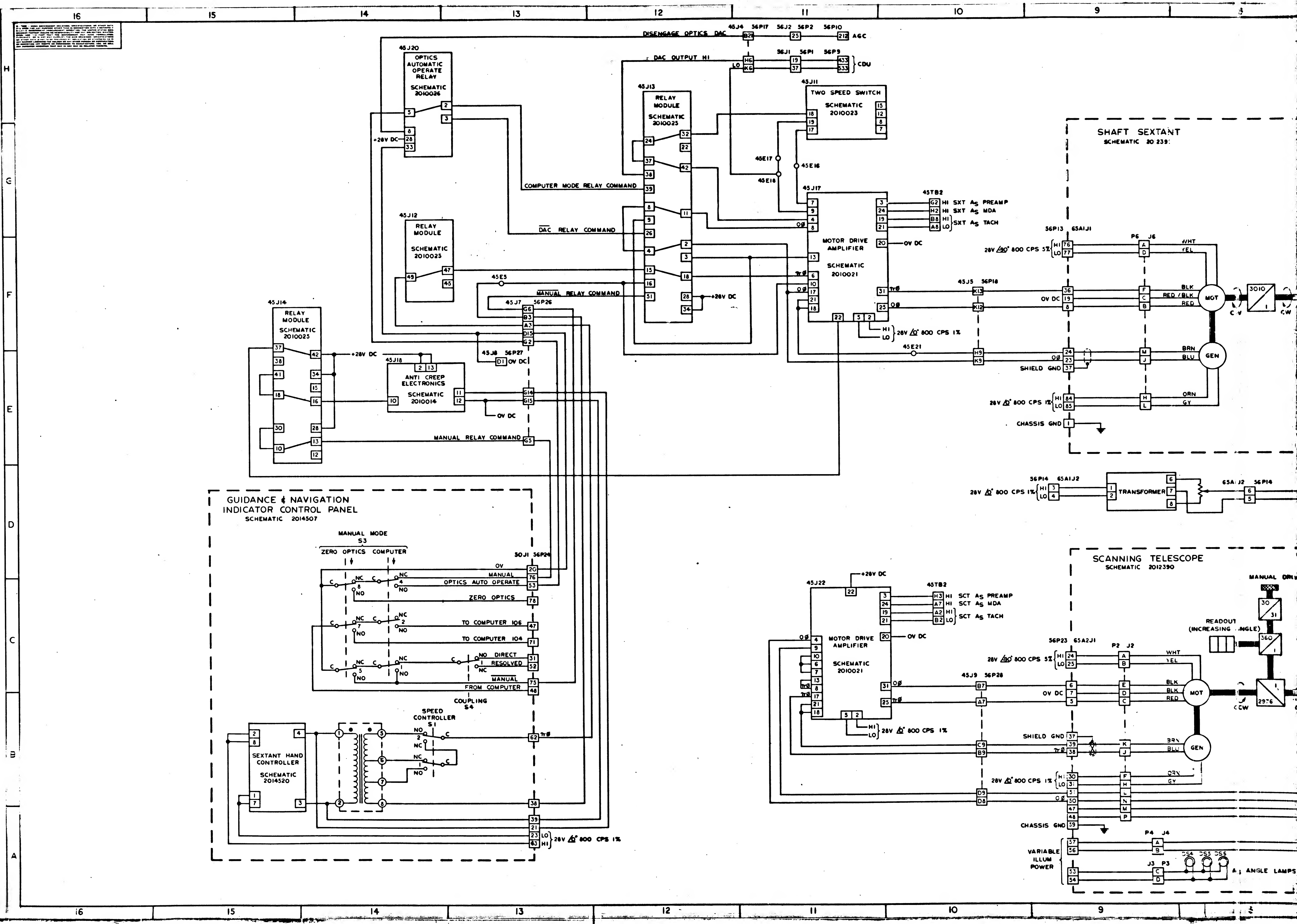
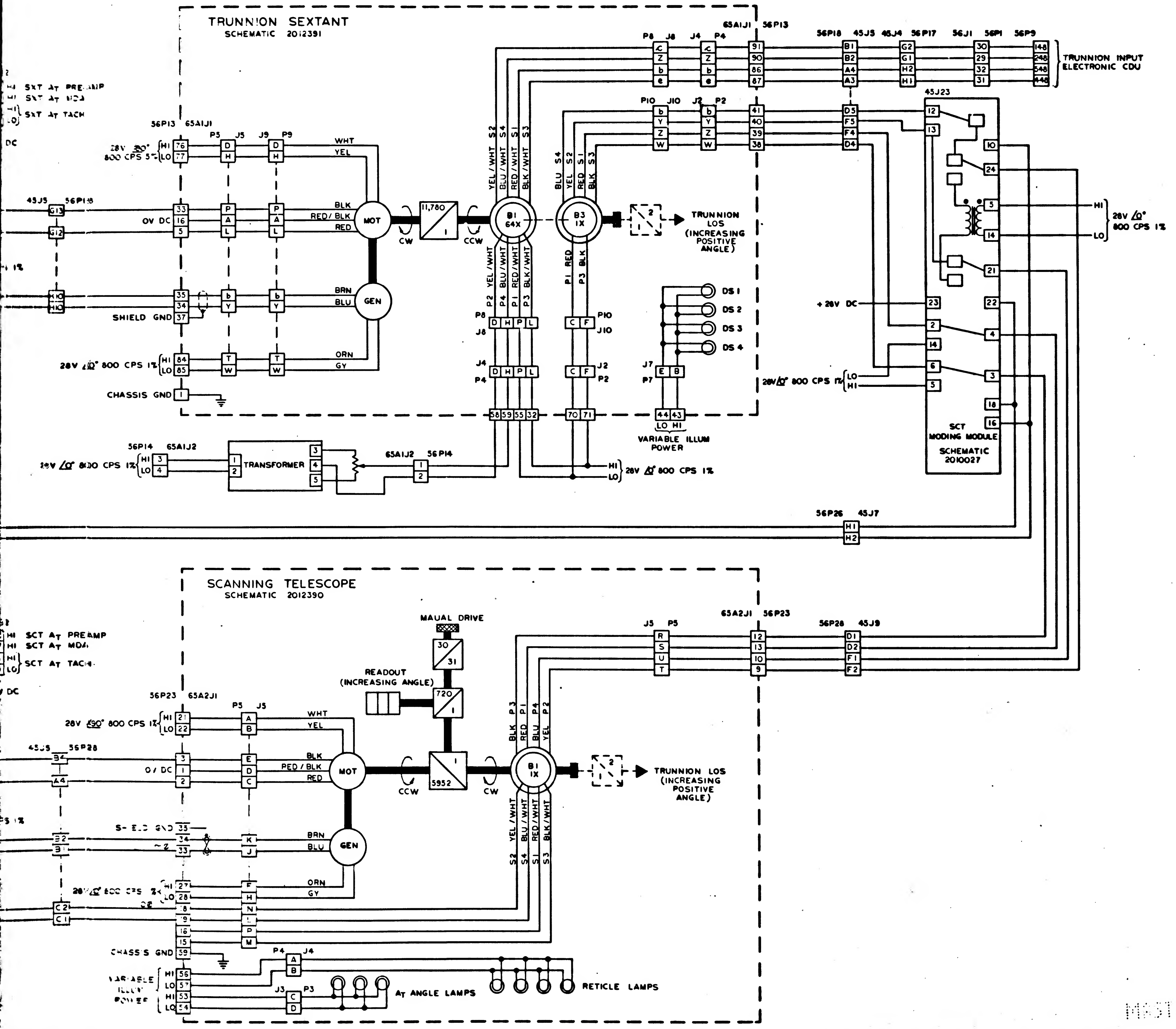
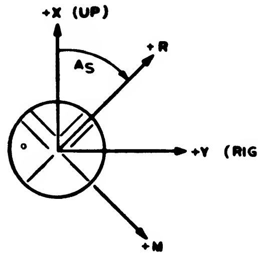
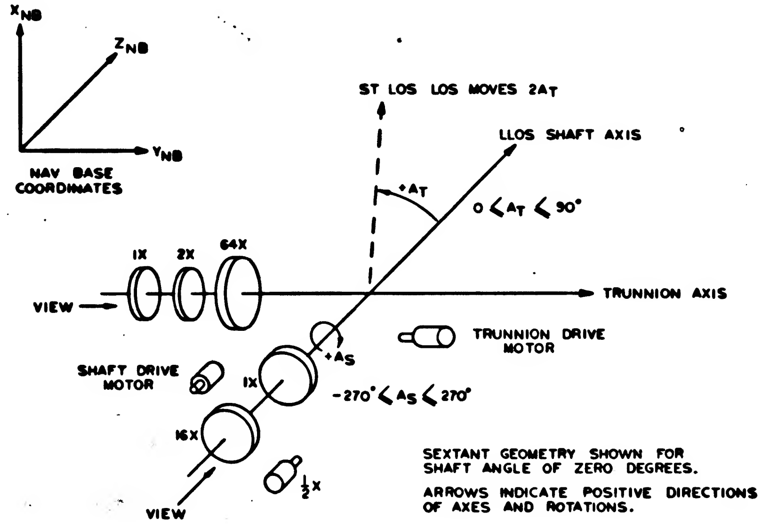






DIRECTION OF IMAGE MOTION AS VIEWED THRU SEXTANT EYEPIECE

CONTROLLER MOTION	SEXTANT TRUNNION ANGLE	DIRECT MODE APPARENT IMAGE MOTION
UP	INCREASE	-R
DOWN	DECREASE	+R



SEXTANT GEOMETRY SHOWN FOR SHAFT ANGLE OF ZERO DEGREES.

ARROWS INDICATE POSITIVE DIRECTIONS OF AXES AND ROTATIONS.

ROTATING COMPONENTS

SXT TRUNNION FOR INCREASING TRUNNION ANGLE IN A POSITIVE DIRECTION.

1. MOTOR TACH ROTATES CW WHEN LOOKING AT THE SHAFT END.
2. 64X, 2X, & 1X RESOLVER ROTORS ROTATE CW WHEN LOOKING IN DIRECTION OF ARROW.

MASTER

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
CAPACITOR VALUES ARE IN µf
RESISTOR VALUES ARE IN OHMS
TOLERANCES ON
FRACTIONS ± — DECIMALS ± — ANGLES ± —
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MATERIAL —

NEXT ASSY | USED ON
APPLICATION

MIT
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CAMBRIDGE, MASS

DRAWN Wunderlich 10-20-66
CHECKED
APPROVED E R Young 1-24-66
APPROVED AA Kosso 1-24-66
APPROVED MIT McMurdy 1-25-66
A. C. METZGER
APPROVED MSC
DATE

MANNED SPACECRAFT CENTER
HOUSTON, TEXAS

TRUNNION MANUAL MODE BLOCK II

CODE IDENT NO. 80230
SIZE
DRAWING NO. 2015504
SCALE —
SHEET 1 OF 1

2015504

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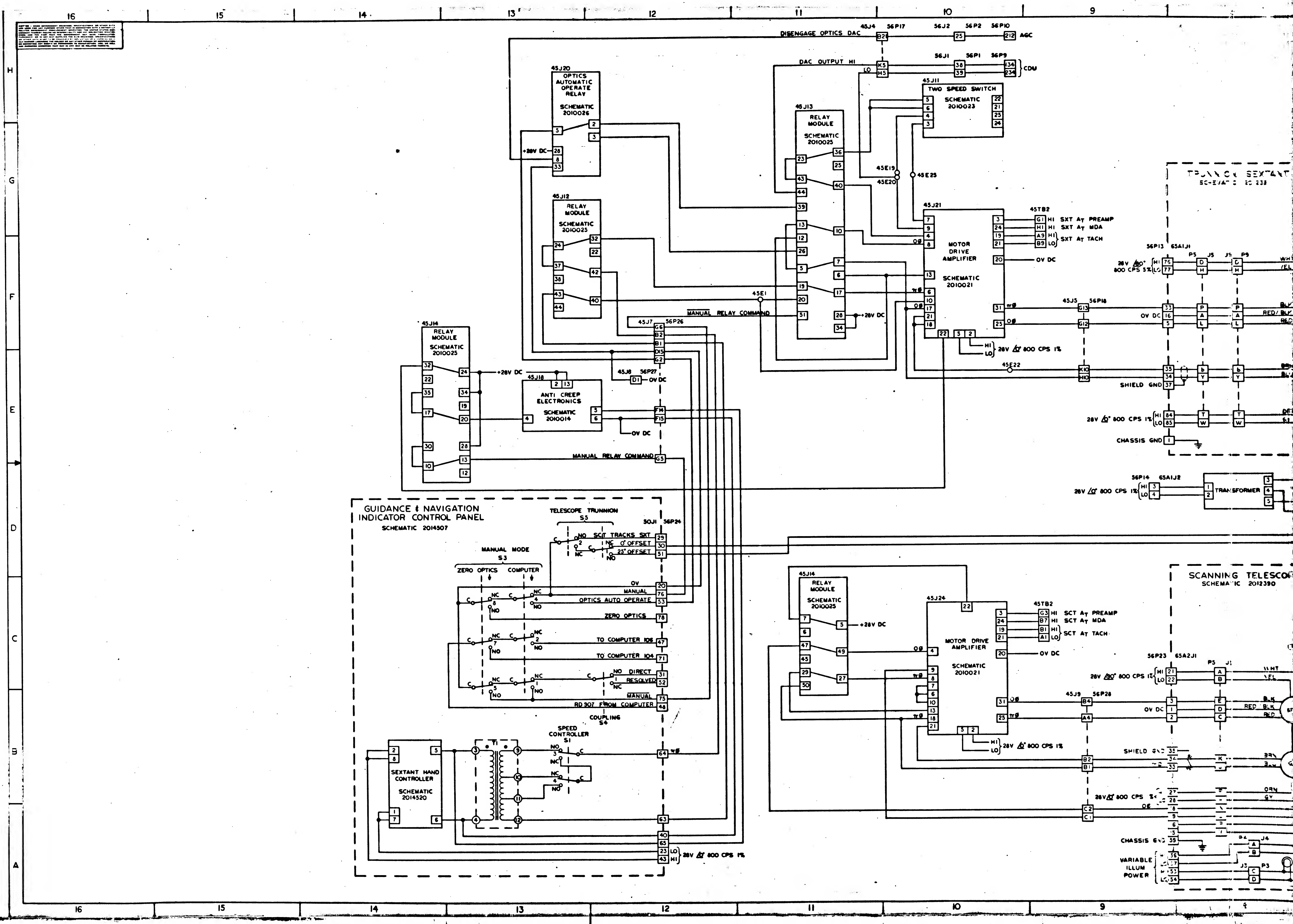
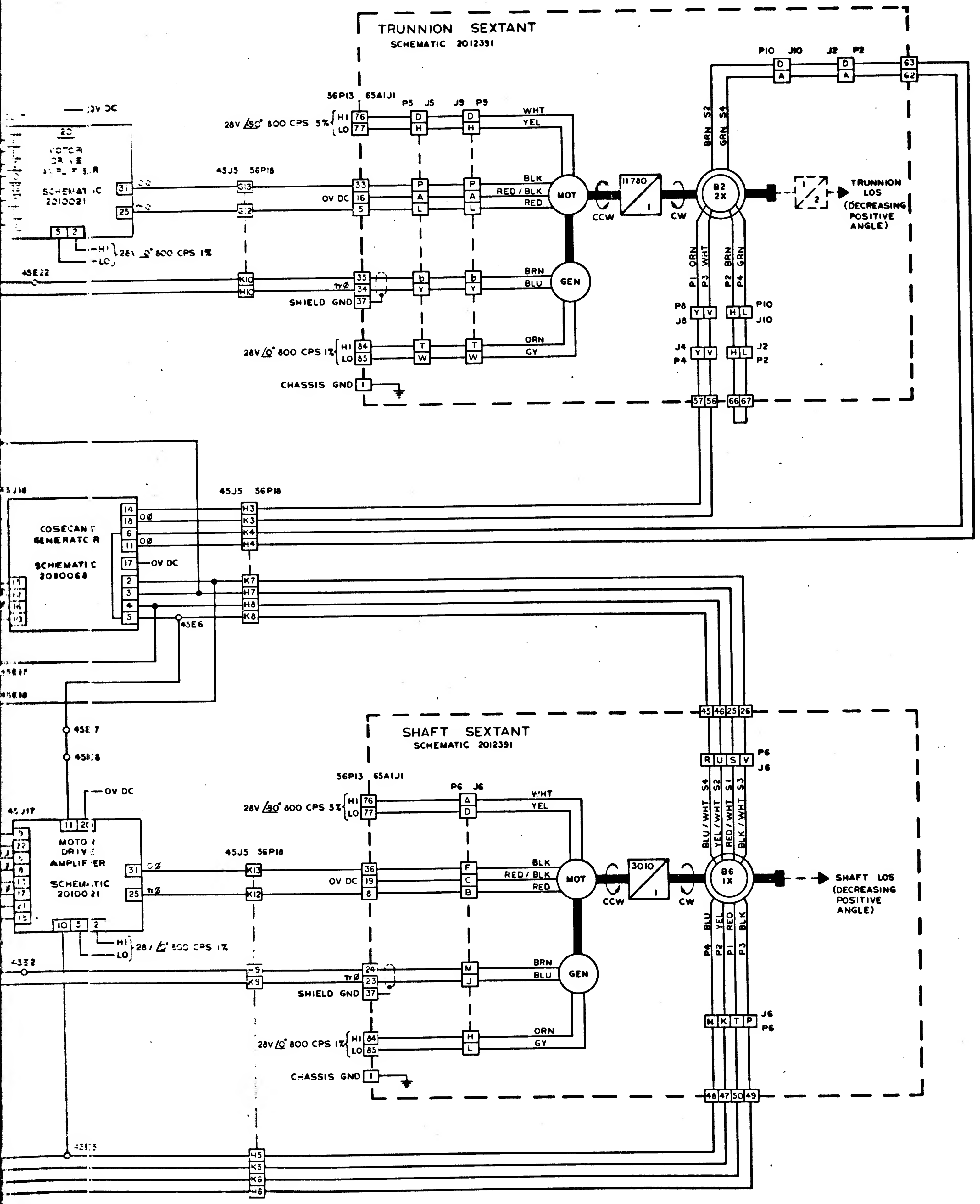
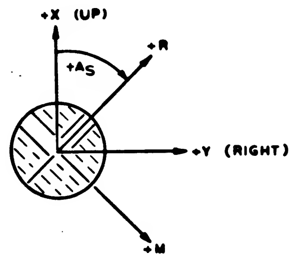
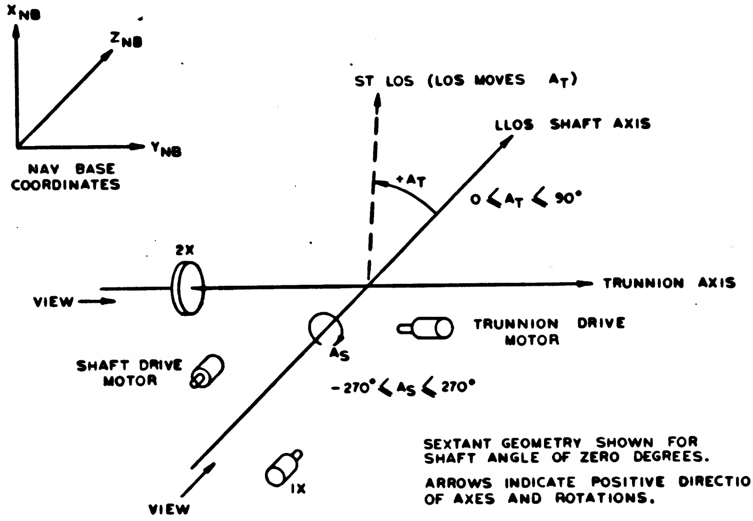






DIRECTION OF IMAGE MOTION AS VIEWED THRU SEXTANT EYEPIECE

CONTROLLER MOTION	SEXTANT TRUNNION ANGLE	SEXTANT SHAFT ANGLE	RESOLVED MODE APPARENT IMAGE MOTION
UP	DECREASE		+ X
DOWN	INCREASE		- X
RIGHT		DECREASE	+ Y
LEFT		INCREASE	- Y



SEXTANT GEOMETRY SHOWN FOR SHAFT ANGLE OF ZERO DEGREES.

ARROWS INDICATE POSITIVE DIRECTIONS OF AXES AND ROTATIONS.

ROTATING COMPONENTS
SXT TRUNNION FOR INCREASING TRUNNION ANGLE IN A POSITIVE DIRECTION
1. MOTOR TACH ROTATES CW WHEN LOOKING AT THE SHAFT END.
2. 2X RESOLVER ROTOR ROTATES CW WHEN LOOKING IN DIRECTION OF ARROW.

SXT SHAFT FOR INCREASING SHAFT ANGLE IN A POSITIVE ANGLE
1. MOTOR TACH ROTATES CW WHEN LOOKING AT THE SHAFT END.
2. 1X RESOLVER ROTATES CCW WHEN LOOKING AT THE SHAFT END.

REVISIONS						
SYM	ZONE	DESCRIPTION	DR	CHK	DATE	APPROVED

3H

MASTER

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
CAPACITOR VALUES ARE IN µf
RESISTOR VALUES ARE IN OHMS
TOLERANCES ON
FRACTIONS DECIMALS ANGLES
± — ± — ± —
DO NOT SCALE THIS DRAWING
MATERIAL —

NEXT ASSY | USED ON
APPLICATION

MIT
INSTRUMENTATION LAB
CAMBRIDGE, MASS.

DRAWN 1-19-66
CHECKED
APPROVED L. R. Young 1-24-66
APPROVED 1-24-66
APPROVED MIT 4-25-66
A. C. METZGER
APPROVED MSC
DATE

MANNED SPACECRAFT CENTER
HOUSTON, TEXAS

SEXTANT OPTICS RESOLVED MODE BLOCK II

CODE IDENT NO. | SIZE J | DRAWING NO. 2015505
SCALE — | SHEET 7 OF 7

J 2015505

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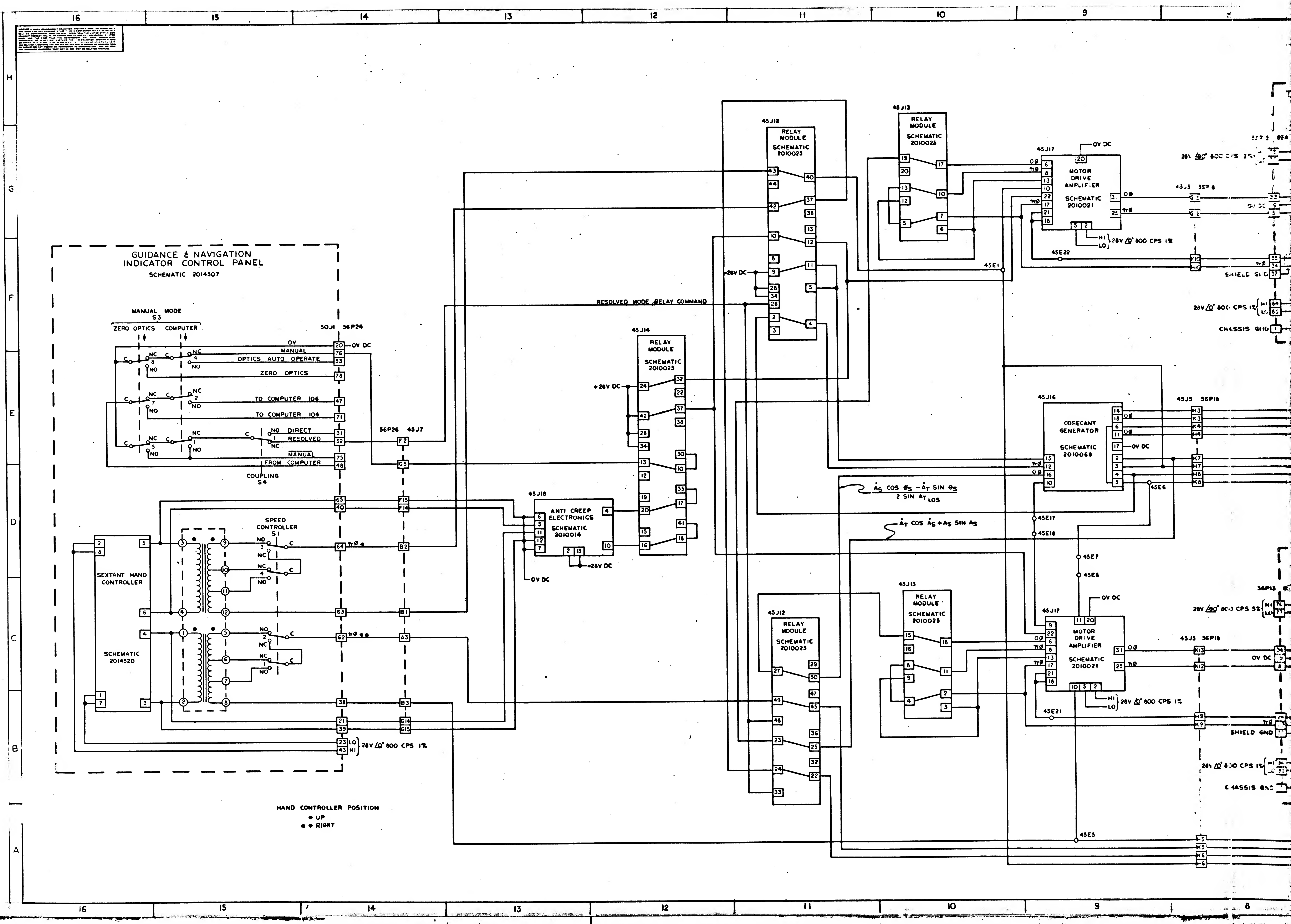
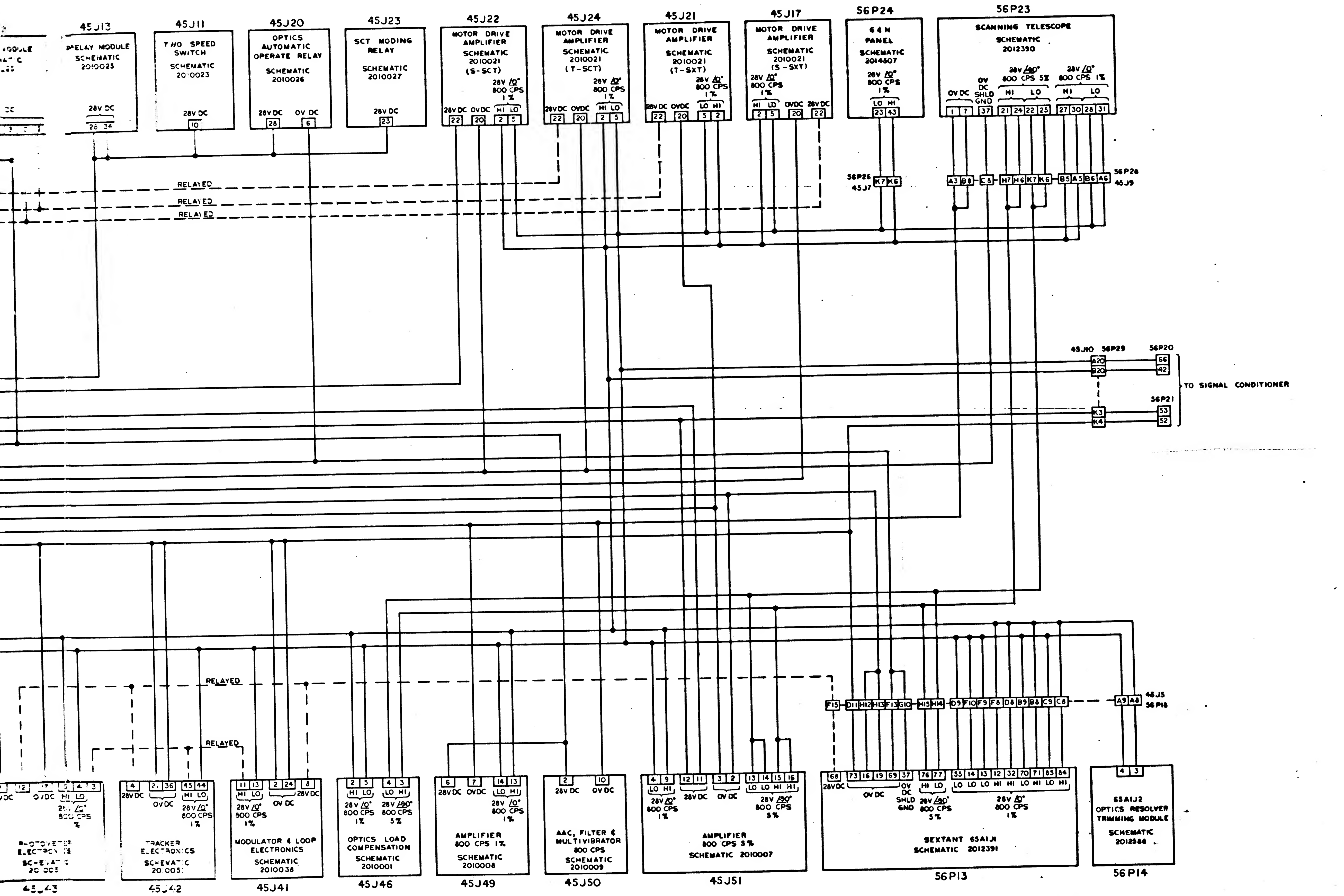


$\dfrac{\dot{A}_S \cos \emptyset_S - \dot{A}_T \sin \theta_S}{2 \sin A_{T\,LOS}}$

$\dot{A}_T \cos \dot{A}_S + A_S \sin A_S$



2H

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
CAPACITOR VALUES ARE IN µf
RESISTOR VALUES ARE IN OHMS
TOLERANCES ON
FRACTIONS DECIMALS ANGLES
± — ± — ± —
DO NOT SCALE THIS DRAWING

MATERIAL
—

MIT
INSTRUMENTATION LAB
CAMBRIDGE MASS

DRAWN Kondratick 1-31-66
CHECKED
APPROVED L. R. Young 1-31-66
APPROVED D. A. Koso 2-1-66
APPROVED MIT W. Kupfer 1 Feb 66
A. C. [illegible]
APPROVED MSC
DATE

MANNED SPACECRAFT CENTER
HOUSTON, TEXAS

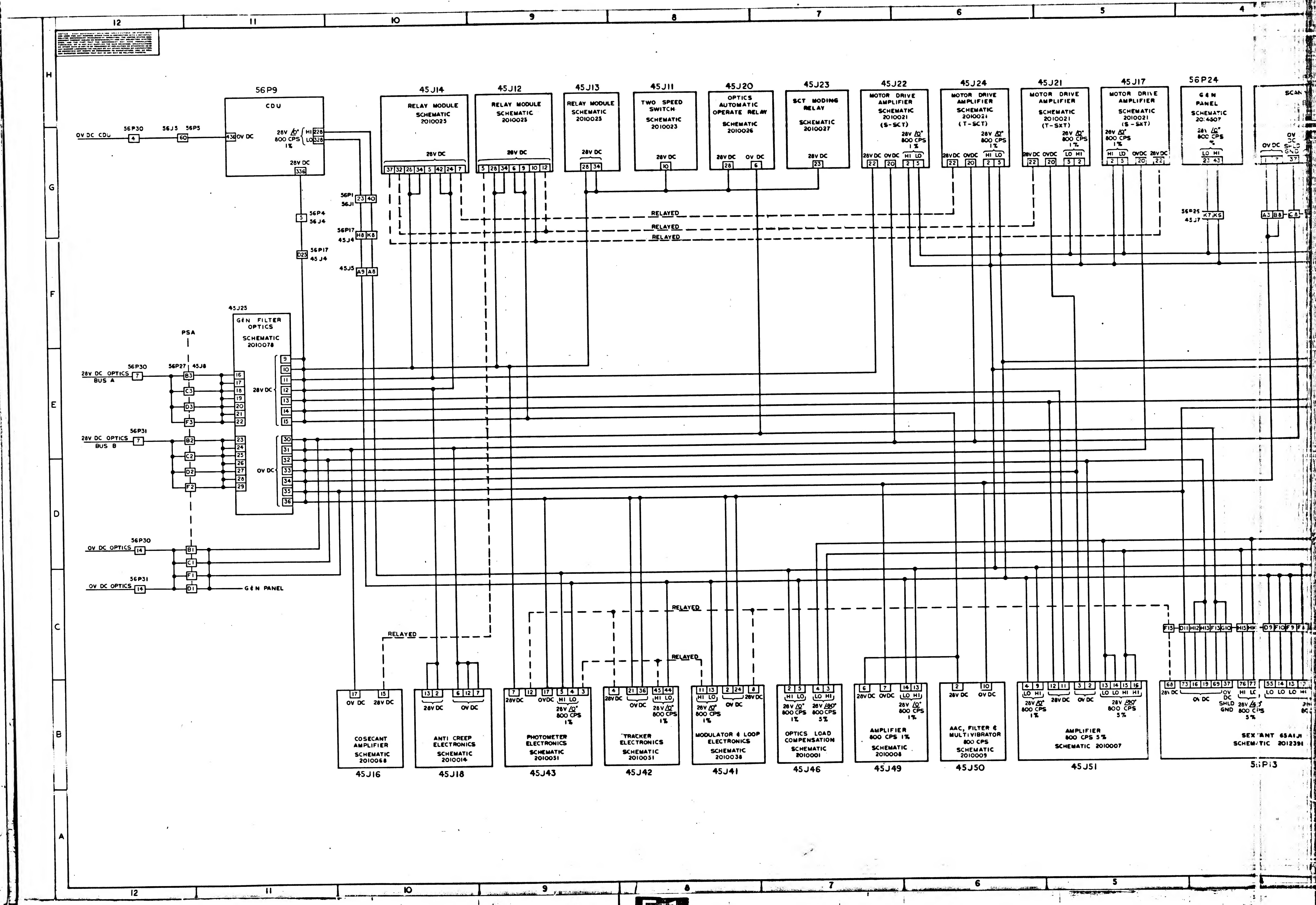
OPTICAL SUBSYSTEM
POWER DISTRIBUTION
BLOCK II

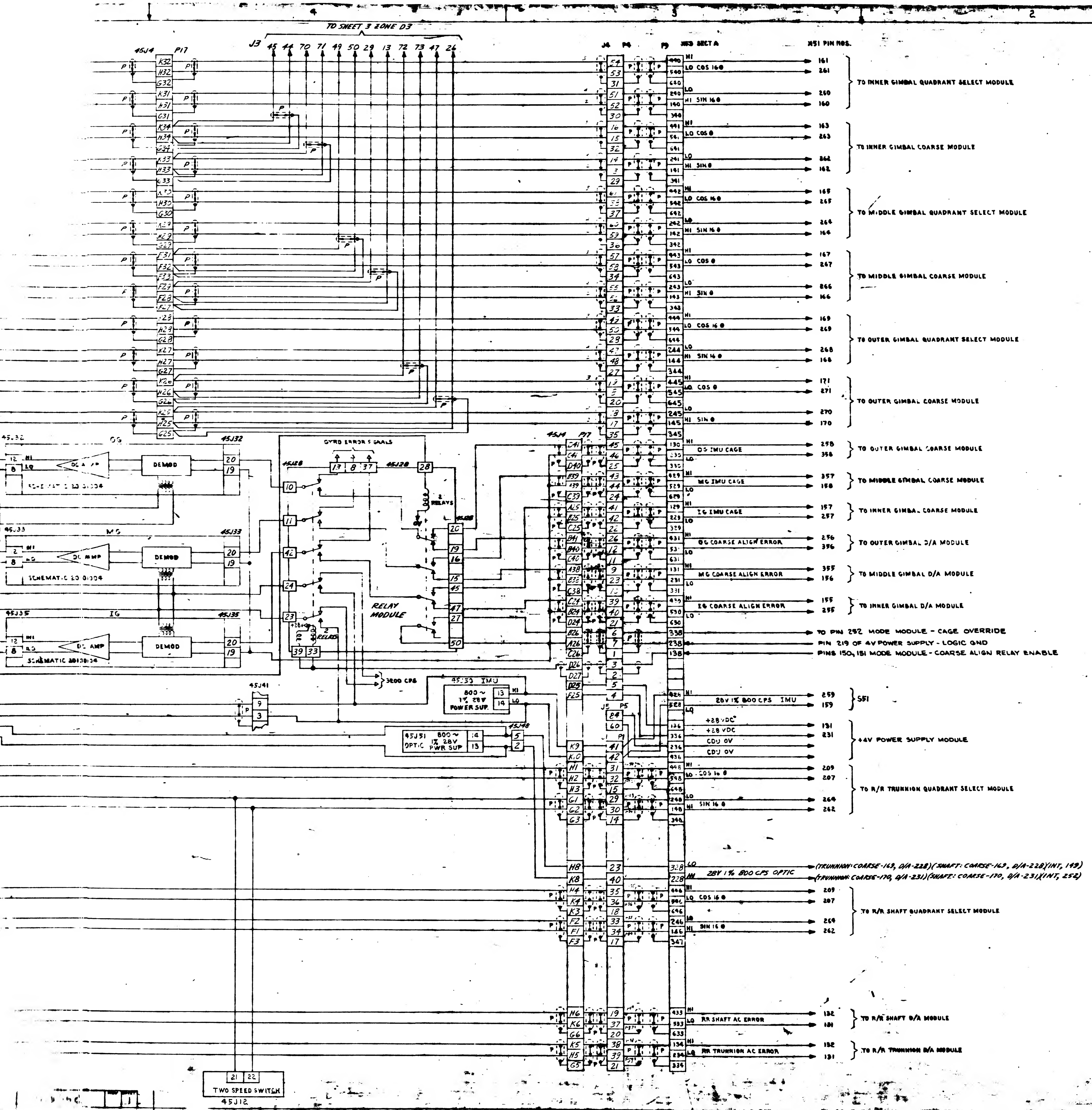
CODE IDENT NO.
SIZE J
DRAWING NO. 2015507
SCALE —
SHEET 1 OF 1

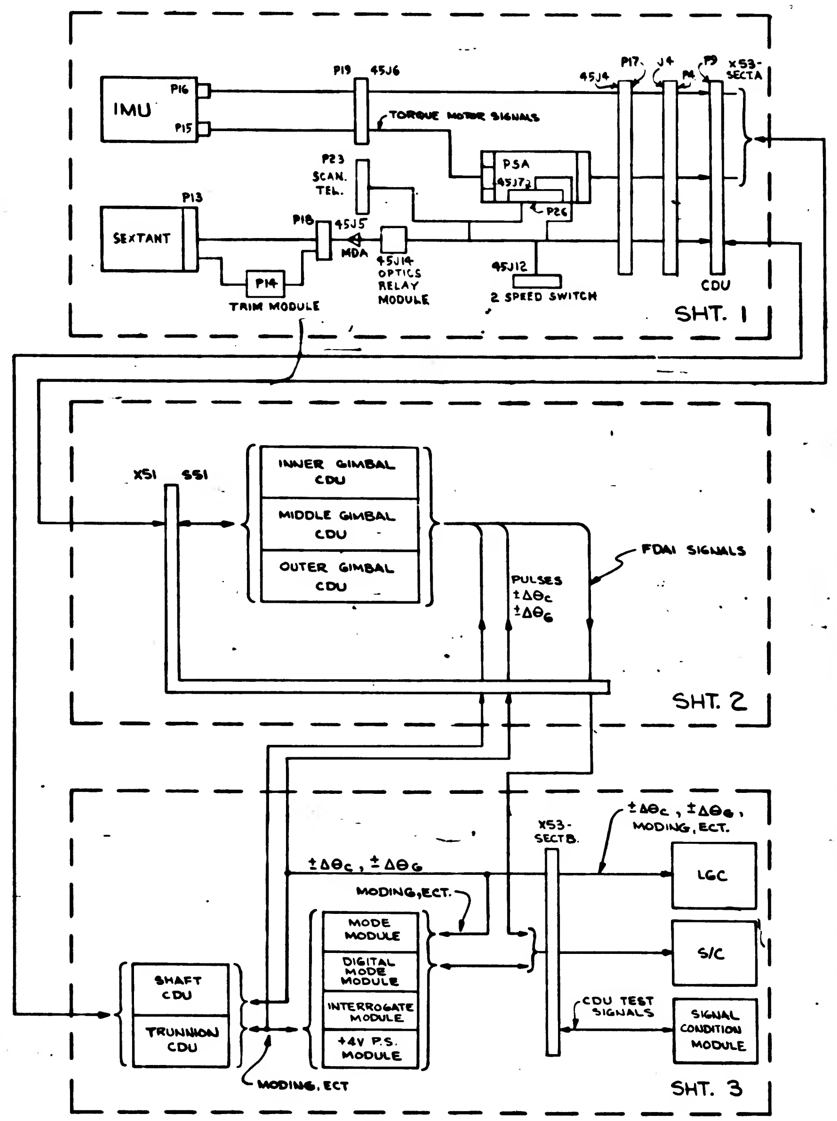
2015507

E-2

NOTICE: WHEN GOVERNMENT DRAWINGS, SPECIFICATIONS, OR OTHER DATA ARE USED FOR ANY PURPOSE OTHER THAN IN CONNECTION WITH A DEFINITELY RELATED GOVERNMENT PROCUREMENT OPERATION, THE UNITED STATES GOVERNMENT THEREBY INCURS NO RESPONSIBILITY NOR ANY OBLIGATION WHATSOEVER, AND THE FACT THAT THE GOVERNMENT MAY HAVE FORMULATED, FURNISHED, OR IN ANY WAY SUPPLIED THE SAID DRAWINGS, SPECIFICATIONS OR OTHER DATA IS NOT TO BE REGARDED BY IMPLICATION OR OTHERWISE AS IN ANY MANNER LICENSING THE HOLDER OR ANY OTHER PERSON OR CORPORATION, OR CONVEYING ANY RIGHTS OR PERMISSION TO MANUFACTURE, USE, OR SELL ANY PATENTED INVENTION THAT MAY IN ANY WAY BE RELATED THERETO.







BLOCKS SHOWN IDENTIFY LOCATION OF PERTINENT SYSTEM FUNCTIONS & COMPONENTS RELATIVE TO APPLICABLE DRAWING SHEET NO..

QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	FIND NO.

LIST OF MATERIALS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS ± DECIMALS ± ANGLES ±
DO NOT SCALE THIS DRAWING
MATERIAL
HEAT TREATMENT
FINAL FINISH

NEXT ASSY | USED ON
APPLICATION

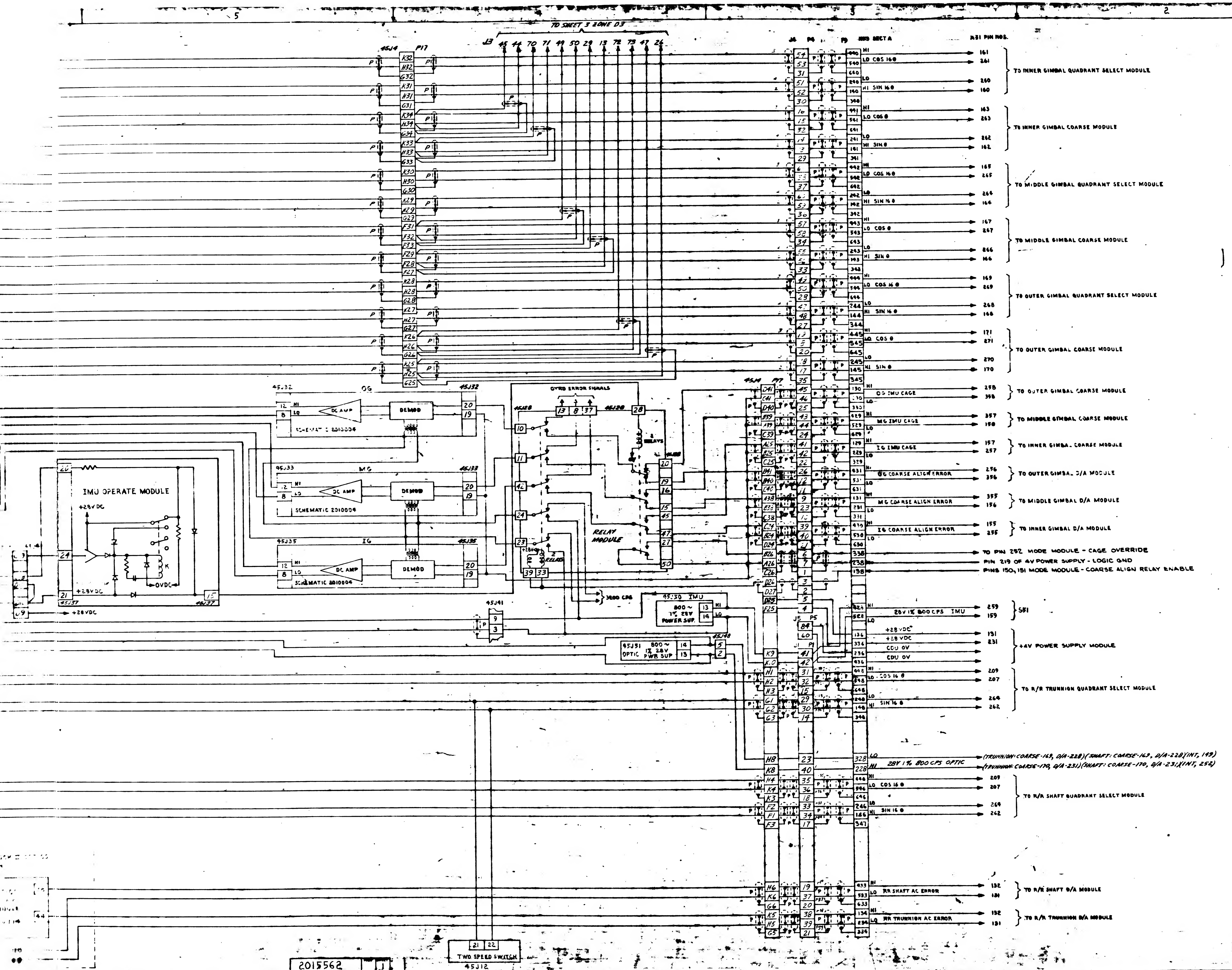
MIT INSTRUMENTATION LAB
CAMBRIDGE, MASS.
DRAWN P. DUNCAN DATE 7-1-65
CHECKED
APPROVAL J. Gilmore 7/65
APPROVAL J.E. Miller
NASA APPROVAL NOT REQUIRED PER LETTER NASA PP7 65-812
MIT APPROVAL

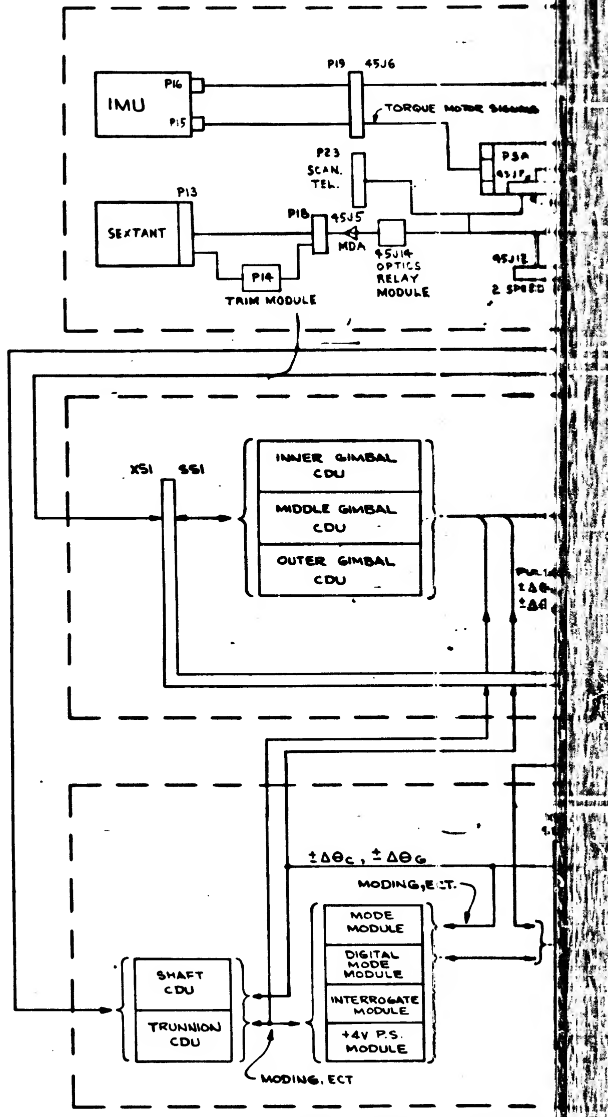
MANNED SPACECRAFT CENTER
HOUSTON, TEXAS

CSM 5-AXIS MODING

CODE IDENT NO. | SIZE | NASA DRAWING NO. 2015562
SCALE | SHEET 1 OF 3

GILMORE


TO SHEET 3 ZONE D3
J3 45 44 70 71 49 50 29 13 72 73 47 26
45J4 P17
J4 P6 P9 J33 SECT A
A31 PIN NOS.
HI LO COS 16θ 161 261
LO HI SIN 16θ 260 160
TO INNER GIMBAL QUADRANT SELECT MODULE
HI LO COS θ 163 263
LO HI SIN θ 262 162
TO INNER GIMBAL COARSE MODULE
HI LO COS 16θ 165 265
LO HI SIN 16θ 264 164
TO MIDDLE GIMBAL QUADRANT SELECT MODULE
HI LO COS θ 167 267
LO HI SIN θ 266 166
TO MIDDLE GIMBAL COARSE MODULE
HI LO COS 16θ 169 269
LO HI SIN 16θ 268 168
TO OUTER GIMBAL QUADRANT SELECT MODULE
HI LO COS θ 171 271
LO HI SIN θ 270 170
TO OUTER GIMBAL COARSE MODULE
OG IMU CAGE 258 358
TO OUTER GIMBAL COARSE MODULE
MG IMU CAGE 357 158
TO MIDDLE GIMBAL COARSE MODULE
IG IMU CAGE 157 257
TO INNER GIMBAL COARSE MODULE
OG COARSE ALIGN ERROR 256 356
TO OUTER GIMBAL D/A MODULE
MG COARSE ALIGN ERROR 355 156
TO MIDDLE GIMBAL D/A MODULE
IG COARSE ALIGN ERROR 155 255
TO INNER GIMBAL D/A MODULE
TO PIN 252 MODE MODULE - CAGE OVERRIDE
PIN 219 OF 4V POWER SUPPLY - LOGIC GND
PINS 150, 151 MODE MODULE - COARSE ALIGN RELAY ENABLE
28V 1% 800 CPS IMU 259 159
SS1
+28VDC
+28 VDC
CDU OV
CDU OV
131 231
+4V POWER SUPPLY MODULE
LO COS 16 θ 209 207
SIN 16 θ 264 262
TO R/R TRUNNION QUADRANT SELECT MODULE
28V 1% 800 CPS OPTIC
(TRUNNION: COARSE-169, D/A-228)(SHAFT: COARSE-169, D/A-228)(INT, 149)
(TRUNNION: COARSE-170, D/A-231)(SHAFT: COARSE-170, D/A-231)(INT, 252)
COS 16 θ 209 207
SIN 16 θ 264 262
TO R/R SHAFT QUADRANT SELECT MODULE
RR SHAFT AC ERROR 132 131
TO R/R SHAFT D/A MODULE
RR TRUNNION AC ERROR 132 131
TO R/R TRUNNION D/A MODULE
45J32 OG 45J32
DC AMP
DEMOD
SCHEMATIC 2010004
45J33 MG 45J33
DC AMP
DEMOD
SCHEMATIC 2010004
45J35 IG 45J35
DC AMP
DEMOD
SCHEMATIC 2010004
IMU OPERATE MODULE
+28VDC
K
OVDC
+28VDC
45J37
+28VDC
GYRO ERROR SIGNALS
45J28
2 RELAYS
RELAY MODULE
3200 CPS
45J41
45J30 IMU
800 ~ 1% 28V POWER SUP.
45J31 OPTIC
800 ~ 1% 28V PWR SUP
45J48
45J4 P17
J5 P5
TWO SPEED SWITCH
45J12
2015562
J
5 4 3 2



BLOCKS SHOWN IDENTIFY LOCATION
SYSTEM FUNCTIONS & COMPONENTS R
APPLICABLE DRAWING SHEET NO.

QTY REQD	PART OR IDENTIFYING NO.

NEXT ASSY	USED ON
APPLICATION	

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DIMENSIONS ARE IN INCHES
TOLERANCES ON
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MATERIAL
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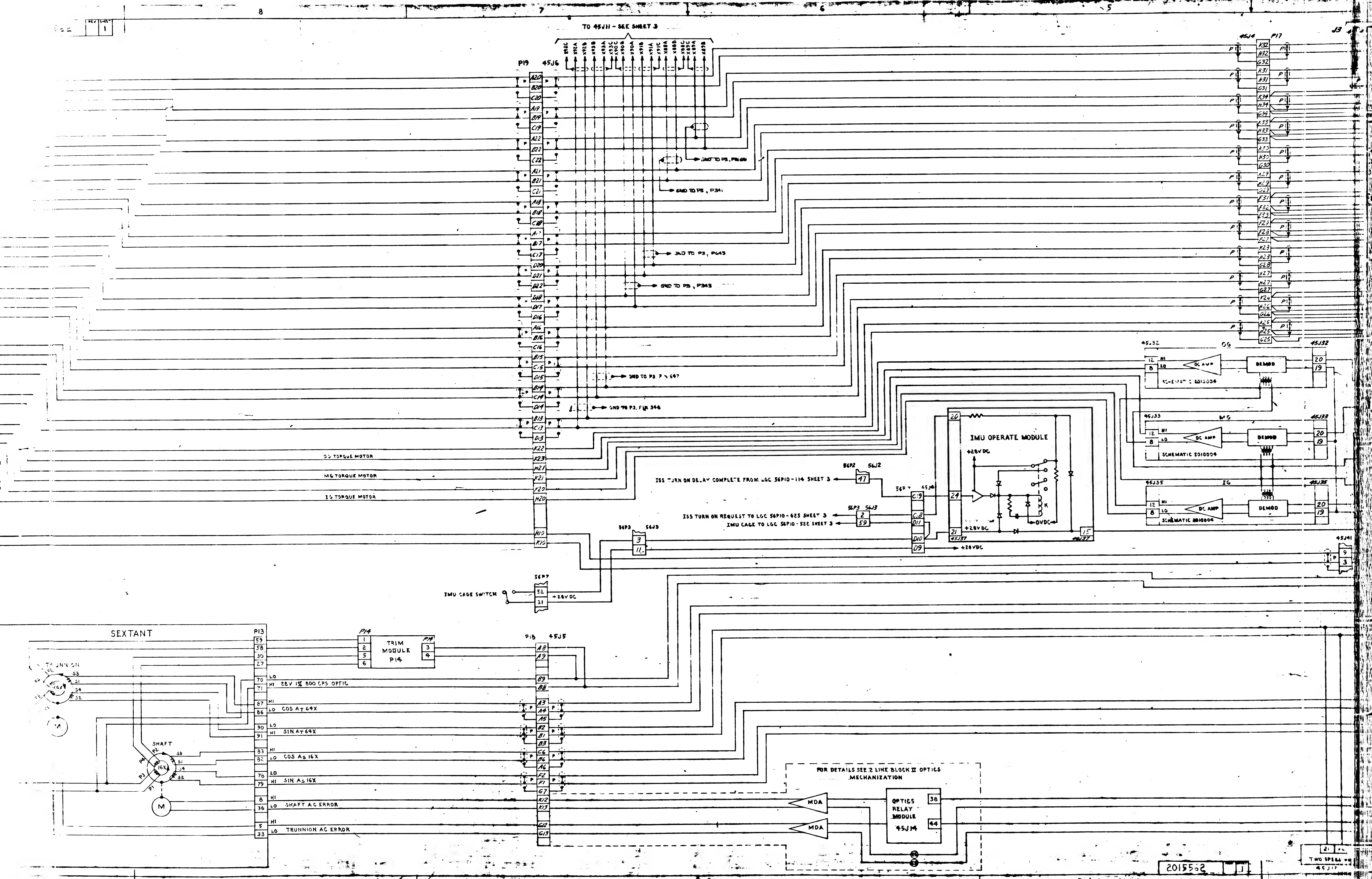
DWG NO. CONTRACT
DRAWN P. DUNCAN DATE 7-1-65
CHECKED
APPROVAL
APPROVAL
NASA APPROVAL NASA PI 65-612
MIT APPROVAL


8
7
6
5
TO 45J11 - SEE SHEET 3
X92C
X92A
X92B
X93B
X93A
X93C
X90C
X90B
X90A
X91B
X91A
X91C
X88A
X88B
X88C
X89C
X89A
X89B
P19
45J6
A20
B20
C20
A19
B19
C19
A22
B22
C22
A21
B21
C21
A18
B18
C18
B17
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B14
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D13
K22
K23
H21
K21
K20
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H10
K10
P
GND TO P3, P1N 611
GND TO P3, P341
GND TO P3, P643
GND TO P3, P343
GND TO P3, P N 647
GND TO P3, PIN 348
OG TORQUE MOTOR
MG TORQUE MOTOR
IG TORQUE MOTOR
45J4
P17
J3
K32
H32
G32
K31
H31
G31
K34
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G34
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G33
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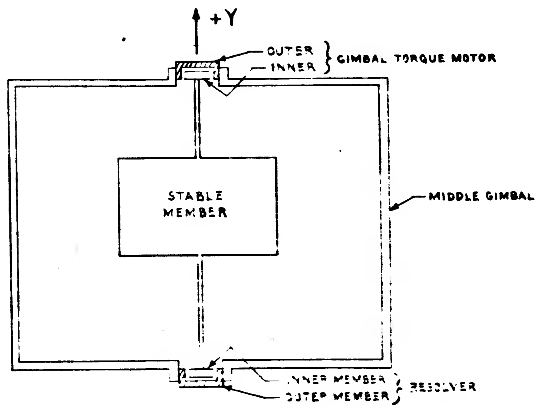
G25
45J32
OG
12
8
HI
LO
DC AMP
DEMOD
SCHEMATIC 2010004
20
19
45J33
MG
45J35
IG
45J41
9
3
IMU OPERATE MODULE
+28VDC
0VDC
K
20
24
21
15
45J37
56P2
56J2
47
ISS TURN ON DELAY COMPLETE FROM LGC 56P10-114 SHEET 3
56P7
45J4
C19
C18
D11
D10
D9
56P3
56J3
2
59
ISS TURN ON REQUEST TO LGC 56P10-625 SHEET 3
IMU CAGE TO LGC 56P10-522 SHEET 3
3
11
+28VDC
56P7
52
31
IMU CAGE SWITCH
SEXTANT
TRUNNION
64X
S3
S1
S4
S2
M
SHAFT
16X
P1
P2
P3
P4
P13
59
58
30
27
70
71
87
86
90
91
83
82
76
79
8
36
5
33
LO
HI
28V 1% 800 CPS OPTIC
COS AT 64X
SIN AT 64X
COS AS 16X
SIN AS 16X
SHAFT AC ERROR
TRUNNION AC ERROR
P14
1
2
5
6
TRIM MODULE P14
3
4
P18
45J5
A8
A9
B9
B8
A3
A4
A5
B2
B1
B3
C6
B6
A6
F2
F1
G7
K12
K13
G12
G13
FOR DETAILS SEE 2 LINE BLOCK II OPTICS MECHANIZATION
MDA
OPTICS RELAY MODULE 45J14
38
44
21
TWO SPEED
45J11
2015562
J

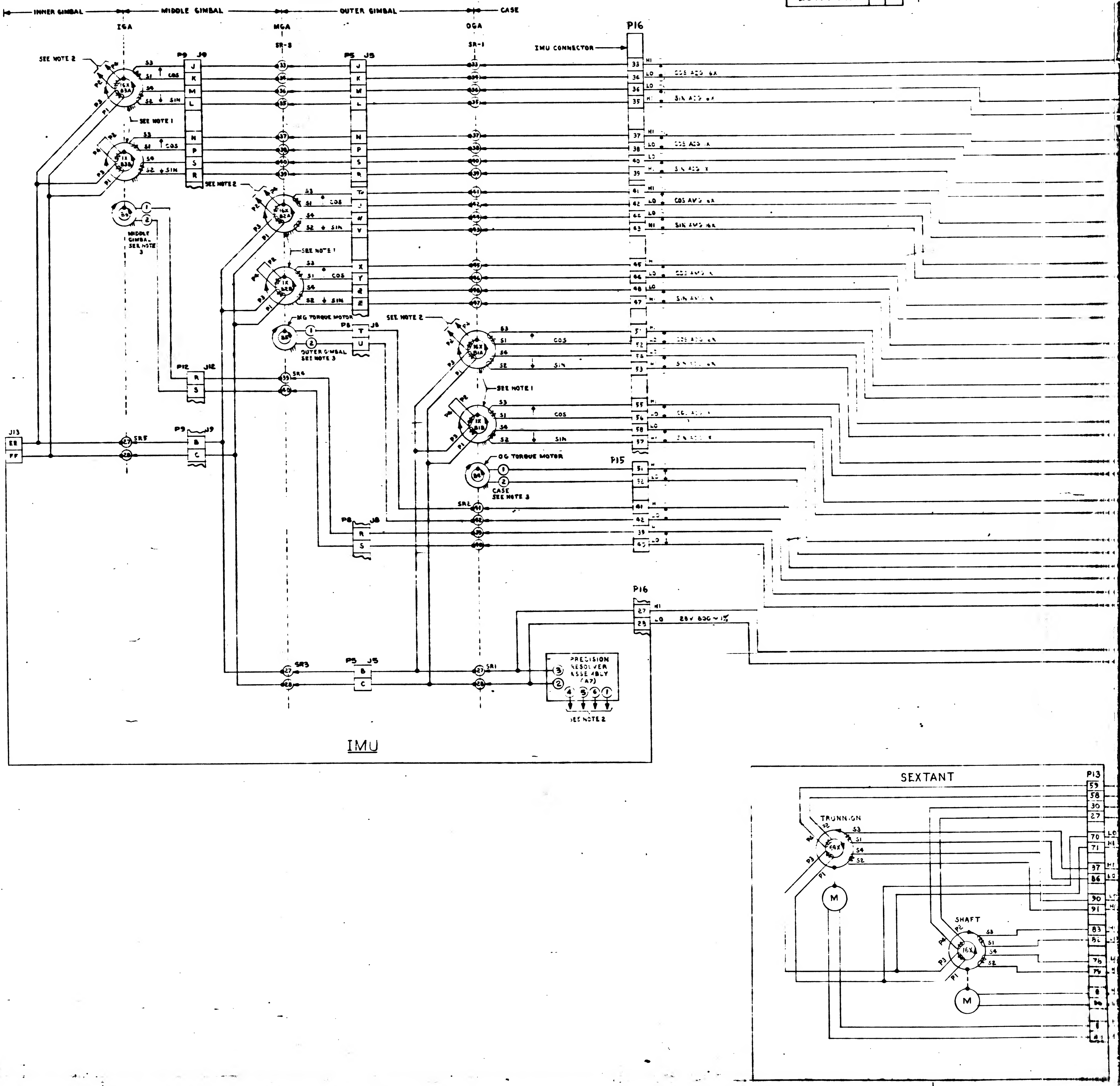
2015562 REV SHEET 1

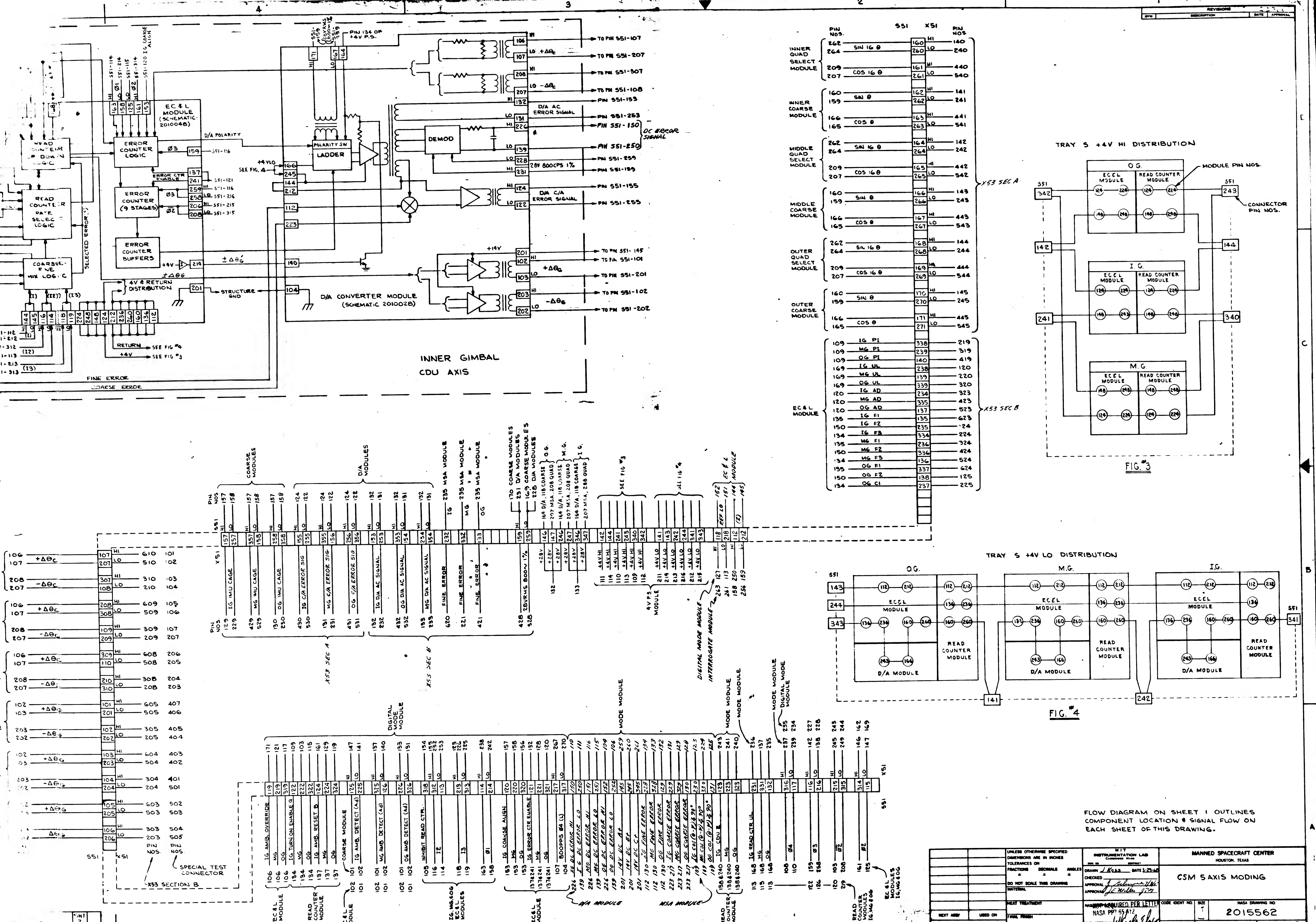


RESOLVER PHASING
VIEW I
(TYPICAL)

PHASING NOTES:

1. a. FOR EACH GIMBAL AXIS THE RESOLVER INNER MEMBER IS FIXED TO THE INNERMOST GIMBAL MEMBER (SEE VIEW I) AND OUTER MEMBER IS FIXED TO THE OUTER MOST GIMBAL MEMBER.
   b. FOR EACH GIMBAL THE RESOLVER AND MOTOR ASSEMBLYS ARE LOCATED AT THE NEGATIVE AND POSITIVE ENDS OF THE GIMBAL RESPECTIVELY
   c. IMU S/C INSTALLATION IN BLOCK II IS SUCH THAT THE IMU AXES, THE ZEROED GIMBAL AXES AND THE S/C AXES ARE ALIGNED.
   d. POSITIVE ANGLES ARE DEFINED ONE AXIS AT A TIME MEASURED FROM AN IMU ZERO GIMBAL POSITION.
   e. FOR INERTIALLY STABILIZED OPERATION, IMU GIMBALS INITIALLY ORTHOGONAL AND AT ZERO, CLOCKWISE ROTATION OF THE SPACECRAFT WHEN VIEWED OUT ALONG THE POSITIVE GIMBAL AXIS IS DEFINED AS POSITIVE ROTATION AND RESULTS IN POSITIVE GIMBAL ROTATION
   THUS (PER "e" ABOVE), RELATIVE GIMBAL MOTION FOR A POSITIVE ROTATION WHEN VIEWED ALONG THE POSITIVE AXIS IS: (SEE VIEW I)
      (1) INERTIAL: CLOCKWISE ROTATION OF THE MIDDLE GIMBAL WITH RESPECT TO THE STABLE MEMBER, CLOCKWISE ROTATION OF THE OUTER GIMBAL WITH RESPECT TO THE MIDDLE GIMBAL, ETC.
      (2) COARSE ALIGNMENT: COUNTER CLOCKWISE ROTATION OF THE STABLE MEMBER WITH RESPECT TO THE MIDDLE GIMBAL, COUNTER CLOCKWISE ROTATION OF THE MIDDLE GIMBAL WITH RESPECT TO THE OUTER GIMBAL, ETC.
   g. POSITIVE ROTATION OF THE INNER RESOLVER AND OUTER RESOLVER MEMBERS (RELATIVE TO EACH OTHER AND IN ACCORDANCE WITH "F" ABOVE) IS SHOWN ON THE SCHEMATIC.
   h. POSITIVE ROTATION FROM THE ZERO GIMBAL POSITION IN THE FIRST QUADRANT OF ELECTRICAL DEGREES RESULTS IN AN INCREASING IN PHASE OUTER MEMBER SINE WINDING VOLTAGE AND DECREASING OUTER MEMBER COSINE WINDING VOLTAGE.
   i. IN PHASE VOLTAGE IS DEFINED WITH RESPECT TO THE REFERENCE 28V 800 cps 1% EXCITATION. P3 IS THE HIGH ON ALL RESOLVER INNER MEMBERS. THE REFERENCE ARROWS BETWEEN THE OUTER MEMBER WINDINGS (S_2 S_4) IDENTIFY THE IN PHASE RELATIONSHIP FOR GIMBAL ANGLES FROM −90° TO 90° ELECTRICAL COS WINDING, 0° TO 180° ELECTRICAL SINE WINDING.
2. ZERO BIAS ADJUSTMENT WINDINGS CONNECTED TO PRECISION RESOLVER ASSEMBLY. ADJUSTMENT MADE IN PRECISION RESOLVER ASSEMBLY TO SET ELECTRICAL NULL OF COINCIDENT 16X RESOLVER TO COINCIDE WITH ZERO GIMBAL ANGLES (REFERENCE E-1230). SEE IMU WIRING DIAGRAM 2015615 FOR INTERCONNECTION DETAILS.
3. a. THE GIMBAL TORQUE MOTOR ROTOR IS FIXED TO THE INNER GIMBAL MEMBER (SEE VIEW I).
   b. POSITIVE ROTATION IS DEFINED AS IN NOTE "1" ABOVE AND SHOWN BY REFERENCE ARROWS ON THE MOTOR.
   c. A POSITIVE DC VOLTAGE APPLIED AT PIN 1 WITH RESPECT TO PIN 2 OF EACH MOTOR WILL RESULT IN POSITIVE GIMBAL ROTATION.

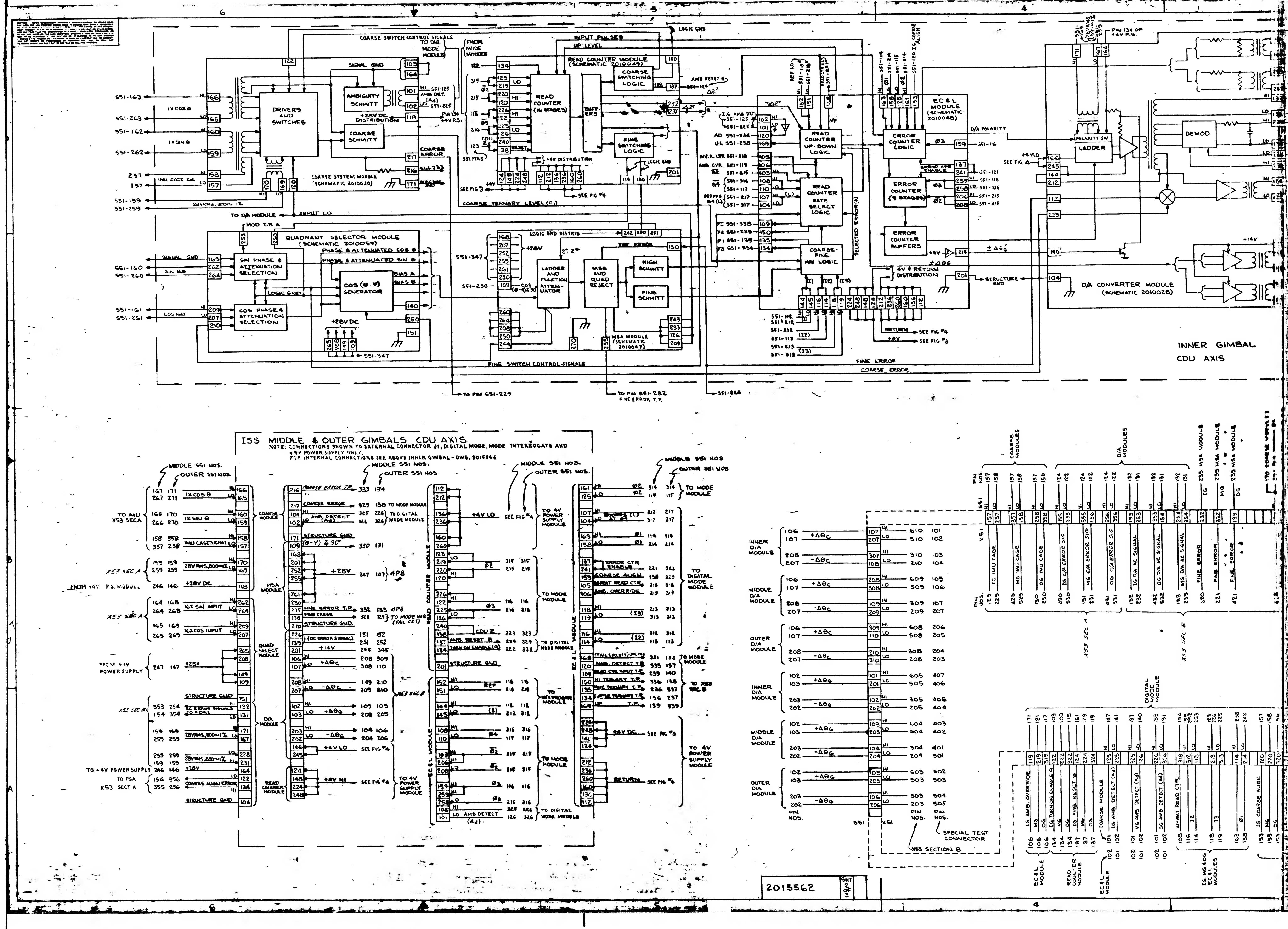




FLOW DIAGRAM ON SHEET 1 OUTLINES COMPONENT LOCATION & SIGNAL FLOW ON EACH SHEET OF THIS DRAWING.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS ± DECIMALS ± ANGLES ± DO NOT SCALE THIS DRAWING	MIT INSTRUMENTATION LAB CAMBRIDGE MASS	MANNED SPACECRAFT CENTER HOUSTON, TEXAS
MATERIAL	DRAWN J Koss DATE 3-29-65 CHECKED APPROVAL J. Helmore 9/8/6- APPROVAL J E Miller	CSM 5 AXIS MODING
HEAT TREATMENT FINAL FINISH	~~NOT~~ REQUIRED PER LETTER NASA PP7 65-412 MIT APPROVAL	CODE IDENT NO. — SIZE J — NASA DRAWING NO. 2015562
NEXT ASSY — USED ON — APPLICATION		SCALE — WT — SHEET 2 OF 3

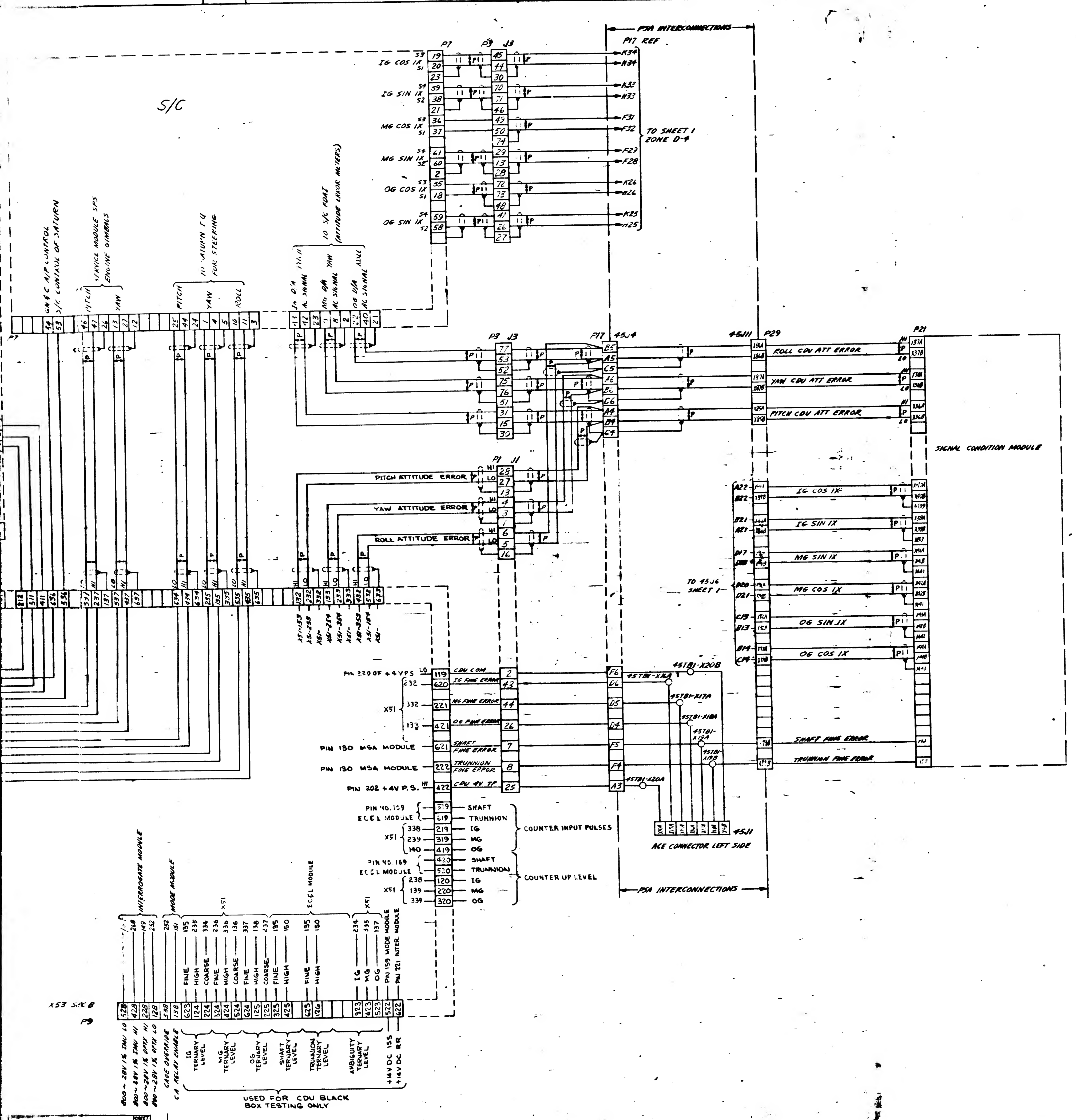
GILMORE



ISS MIDDLE & OUTER GIMBALS CDU AXIS

NOTE: CONNECTIONS SHOWN TO EXTERNAL CONNECTOR J1, DIGITAL MODE, MODE, INTERROGATE AND +4V POWER SUPPLY ONLY. FOR INTERNAL CONNECTIONS SEE ABOVE INNER GIMBAL - DWG. 2015566

2015562 SHT 2 OF 3



REVISIONS

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CSM
5 AXIS MODING

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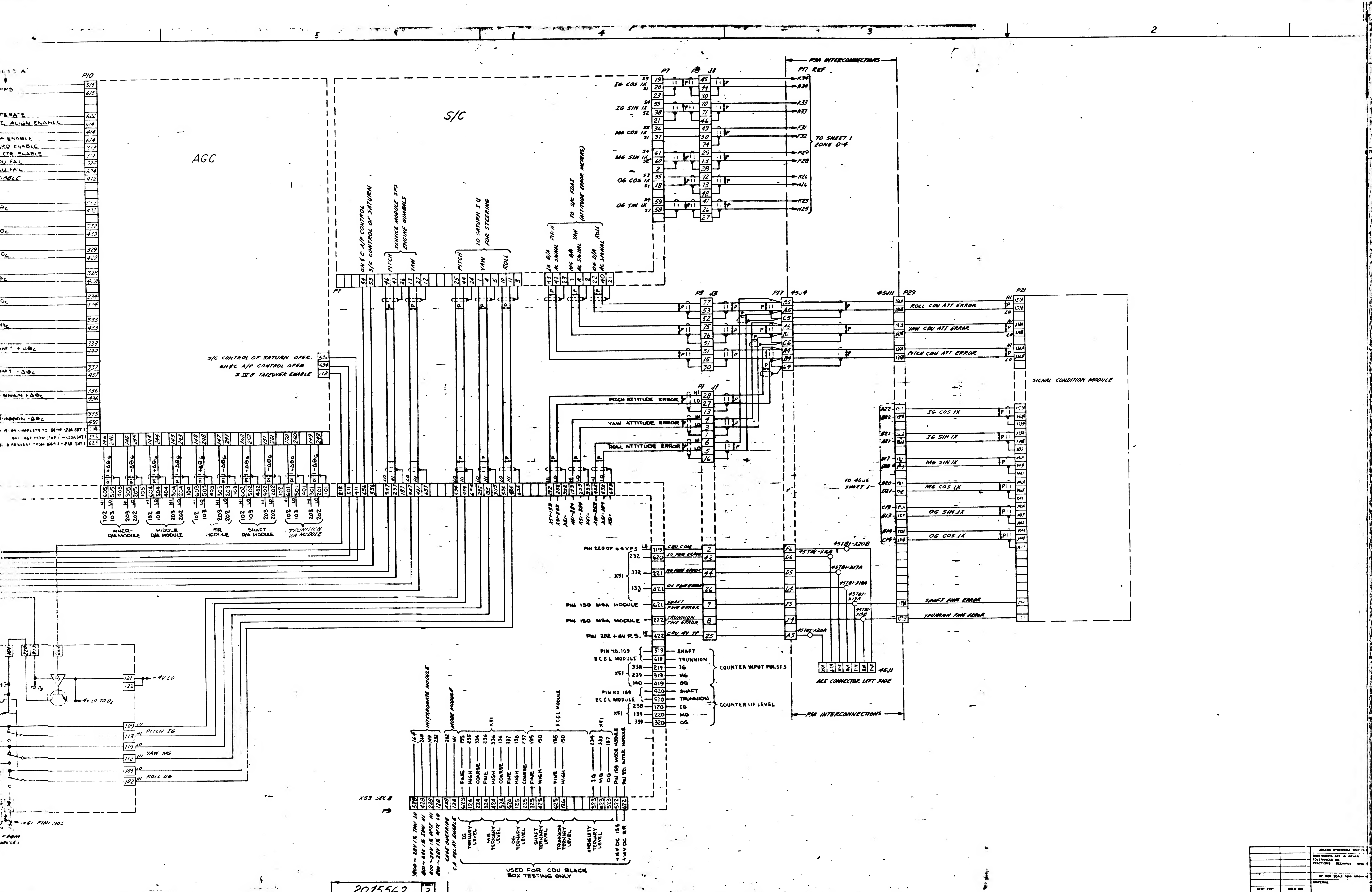
NASA DRAWING NO
2015562
SHEET 3 OF 3

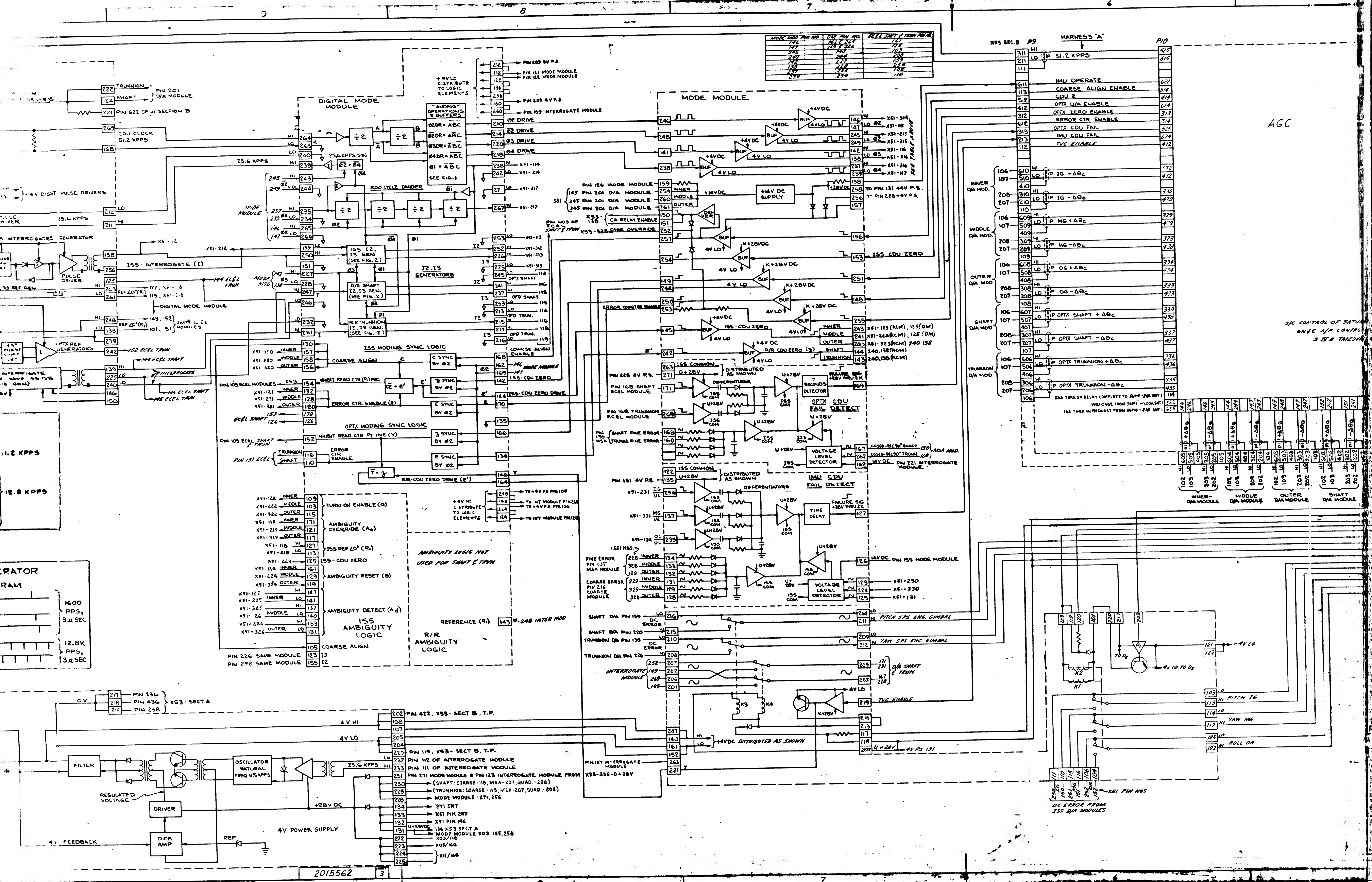
GILMORE

2015562 SHEET 3



2015562 SHEET 3

E3



MODE MOD PIN NO.	DM PIN NO.	EC&L SHFT & TRUN PIN NO.
146	162 & 265	161
147	169 & 266	125
245	243	103
249	244	208
142	227	159
138	228	258
237	233	108
239	234	110

2015562 SHEET 3

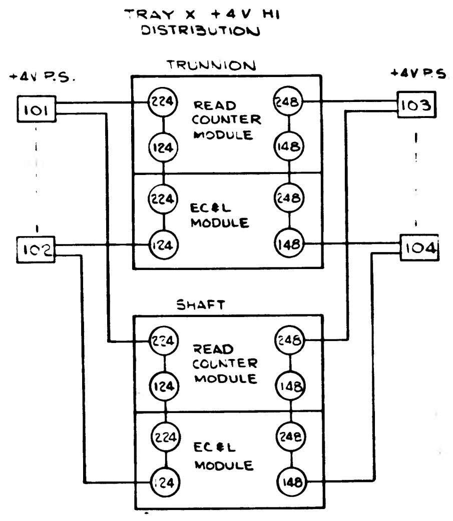


FIGURE #5

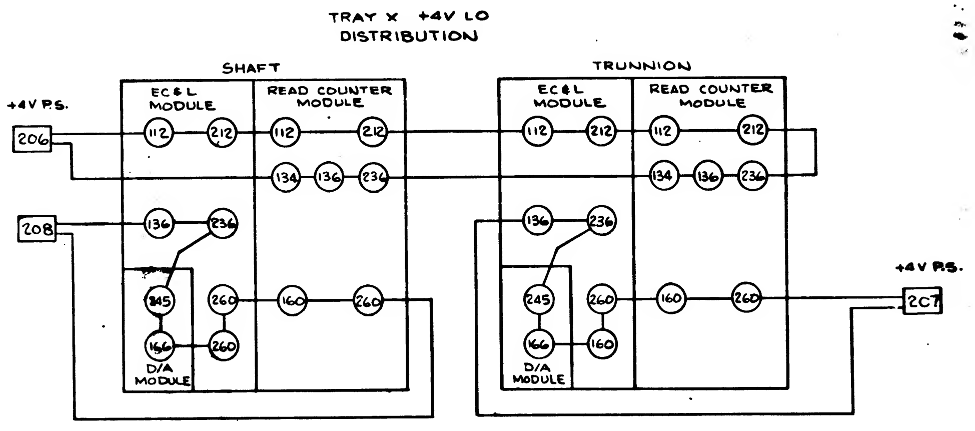
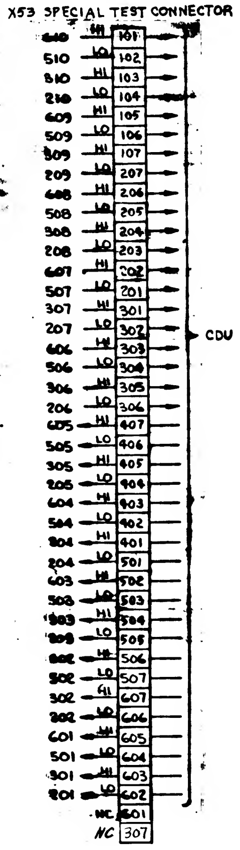
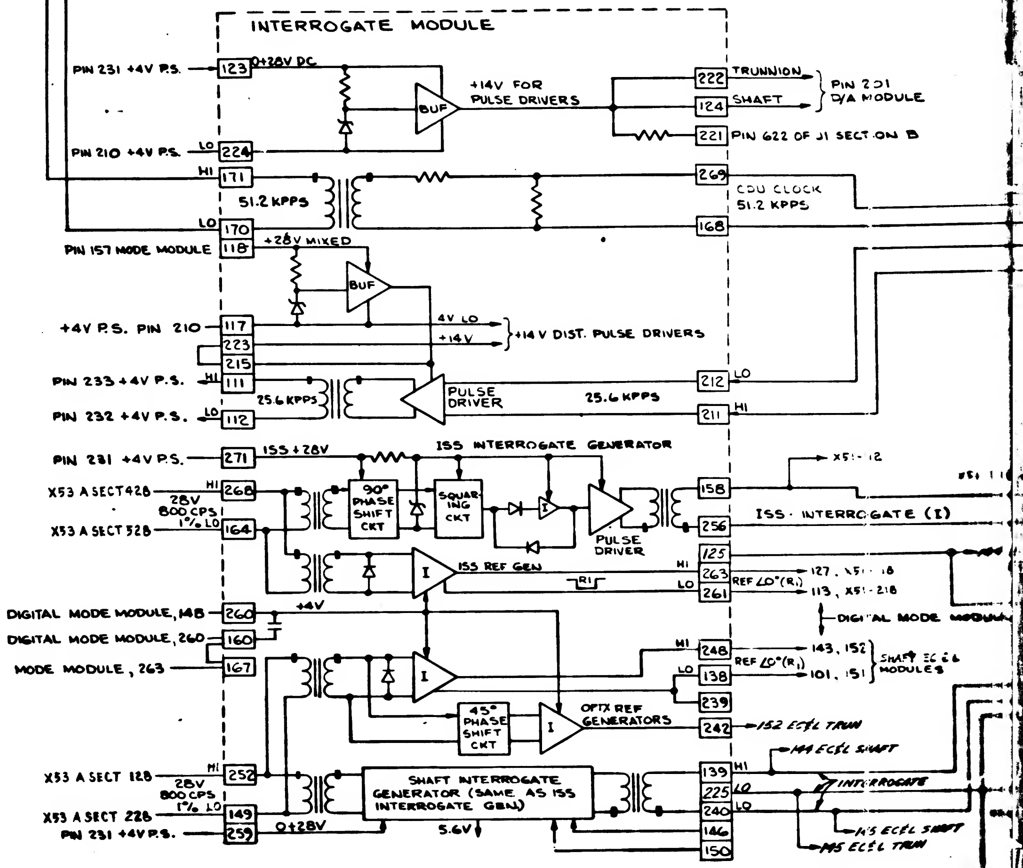


FIGURE #6





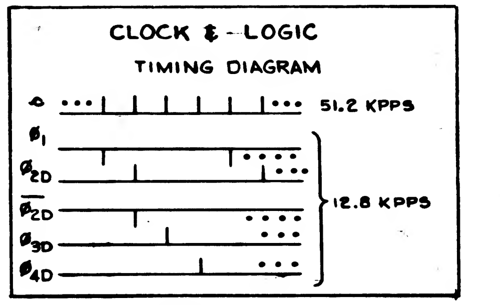


FIGURE 1

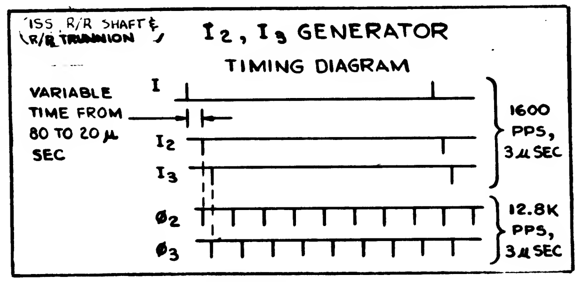
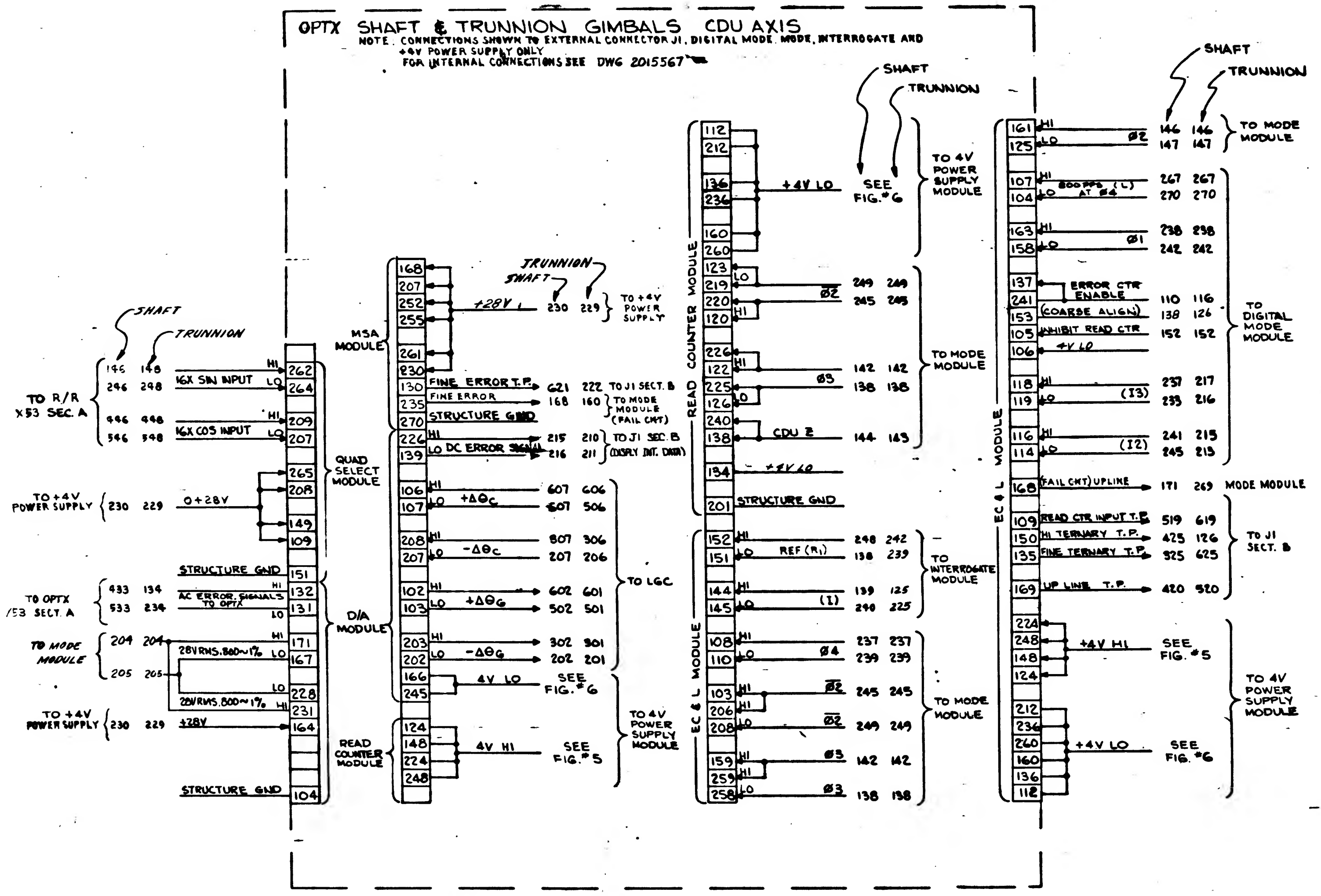
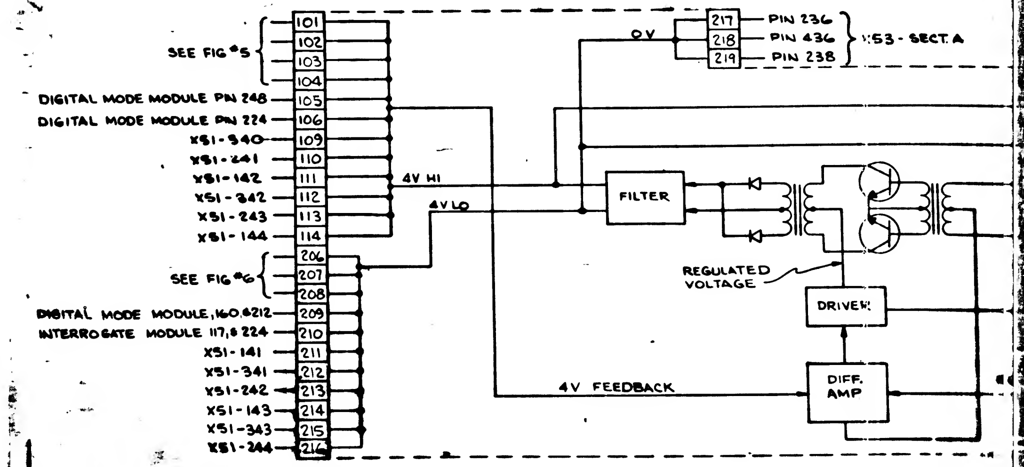

ISS R/R SHAFT & R/R TRUNNION
I2, I3 GENERATOR TIMING DIAGRAM
VARIABLE TIME FROM 80 TO 20 μ SEC
I
I2
I3
1600 PPS, 3 μ SEC
Ø2
Ø3
12.8K PPS, 3 μ SEC

FIGURE-2

OPTX SHAFT & TRUNNION GIMBALS CDU AXIS

NOTE. CONNECTIONS SHOWN TO EXTERNAL CONNECTOR J1, DIGITAL MODE MODE, INTERROGATE AND +4V POWER SUPPLY ONLY. FOR INTERNAL CONNECTIONS SEE DWG 2015567





2015562

SHEET 3

SYM	DESCRIPTION	DATE	APPROVAL
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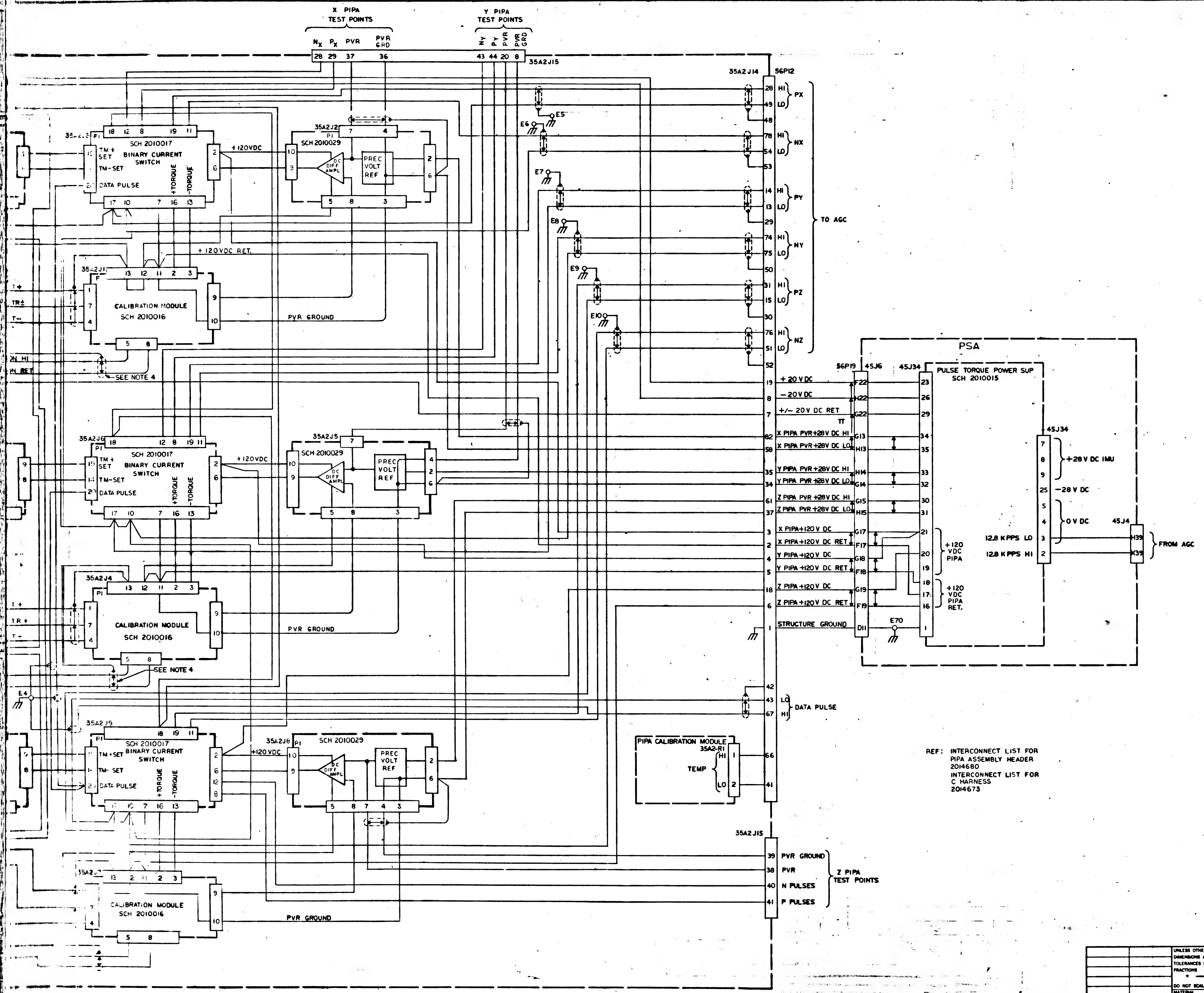
REVISIONS 1463

2015563 A



REF: INTERCONNECT LIST FOR PIPA ASSEMBLY HEADER 2014680
INTERCONNECT LIST FOR C HARNESS 2014673

QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	FIND NO

LIST OF MATERIALS

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APPROVAL J S. 12/7/64
NASA APPROVAL W. J. Rhine 12-8-64
MIT APPROVAL W. Kupfer

MANNED SPACECRAFT CENTER
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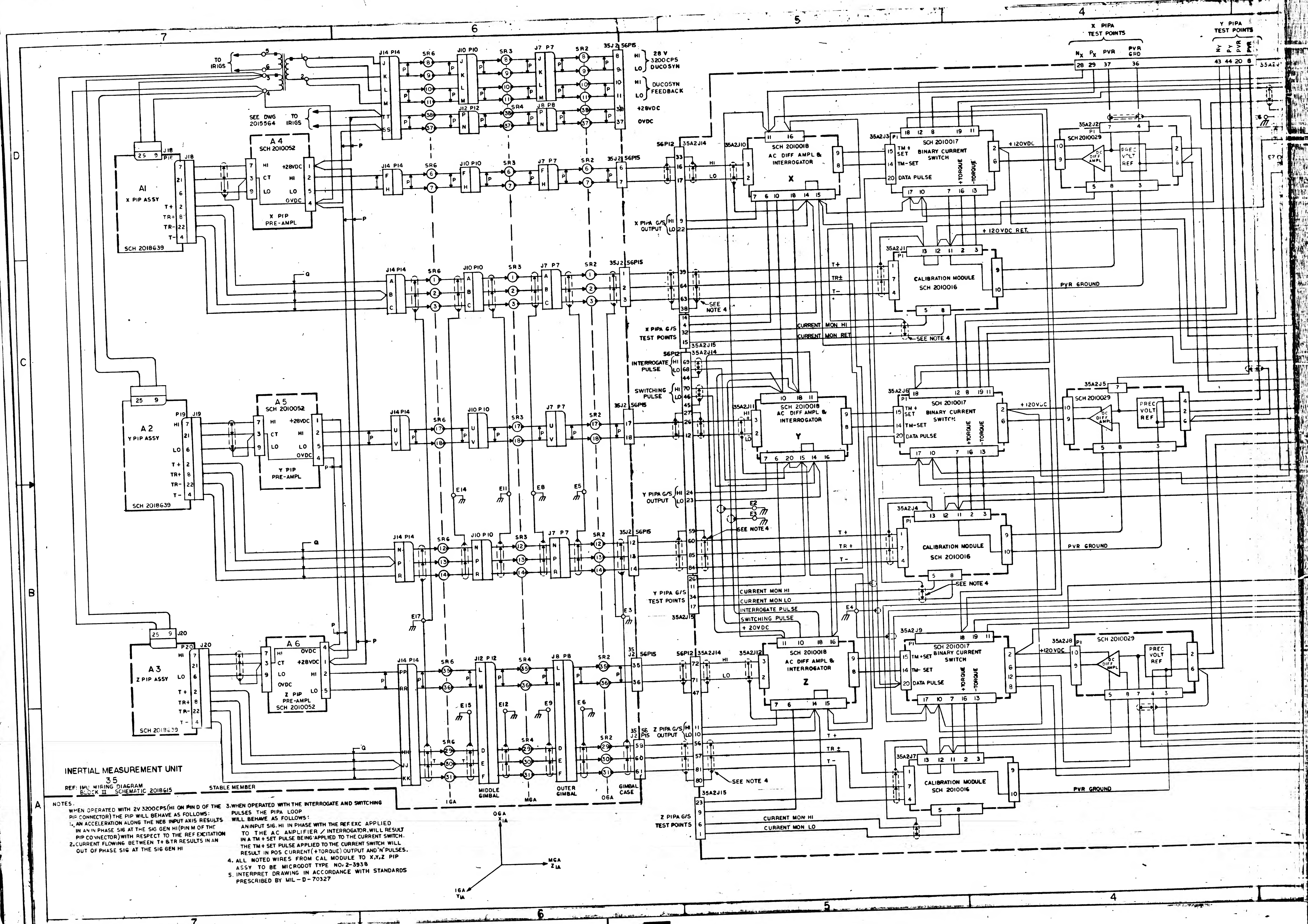
TWO WIRE MECHANIZATION OF APOLLO PIPA LOOPS

CODE IDENT NO 80230
SIZE J
NASA DRAWING NO. 2015563
SCALE —
WT —
SHEET 1 OF 1

MASTER

21



INERTIAL MEASUREMENT UNIT

35

REF: IMU WIRING DIAGRAM
BLOCK II SCHEMATIC 2018615

NOTES.

WHEN OPERATED WITH 2V 3200CPS(HI ON PIN D OF THE PIP CONNECTOR) THE PIP WILL BEHAVE AS FOLLOWS:

1. AN ACCELERATION ALONG THE NEG INPUT AXIS RESULTS IN AN IN PHASE SIG AT THE SIG GEN HI (PIN M OF THE PIP CONNECTOR) WITH RESPECT TO THE REF EXCITATION
2. CURRENT FLOWING BETWEEN T+ & TR RESULTS IN AN OUT OF PHASE SIG AT THE SIG GEN HI
3. WHEN OPERATED WITH THE INTERROGATE AND SWITCHING PULSES THE PIPA LOOP WILL BEHAVE AS FOLLOWS:
   AN INPUT SIG. HI IN PHASE WITH THE REF. EXC APPLIED TO THE AC AMPLIFIER / INTERROGATOR, WILL RESULT IN A TM + SET PULSE BEING APPLIED TO THE CURRENT SWITCH. THE TM + SET PULSE APPLIED TO THE CURRENT SWITCH WILL RESULT IN POS CURRENT (+TORQUE) OUTPUT AND "N" PULSES.
4. ALL NOTED WIRES FROM CAL MODULE TO X,Y,Z PIP ASSY TO BE MICRODOT TYPE NO. 2-3938
5. INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY MIL-D-70327

2015563 B

SYM	DESCRIPTION	DATE	APPROVAL
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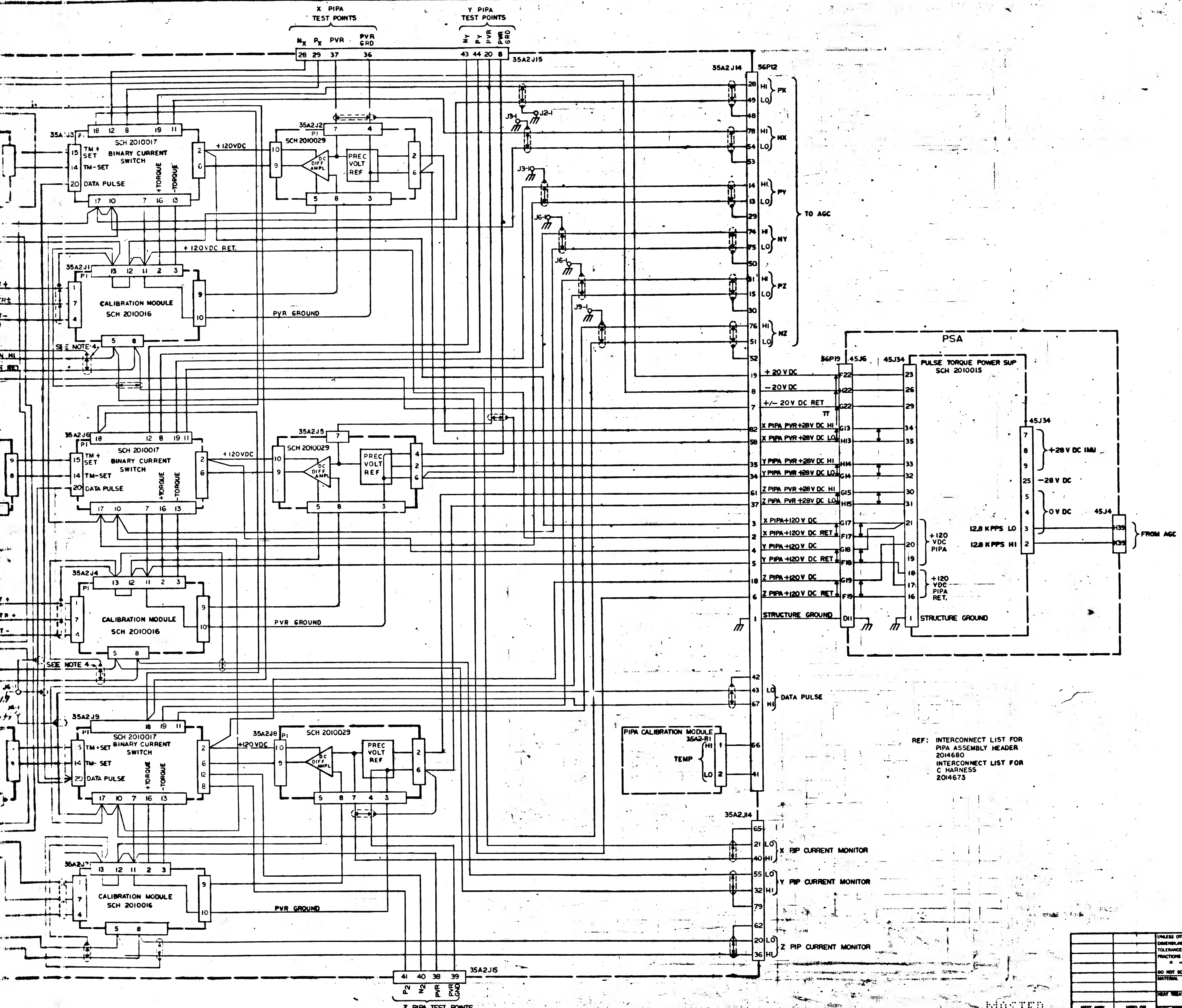
B	REVISED PER TDRR 29124	5-24-66	[illegible]

REVISIONS 14697



REF: INTERCONNECT LIST FOR PIPA ASSEMBLY HEADER 2014680
INTERCONNECT LIST FOR C HARNESS 2014673

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APPROVAL J S[illegible] 12/7/64
NASA APPROVAL W [illegible] 12-8-64
MIT APPROVAL W Kapp[illegible]

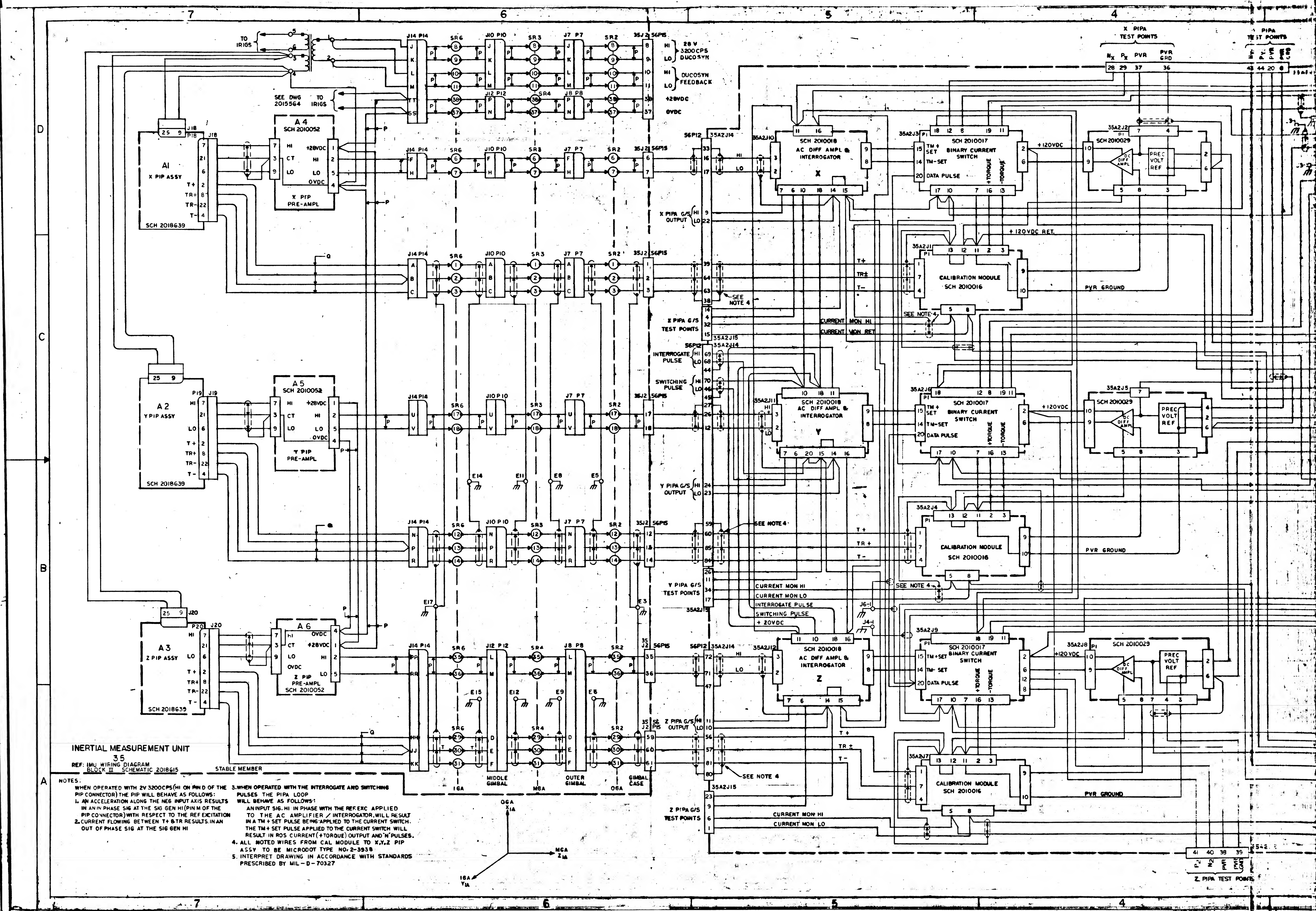
MANNED SPACECRAFT CENTER
HOUSTON, TEXAS

TWO WIRE MECHANIZATION
OF APOLLO PIPA LOOPS

CODE IDENT NO. 80230
SIZE J
NASA DRAWING NO. 2015563
SCALE —
WT —
SHEET 1 of 1

(24)

F-2



INERTIAL MEASUREMENT UNIT

35

REF: IMU WIRING DIAGRAM
BLOCK II SCHEMATIC 2018615

STABLE MEMBER

NOTES.

WHEN OPERATED WITH 2V 3200CPS (HI ON PIN D OF THE PIP CONNECTOR) THE PIP WILL BEHAVE AS FOLLOWS:

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2. CURRENT FLOWING BETWEEN T+ & TR RESULTS IN AN OUT OF PHASE SIG AT THE SIG GEN HI
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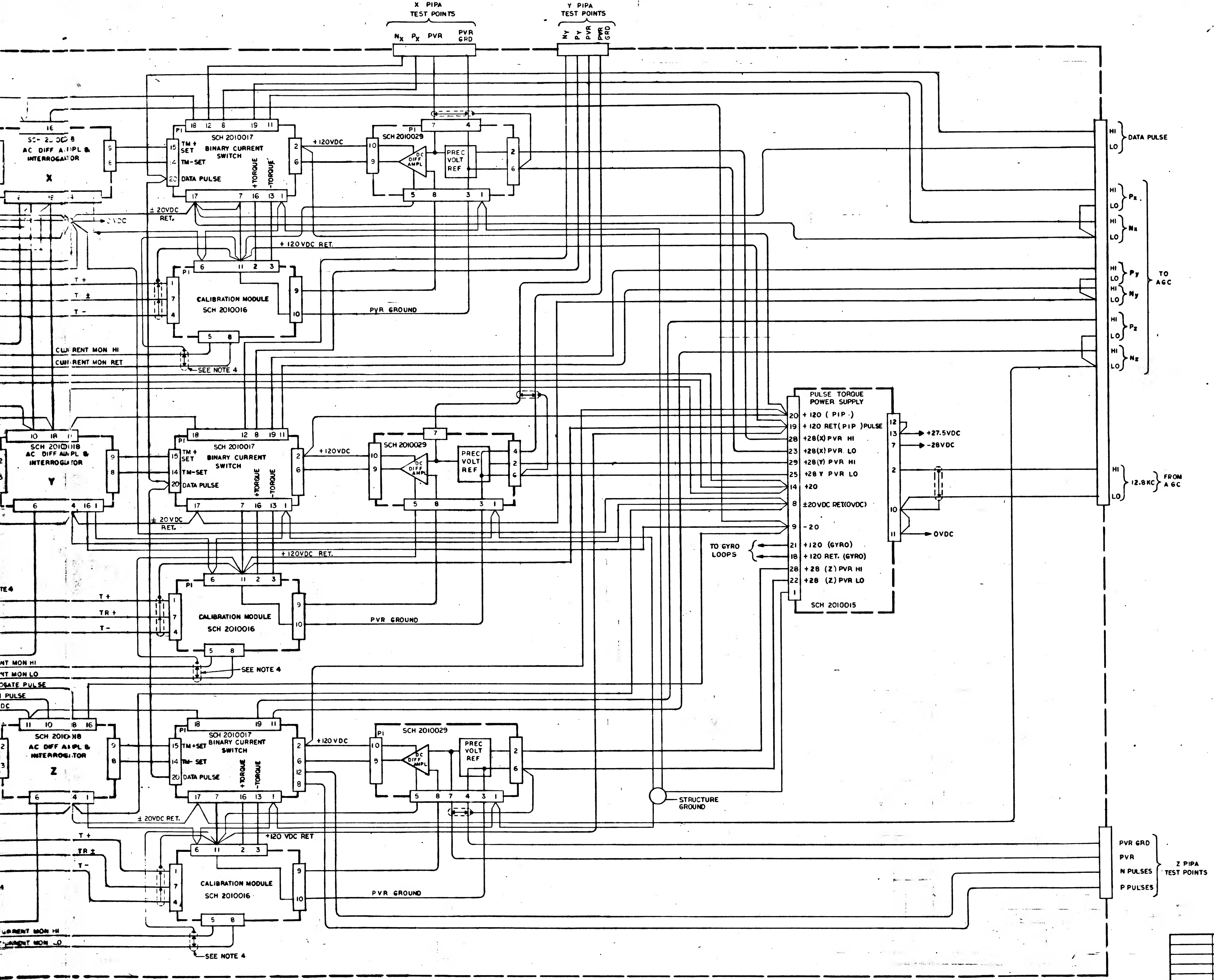
   AN INPUT SIG. HI IN PHASE WITH THE REF. EXC APPLIED TO THE AC AMPLIFIER / INTERROGATOR, WILL RESULT IN A TM + SET PULSE BEING APPLIED TO THE CURRENT SWITCH. THE TM + SET PULSE APPLIED TO THE CURRENT SWITCH WILL RESULT IN POS CURRENT (+TORQUE) OUTPUT AND "N" PULSES.
4. ALL NOTED WIRES FROM CAL MODULE TO X,Y,Z PIP ASSY TO BE MICRODOT TYPE NO. 2-3938
5. INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY MIL-D-70327

F-1

SYM	REVISIONS DESCRIPTION	DATE	APPROVAL



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NASA APPROVAL W J Robie 12-8-64
MIT APPROVAL

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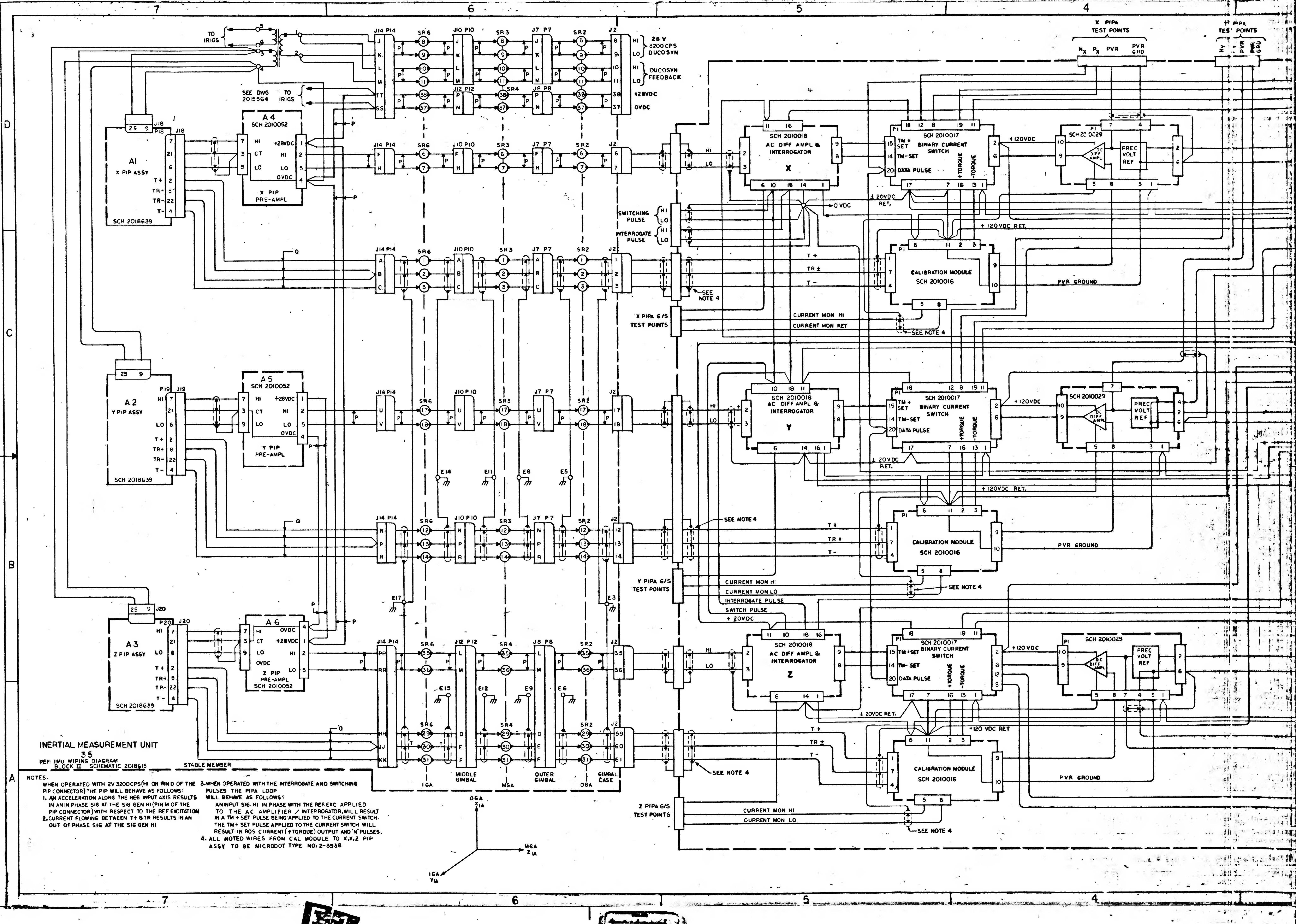
TWO WIRE MECHANIZATION OF APOLLO PIPA LOOPS

CODE IDENT NO. —
SIZE J
NASA DRAWING NO. 2015563
SCALE —
WT —
SHEET OF

MASTER



INERTIAL MEASUREMENT UNIT

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REF: IMU WIRING DIAGRAM
BLOCK II SCHEMATIC 2018615

NOTES:

WHEN OPERATED WITH 2V 3200CPS(HI ON PIN D OF THE PIP CONNECTOR) THE PIP WILL BEHAVE AS FOLLOWS:

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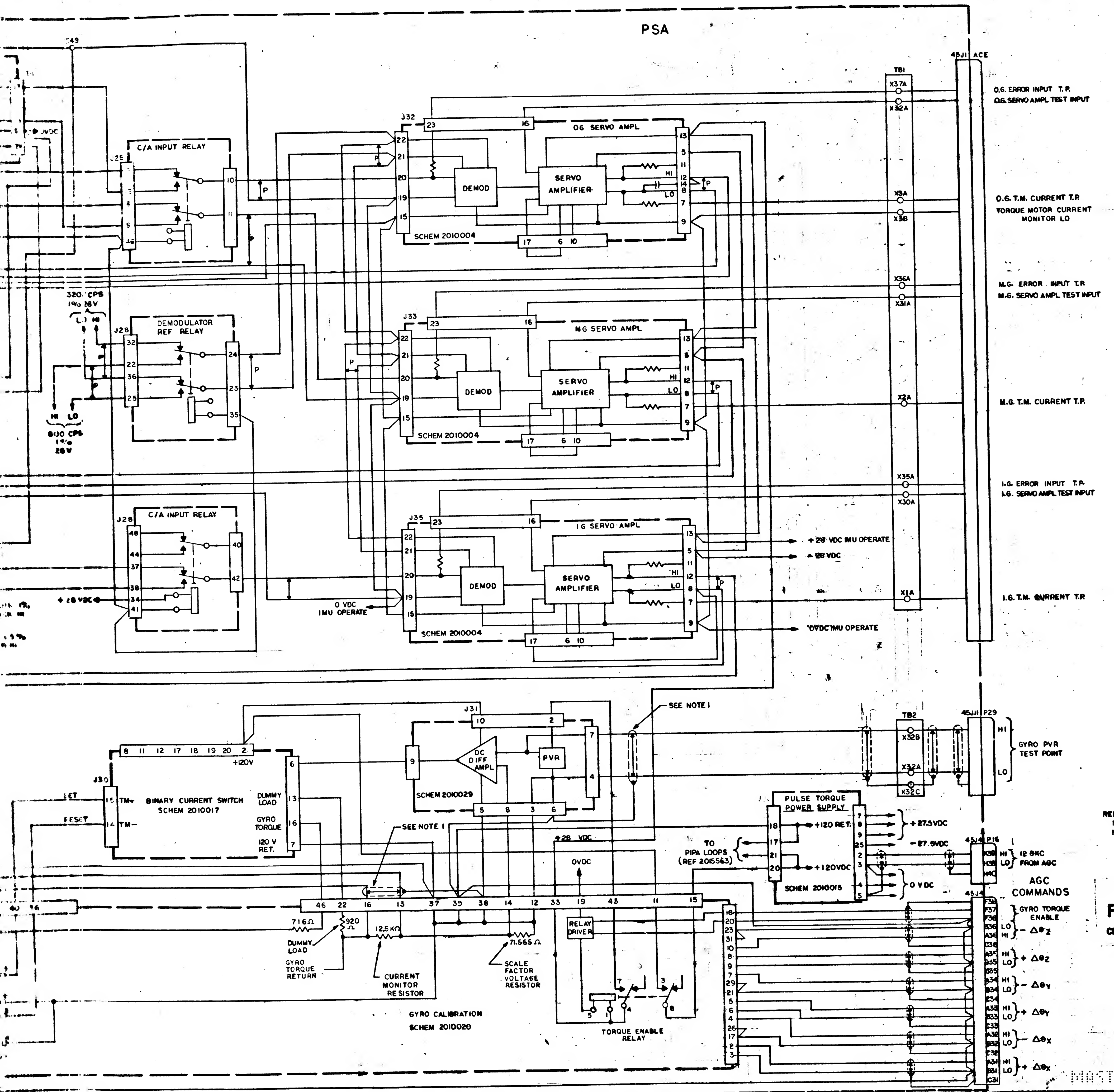

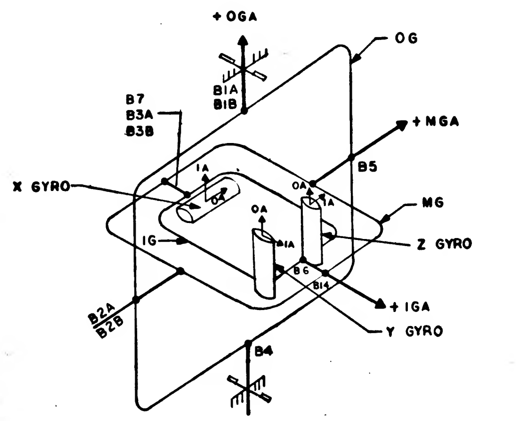

INERTIAL COMPONENT MECHANICAL SCHEM

REF:
INTERCONNECT LIST FOR PSA HEADER, DWG NO. 2014679

FOR INFORMATION ONLY

CLASS B RELEASE TDR No. 15947 DATE

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL
A	REVISED PER TDRR 22301	9-21-65	

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APPROVAL 1/26/65
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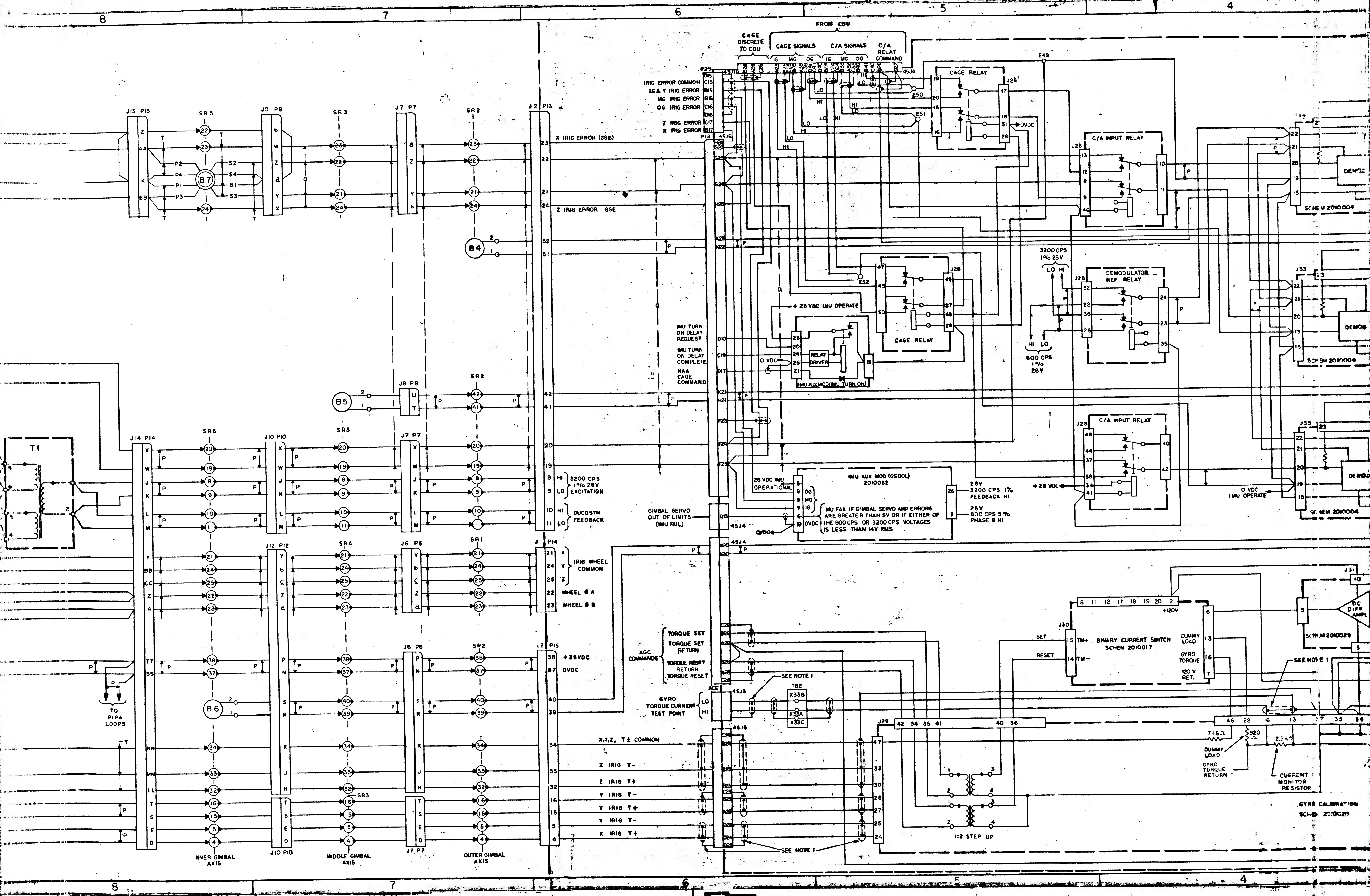
TWO WIRE MECHANIZATION
OF APOLLO STABILIZATION
LOOPS

CODE IDENT NO. 80230
SIZE J
NASA DRAWING NO. 2015564
SCALE
WT
SHEET 1 OF 1

2015564


8
7
6
5
4
FROM CDU
CAGE DISCRETE TO CDU
CAGE SIGNALS
C/A SIGNALS
C/A RELAY COMMAND
IG MG OG
IG MG OG
P29
45J4
E49
CAGE RELAY
J28
OVDC
E50
E51
IRIG ERROR COMMON
IG & Y IRIG ERROR
MG IRIG ERROR
OG IRIG ERROR
Z IRIG ERROR
X IRIG ERROR
P18
45J6
J13 P13
SR 5
J9 P9
SR 3
J7 P7
SR 2
J2 P13
B7
B4
X IRIG ERROR (GSE)
Z IRIG ERROR GSE
C/A INPUT RELAY
DEMOD
SCHEM 2010004
3200 CPS 1% 28 V
LO HI
DEMODULATOR REF RELAY
800 CPS 1% 28V
J33
J35
E52
+ 28 VDC IMU OPERATE
CAGE RELAY
IMU TURN ON DELAY REQUEST
IMU TURN ON DELAY COMPLETE
NAA CAGE COMMAND
0 VDC
RELAY DRIVER
IMU AUX MOD (IMU TURN ON)
B5
J8 P8
SR2
T1
J14 P14
SR6
J10 P10
SR3
J7 P7
3200 CPS 1% 28V EXCITATION
DUCOSYN FEEDBACK
28 VDC IMU OPERATIONAL
IMU AUX MOD (G500L) 2010082
IMU FAIL IF GIMBAL SERVO AMP ERRORS ARE GREATER THAN 5V OR IF EITHER OF THE 800 CPS OR 3200 CPS VOLTAGES IS LESS THAN 14V RMS
28V 3200 CPS 1% FEEDBACK HI
25V 800 CPS 5% PHASE B HI
+28 VDC
0 VDC IMU OPERATE
GIMBAL SERVO OUT OF LIMITS (IMU FAIL)
J12 P12
SR4
J6 P6
SR1
J1 P14
IRIG WHEEL COMMON
WHEEL φ A
WHEEL φ B
J8 P8
SR2
J2 P15
+28VDC
OVDC
B6
TO PIPA LOOPS
AGC COMMANDS
TORQUE SET
TORQUE SET RETURN
TORQUE RESET RETURN
TORQUE RESET
GYRO TORQUE CURRENT TEST POINT
SEE NOTE 1
TB2
X33B
X33A
X33C
45J3
J30
SET
RESET
BINARY CURRENT SWITCH SCHEM 2010017
+120V
DUMMY LOAD
GYRO TORQUE
120 V RET.
J31
DC DIFF AMPL
SCHEM 2010029
SEE NOTE 1
X,Y,Z, T± COMMON
Z IRIG T-
Z IRIG T+
Y IRIG T-
Y IRIG T+
X IRIG T-
X IRIG T+
J29
1:2 STEP UP
716Ω
920 Ω
12.5 kΩ
DUMMY LOAD
GYRO TORQUE RETURN
CURRENT MONITOR RESISTOR
GYRO CALIBRATION SCHEM 2010029
INNER GIMBAL AXIS
J10 P10
MIDDLE GIMBAL AXIS
J7 P7
OUTER GIMBAL AXIS
SEE NOTE 1

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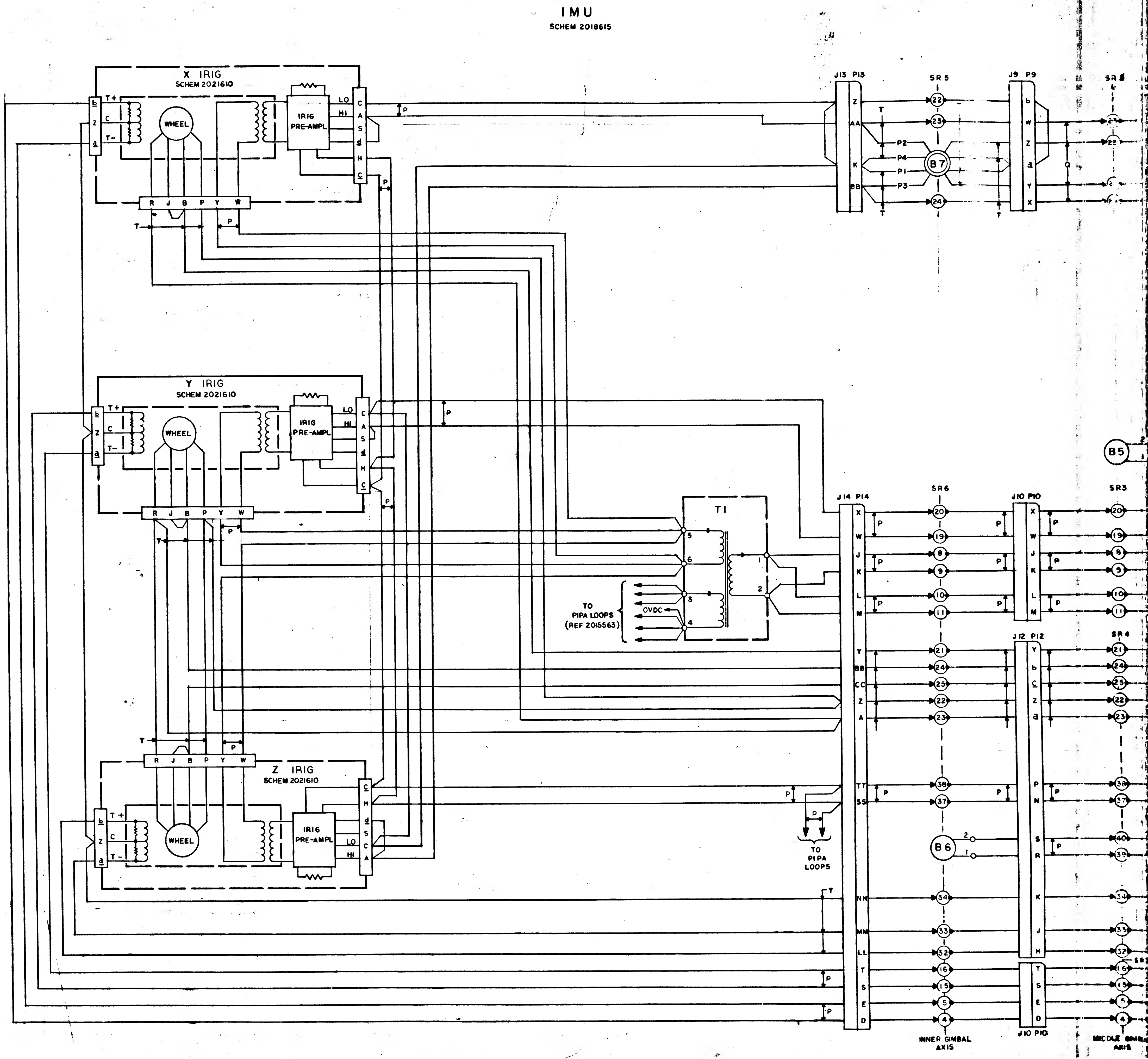

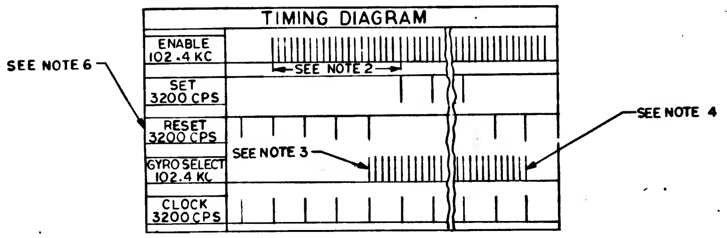

NOTES:

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5. ALL INPUTS FROM THE COMPUTER ARE TO BE TWISTED SHIELDED PAIRS
6. CURRENT SWITCH MUST BE IN RESET CONDITION PRIOR TO RECEIVING GYRO TORQUE ENABLE SIGNAL FROM THE COMPUTER
7. A POSITIVE AGC TORQUE COMMAND (+Δθ) SIGNAL PRODUCES TORQUE IN THE TM-WINDING OF THE GYRO RESULTING IN A POSITIVE ROTATION ABOUT THE GYRO INPUT AXIS
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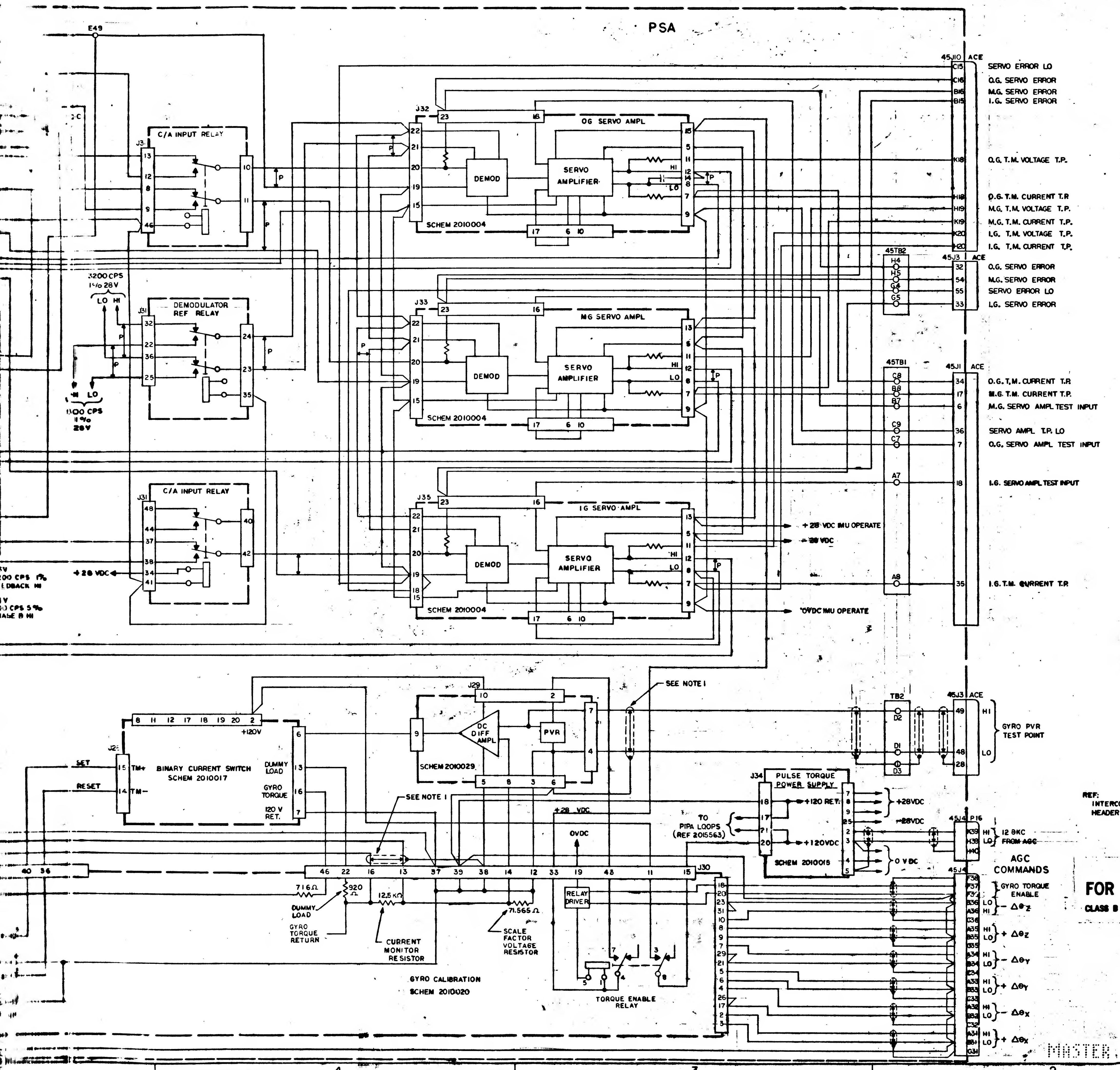
9. ERROR SIGNAL IN PHASE WITH DEMODULATOR REFERENCE RESULTS IN A POSITIVE TORQUE MOTOR VOLTAGE
10. INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY MIL-D-70327.

SYM	DESCRIPTION	DATE	APPROVAL
	REVISIONS 15947		
A	REVISED PER TDRR 22301	9-21-65	
B	REVISED PER TDRR 29126		



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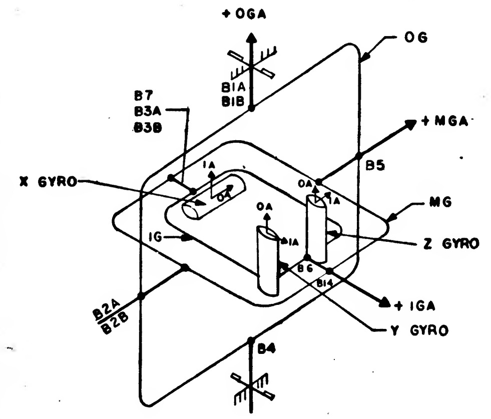


INERTIAL COMPONENT MECHANICAL SCHEM

FOR INFORMATION ONLY

CLASS B RELEASE TDR No. 15947 DATE

QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	FIND NO

LIST OF MATERIALS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS ± DECIMALS ± ANGLES ±
DO NOT SCALE THIS DRAWING
MATERIAL
HEAT TREATMENT
FINAL FINISH

NEXT ASSY | USED ON
APPLICATION

MIT
INSTRUMENTATION LAB
CAMBRIDGE, MASS

DRAWN A. D. Bo DATE
CHECKED 1-20-65
APPROVAL 1/25/65
APPROVAL N. Kramer 1/26/65
NASA APPROVAL
MIT APPROVAL

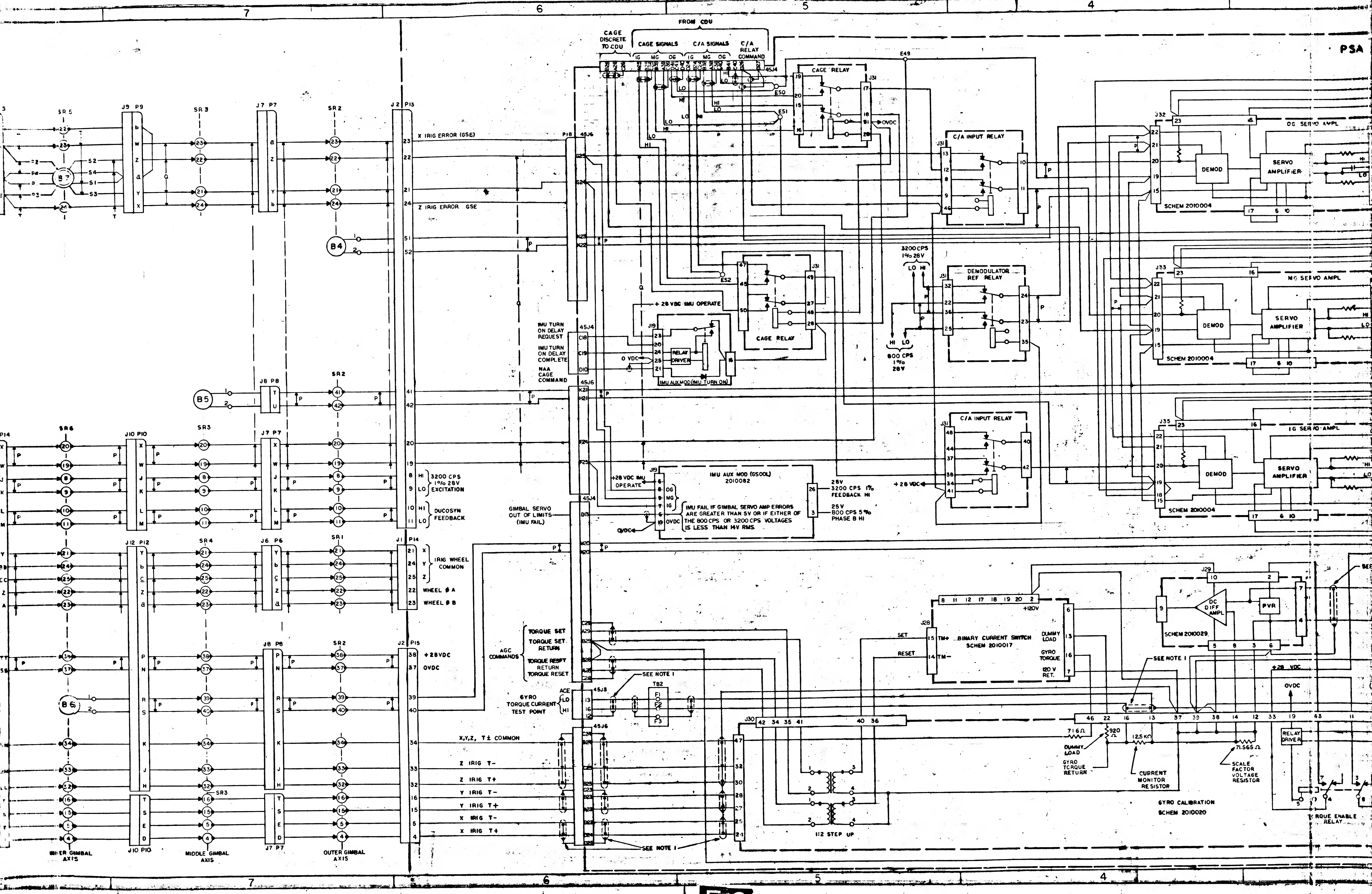
MANNED SPACECRAFT CENTER
HOUSTON, TEXAS

TWO WIRE MECHANIZATION OF APOLLO STABILIZATION LOOPS

CODE IDENT NO. 80230
SIZE J
NASA DRAWING NO. 2015564
SCALE —
WT —
SHEET 1 OF 1

MASTER

2015564 B


7
6
5
4
PSA
FROM CDU
CAGE DISCRETE TO CDU
CAGE SIGNALS
C/A SIGNALS
C/A RELAY COMMAND
IG MG OG
45J4
E49
E50
E51
E52
CAGE RELAY
J31
OVDC
C/A INPUT RELAY
J32
OG SERVO AMPL
DEMOD
SERVO AMPLIFIER
SCHEM 2010004
HI
LO
SR5
SR3
SR2
SR6
SR4
SR1
J9 P9
J7 P7
J2 P13
J8 P8
J10 P10
J12 P12
J6 P6
J1 P14
J2 P15
P14
B4
B5
B6
X IRIG ERROR (GSE)
Z IRIG ERROR GSE
P18 45J6
+ 28 VDC IMU OPERATE
J19
RELAY DRIVER
IMU AUXMOD(IMU TURN ON)
IMU TURN ON DELAY REQUEST
IMU TURN ON DELAY COMPLETE
NAA CAGE COMMAND
3200 CPS 1% 28V
DEMODULATOR REF RELAY
800 CPS 1% 28V
J33
MG SERVO AMPL
J35
IG SERVO AMPL
3200 CPS 1% 28V EXCITATION
DUCOSYN FEEDBACK
+28 VDC IMU OPERATE
IMU AUX MOD (GSOOL) 2010082
IMU FAIL IF GIMBAL SERVO AMP ERRORS ARE GREATER THAN 5V OR IF EITHER OF THE 800 CPS OR 3200 CPS VOLTAGES IS LESS THAN 14V RMS
28V 3200 CPS 1% FEEDBACK HI
25V 800 CPS 5% PHASE B HI
+28 VDC
GIMBAL SERVO OUT OF LIMITS (IMU FAIL)
OVDC
IRIG WHEEL COMMON
WHEEL ϕ A
WHEEL ϕ B
+28VDC
OVDC
AGC COMMANDS
TORQUE SET
TORQUE SET RETURN
TORQUE RESET RETURN
TORQUE RESET
45J3
GYRO TORQUE CURRENT TEST POINT
ACE LO HI
SEE NOTE 1
TB2
F1 F2 F3
X,Y,Z, T± COMMON
Z IRIG T-
Z IRIG T+
Y IRIG T-
Y IRIG T+
X IRIG T-
X IRIG T+
J30
1:2 STEP UP
J28
SET
RESET
TM+ TM-
BINARY CURRENT SWITCH SCHEM 2010017
+120V
DUMMY LOAD
GYRO TORQUE
120 V RET.
J29
DC DIFF AMPL
PVR
SCHEM 2010029
716 Ω
920 Ω
12.5 KΩ
71.565 Ω
DUMMY LOAD
GYRO TORQUE RETURN
CURRENT MONITOR RESISTOR
SCALE FACTOR VOLTAGE RESISTOR
RELAY DRIVER
GYRO CALIBRATION SCHEM 2010020
TORQUE ENABLE RELAY
INNER GIMBAL AXIS
MIDDLE GIMBAL AXIS
OUTER GIMBAL AXIS
J10 P10
J7 P7

F-2

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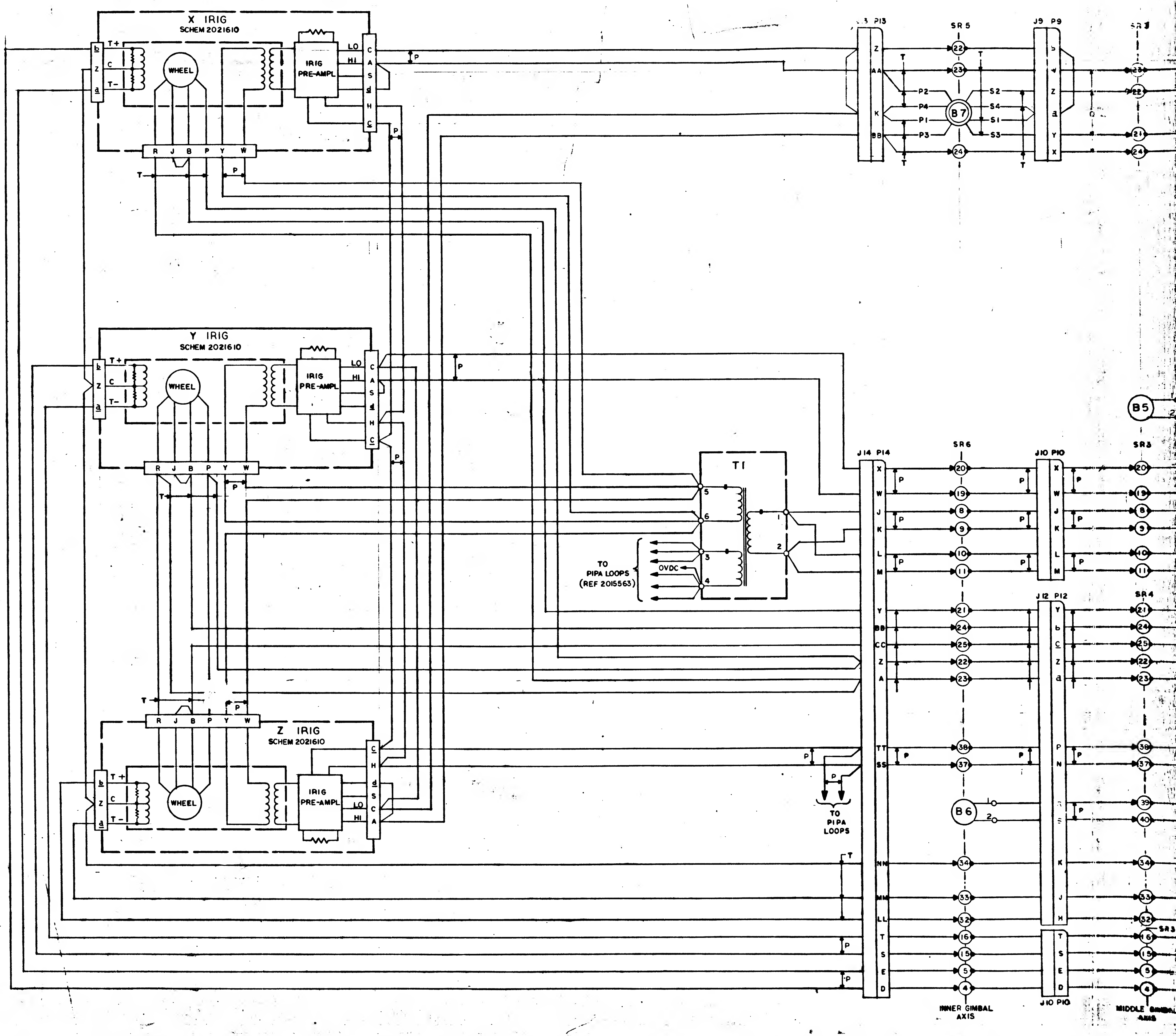
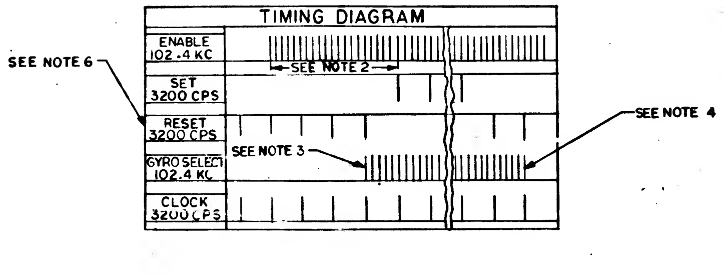
IMU

SCHEM 2018615





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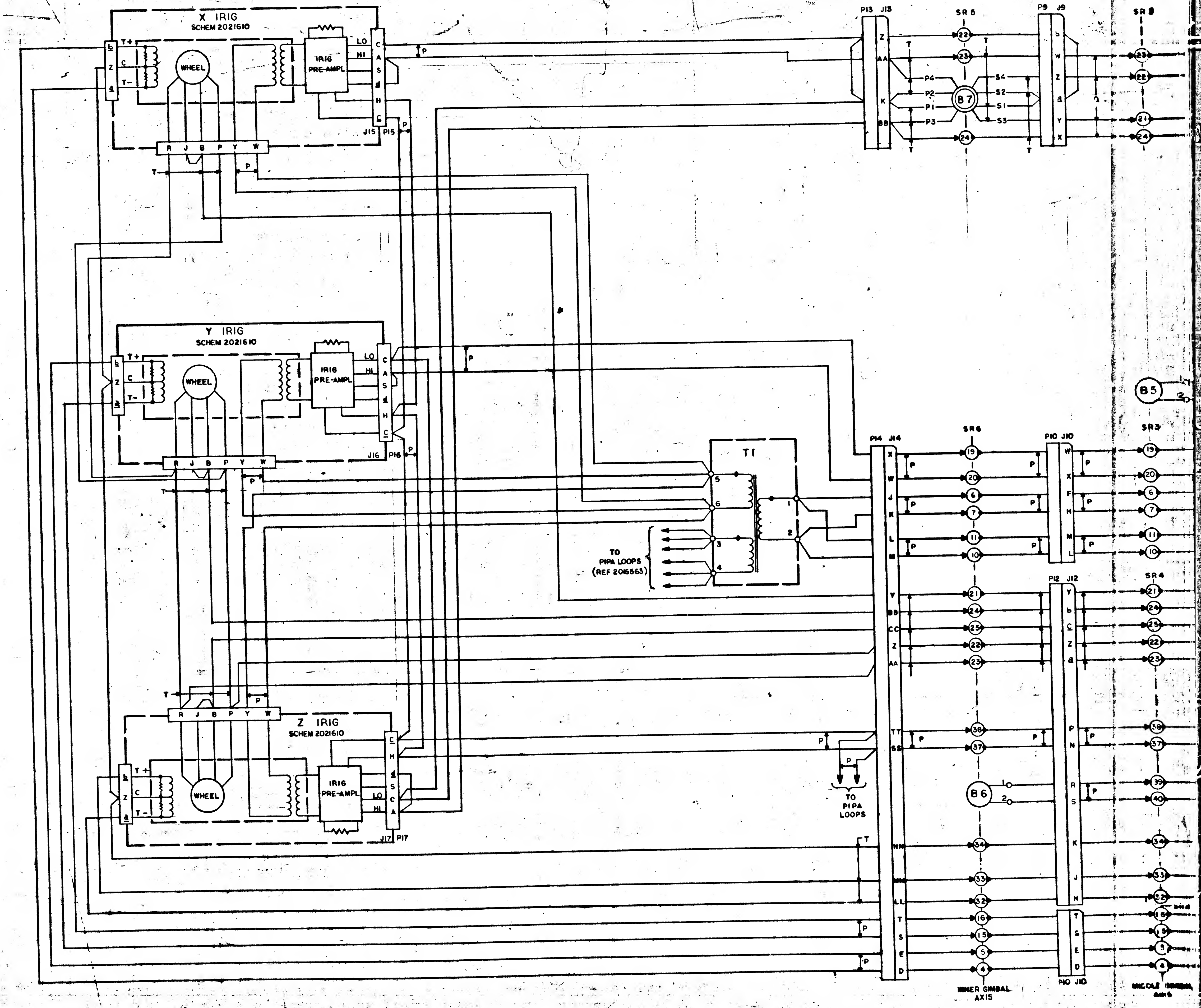
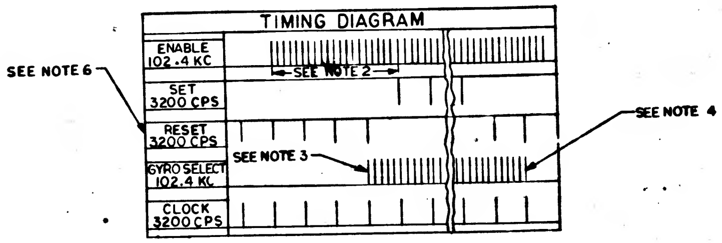
10. INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY MIL-D-70327.

IMU
SCHEM 2018615





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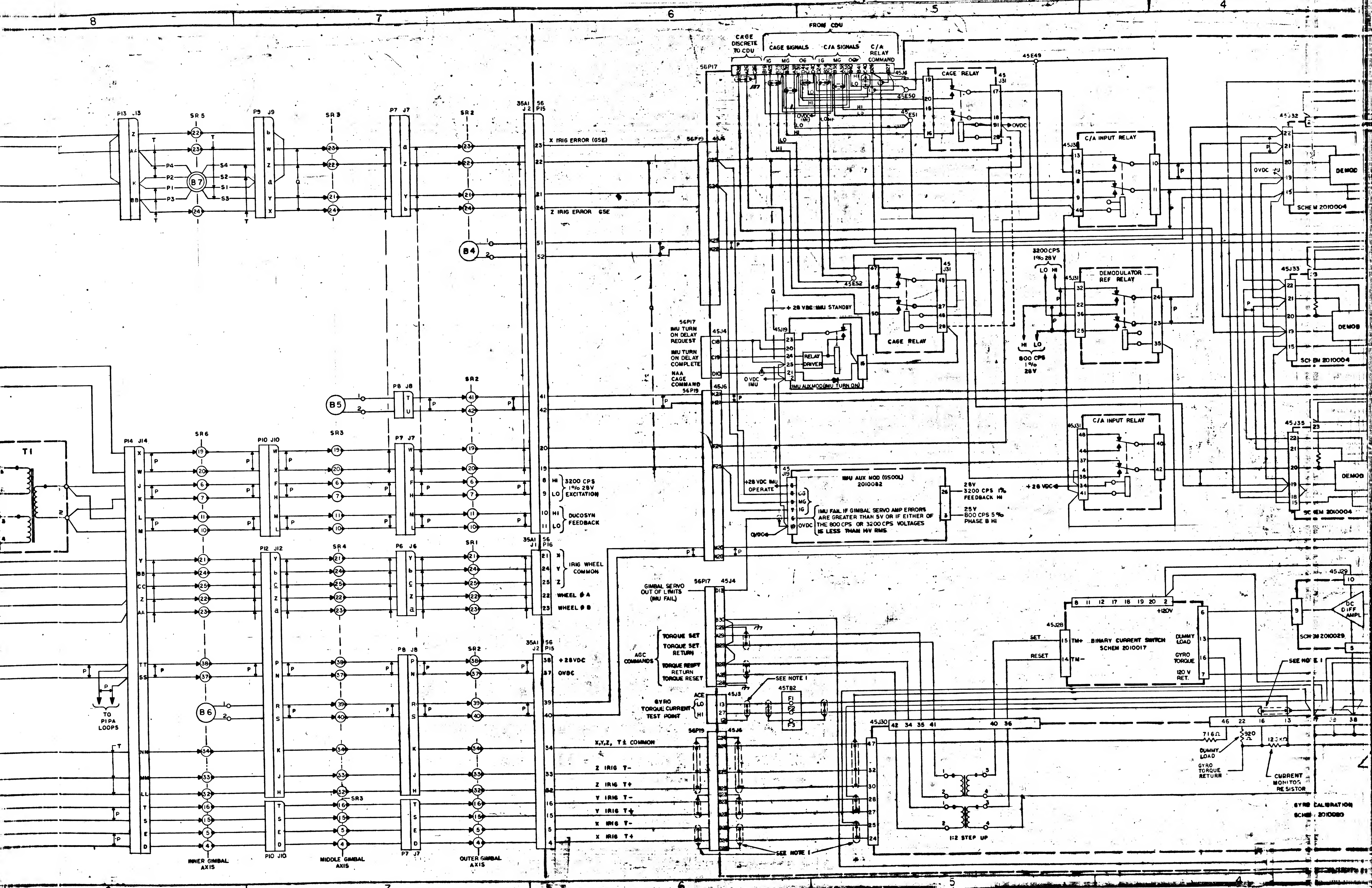
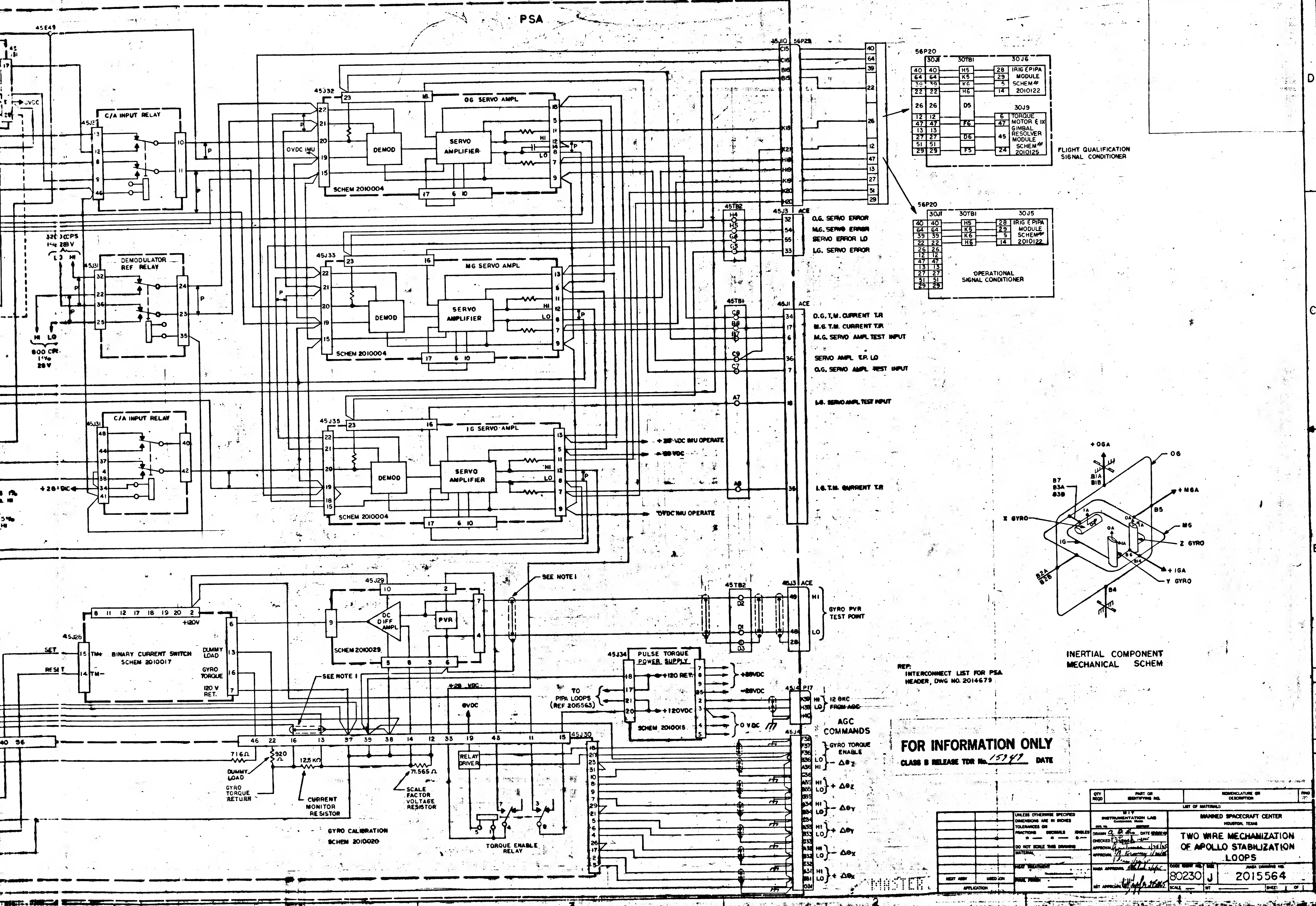

8
7
6
5
4
FROM CDU
CAGE DISCRETE TO CDU
CAGE SIGNALS
C/A SIGNALS
C/A RELAY COMMAND
IG MG OG
IG MG OG
56P17
45J4
45E50
45E51
45E49
CAGE RELAY
45 J31
OVDC
C/A INPUT RELAY
45J30
45J32
DEMOD
SCHEM 2010004
P13 J13
SR 5
P9 J9
SR 3
P7 J7
SR 2
35A1 J2
56 P15
B7
P4
P2
P1
P3
S4
S2
S1
S3
X IRIG ERROR (GSE)
Z IRIG ERROR GSE
56P19
45J6
B4
45E52
CAGE RELAY
3200 CPS 1% 28V
LO HI
DEMODULATOR REF RELAY
45J33
HI LO
800 CPS 1% 28V
+28 VDC IMU STANDBY
56P17
IMU TURN ON DELAY REQUEST
IMU TURN ON DELAY COMPLETE
NAA CAGE COMMAND
45J4
45J19
RELAY DRIVER
OVDC IMU
IMU AUX MOD (IMU TURN ON)
B5
P8 J8
SR2
T1
P14 J14
SR6
P10 J10
SR3
P7 J7
3200 CPS 1% 28V EXCITATION
DUCOSYN FEEDBACK
C/A INPUT RELAY
45J35
+28 VDC IMU OPERATE
IMU AUX MOD (GS00L) 2010082
IMU FAIL IF GIMBAL SERVO AMP ERRORS ARE GREATER THAN 5V OR IF EITHER OF THE 800 CPS OR 3200 CPS VOLTAGES IS LESS THAN 14V RMS
28V 3200 CPS 1% FEEDBACK HI
25V 800 CPS 5% PHASE B HI
+28 VDC
P12 J12
SR4
P6 J6
SR1
35A1 J1
56 P16
IRIG WHEEL COMMON
WHEEL φ A
WHEEL φ B
GIMBAL SERVO OUT OF LIMITS (IMU FAIL)
56P17
45J4
45J29
DC DIFF AMPL
SCHEM 2010029
AGC COMMANDS
TORQUE SET
TORQUE SET RETURN
TORQUE RESET RETURN
TORQUE RESET
+120V
45J28
SET
RESET
TM+
TM−
BINARY CURRENT SWITCH SCHEM 2010017
DUMMY LOAD
GYRO TORQUE
120 V RET.
SEE NOTE 1
GYRO TORQUE CURRENT TEST POINT
ACE
LO
HI
45J3
45TB2
F1
F2
F3
P8 J8
SR2
35A1 J2
56 P15
+28VDC
OVDC
B6
TO PIPA LOOPS
45J30
X,Y,Z, T± COMMON
Z IRIG T−
Z IRIG T+
Y IRIG T−
Y IRIG T+
X IRIG T−
X IRIG T+
SEE NOTE 1
1:2 STEP UP
716Ω
920 Ω
12.5KΩ
DUMMY LOAD
GYRO TORQUE RETURN
CURRENT MONITOR RESISTOR
GYRO CALIBRATION SCHEM 2010080
INNER GIMBAL AXIS
P10 J10
MIDDLE GIMBAL AXIS
P7 J7
OUTER GIMBAL AXIS
SR3

SYM	DESCRIPTION	DATE	APPROVAL
	REVISIONS	15947	
A	REVISED PER TDRR 22301	9-21-65	[illegible]
B	REVISED PER TDRR 29126	5-24-66	[illegible]
C	REVISED PER TDRR 30664	[illegible]	[illegible]



REF:
INTERCONNECT LIST FOR PSA
HEADER, DWG NO. 2014679

FOR INFORMATION ONLY
CLASS B RELEASE TDR No. 15947 DATE

QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	FIND NO.
	LIST OF MATERIAL		

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS ± — DECIMALS ± — ANGLES ± —
DO NOT SCALE THIS DRAWING
MATERIAL —
HEAT TREATMENT —
FINAL FINISH —

MIT
INSTRUMENTATION LAB
CAMBRIDGE, MASS.
DRAWN A. B. [illegible] DATE [illegible]
CHECKED [illegible] 1-2-65
APPROVAL [illegible] 1/25/65
APPROVAL N. [illegible] 1/26/65
[illegible] 1/26/65
NASA APPROVAL [illegible]
MIT APPROVAL [illegible] 2-5-65

MANNED SPACECRAFT CENTER
HOUSTON, TEXAS

TWO WIRE MECHANIZATION
OF APOLLO STABILIZATION
LOOPS

CODE IDENT NO.	SIZE	NASA DRAWING NO.
80230	J	2015564

SCALE — WT — SHEET 1 OF 1

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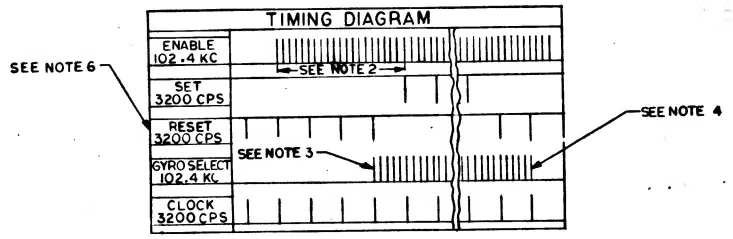

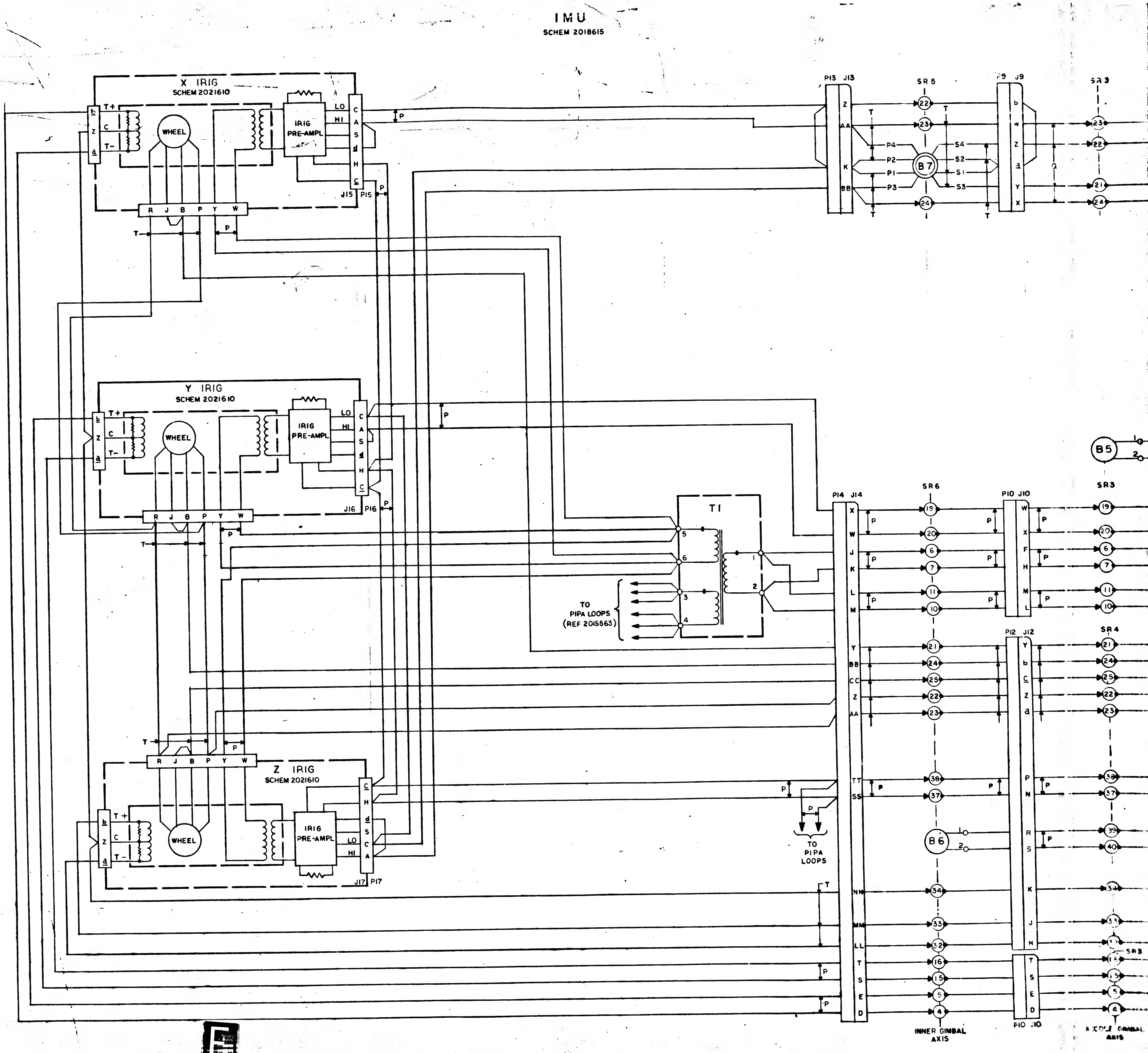

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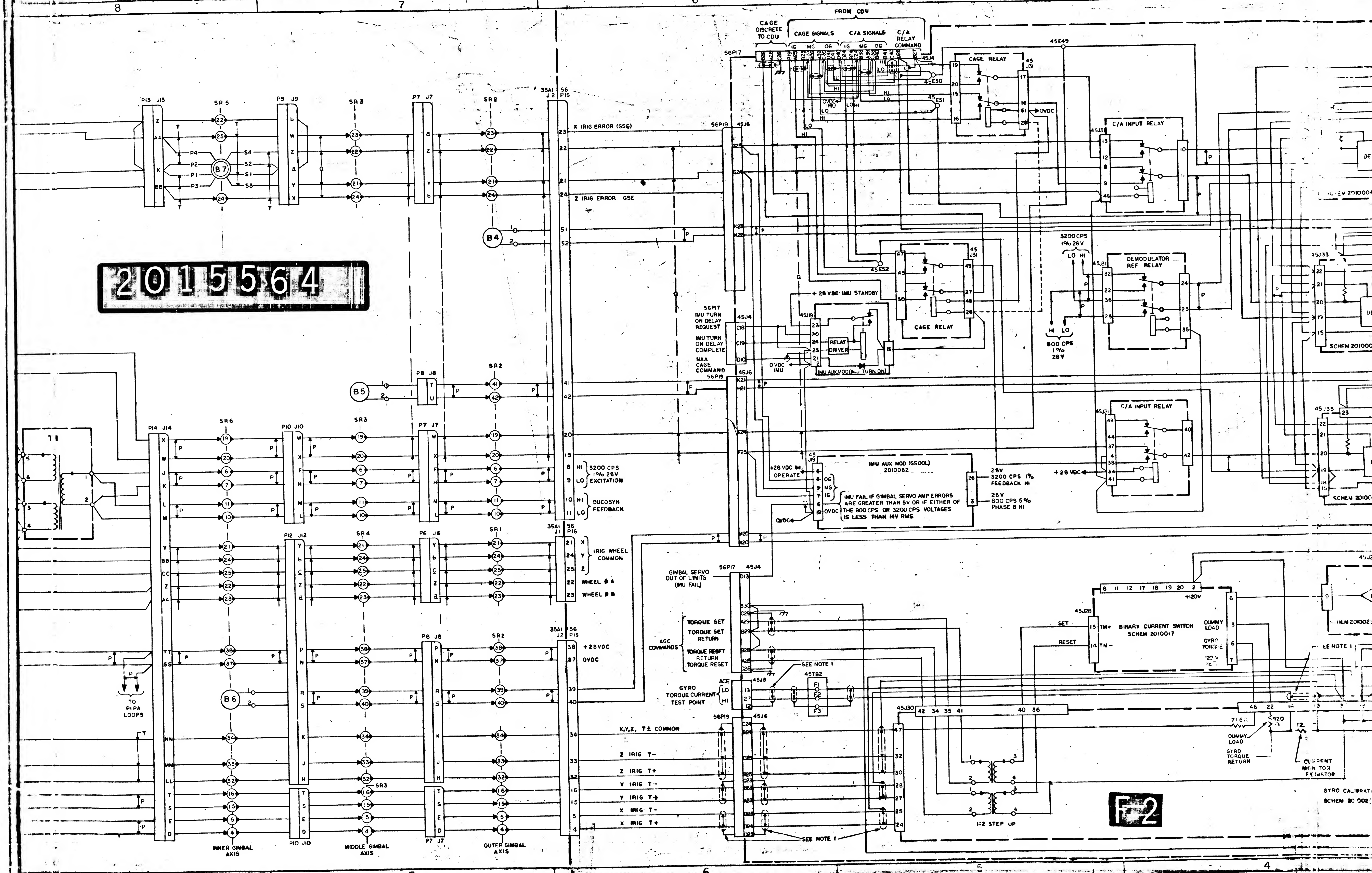
10. INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY MIL-D-70327.

2015564

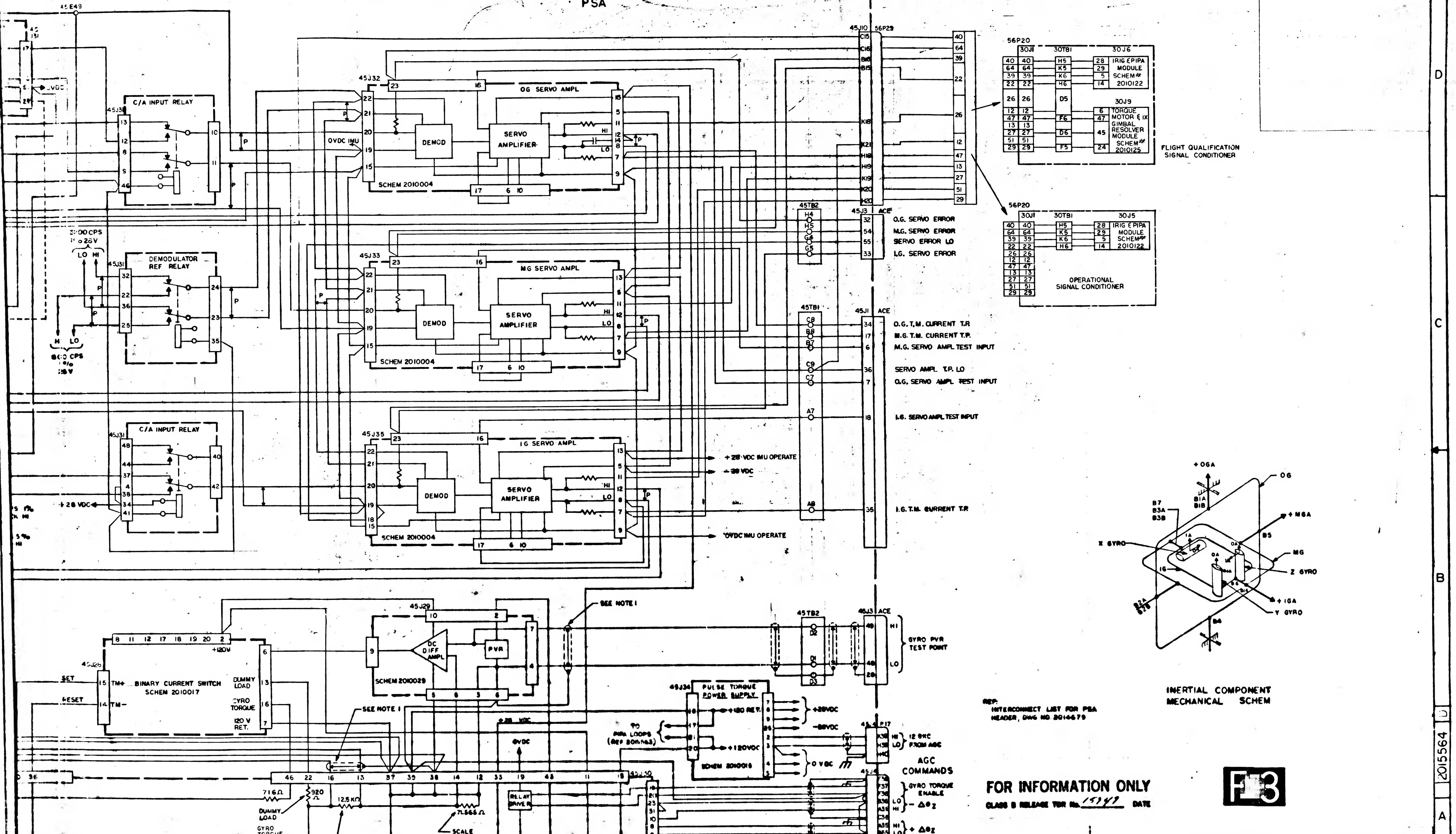
F

2015564


8
7
6
5
4
FROM CDU
CAGE DISCRETE TO CDU
CAGE SIGNALS
C/A SIGNALS
C/A RELAY COMMAND
IG MG OG
56P17
45J4
45E49
45E50
45E51
45E52
CAGE RELAY
C/A INPUT RELAY
OVDC
OVDC IMU
HI LO
P13 J13
SR5
B7
P9 J9
SR3
P7 J7
SR2
35A1 J2
56 P15
X IRIG ERROR (GSE)
Z IRIG ERROR GSE
B4
56P19
45J6
SCHEM 2010004
3200 CPS 1% 26 V
DEMODULATOR REF RELAY
800 CPS 1% 28V
45J31
45J33
SCHEM 201000
+ 28 VDC IMU STANDBY
IMU TURN ON DELAY REQUEST
IMU TURN ON DELAY COMPLETE
NAA CAGE COMMAND
45J19
RELAY DRIVER
IMU AUX MOD (IMU TURN ON)
B5
P8 J8
SR2
T1
P14 J14
SR6
P10 J10
SR3
3200 CPS 1% 28V EXCITATION
DUCOSYN FEEDBACK
+28 VDC IMU OPERATE
IMU AUX MOD (G500L) 2010082
IMU FAIL IF GIMBAL SERVO AMP ERRORS ARE GREATER THAN 5V OR IF EITHER OF THE 800 CPS OR 3200 CPS VOLTAGES IS LESS THAN 14V RMS
28V 3200 CPS 1% FEEDBACK HI
25V 800 CPS 5% PHASE B HI
+ 28 VDC
45J35
SCHEM 20100
P12 J12
SR4
P6 J6
SR1
35A1 J1
56 P16
IRIG WHEEL COMMON
WHEEL Ø A
WHEEL Ø B
GIMBAL SERVO OUT OF LIMITS (IMU FAIL)
AGC COMMANDS
TORQUE SET
TORQUE SET RETURN
TORQUE RESET
TORQUE RESET RETURN
SEE NOTE 1
45TB2
GYRO TORQUE CURRENT TEST POINT
ACE
45J3
45J28
SET
RESET
BINARY CURRENT SWITCH SCHEM 2010017
+120V
DUMMY LOAD
GYRO TORQUE
120 V RET
SCHEM 2010023
SEE NOTE 1
TO PIPA LOOPS
B6
+28VDC
OVDC
X,Y,Z, T± COMMON
Z IRIG T−
Z IRIG T+
Y IRIG T−
Y IRIG T+
X IRIG T−
X IRIG T+
45J30
1:2 STEP UP
716Ω
920Ω
12Ω
DUMMY LOAD
GYRO TORQUE RETURN
CURRENT MONITOR RESISTOR
GYRO CALIBRATI
SCHEM 20 002
INNER GIMBAL AXIS
MIDDLE GIMBAL AXIS
OUTER GIMBAL AXIS
SEE NOTE 1

F-2

SYM	DESCRIPTION	DATE	APPROVAL
A	REVISED PER TDRR 22301	9-21-65	
B	REVISED PER TDRR 29126		
C	REVISED PER TDRR 30664		
D	REVISED PER TDRR 33298	3/13/67	



REF:
INTERCONNECT LIST FOR PSA
HEADER, DWG NO 2014679

FOR INFORMATION ONLY
CLASS B RELEASE TDR No. 15949 DATE

F3

MASTER

QTY REQ	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	FIND NO

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
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FINAL FINISH
NEXT ASSY USED ON
APPLICATION

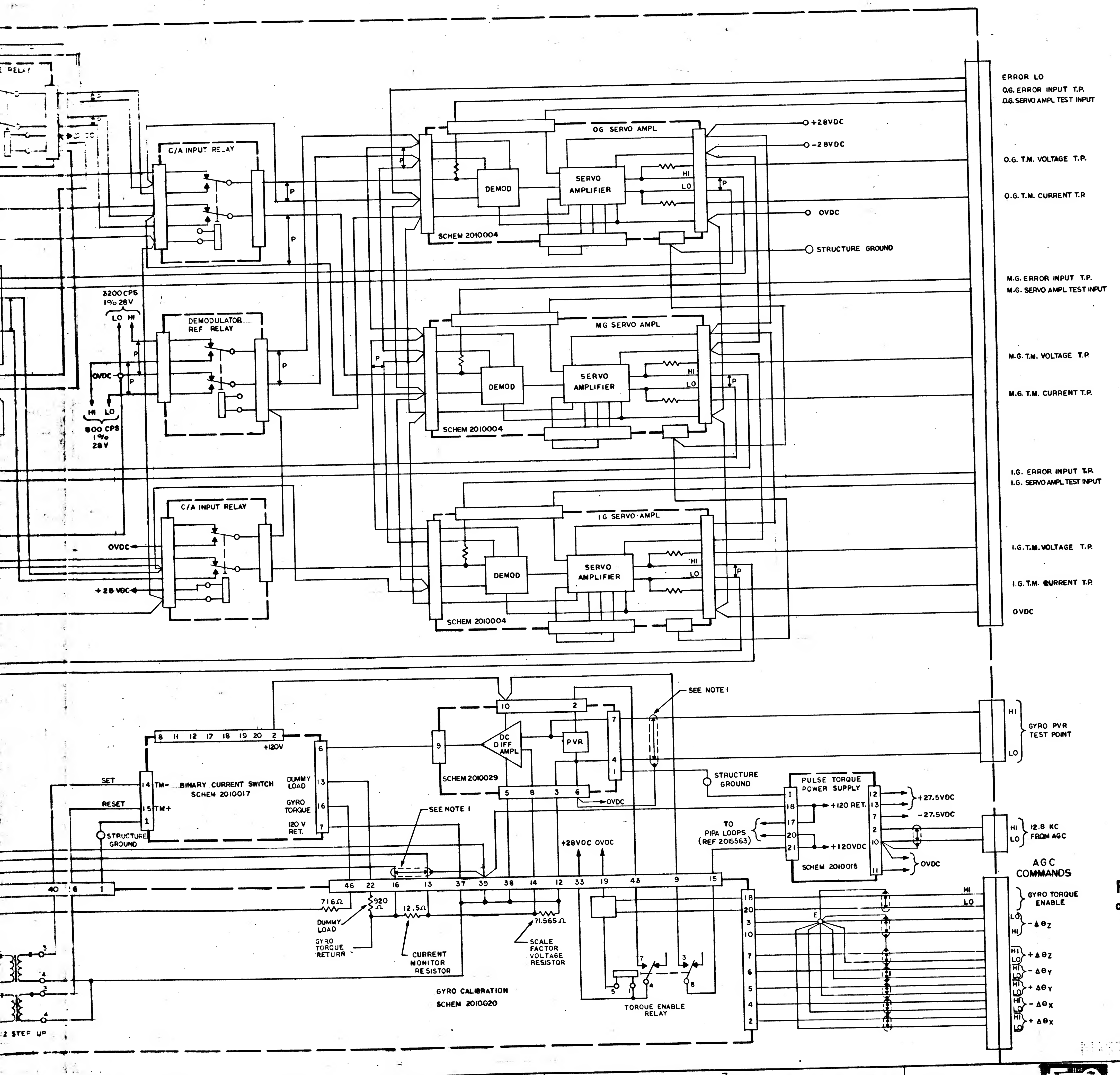
MIT INSTRUMENTATION LAB
DRAWN DATE
CHECKED
APPROVAL 1/26/65
APPROVAL
NASA APPROVAL
MIT APPROVAL

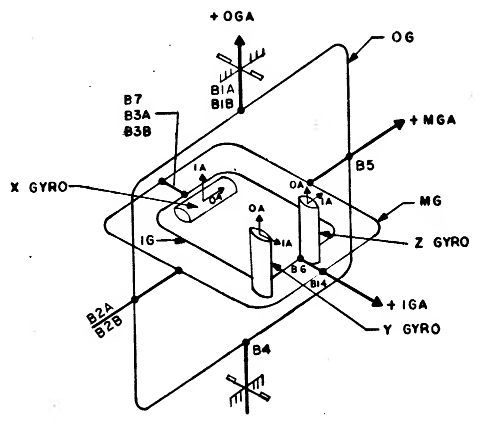
MANNED SPACECRAFT CENTER
HOUSTON, TEXAS

TWO WIRE MECHANIZATION
OF APOLLO STABILIZATION
LOOPS

CODE IDENT NO 80230 SIZE J NASA DRAWING NO. 2015564
SCALE — WT — SHEET 1 OF 1

2015564





INERTIAL COMPONENT MECHANICAL SCHEM

FOR INFORMATION ONLY

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS ± — DECIMALS ± — ANGLES ± —
DO NOT SCALE THIS DRAWING
MATERIAL —
HEAT TREATMENT —
FINAL FINISH —

MIT
INSTRUMENTATION LAB
CAMBRIDGE, MASS

DRAWN A. D. [illegible] DATE [illegible]
CHECKED [illegible] -2965
APPROVAL [illegible] 1/25/65
APPROVAL N. Kramer 1/26/65
NASA APPROVAL [illegible]
MIT APPROVAL [illegible] 2 Feb 65

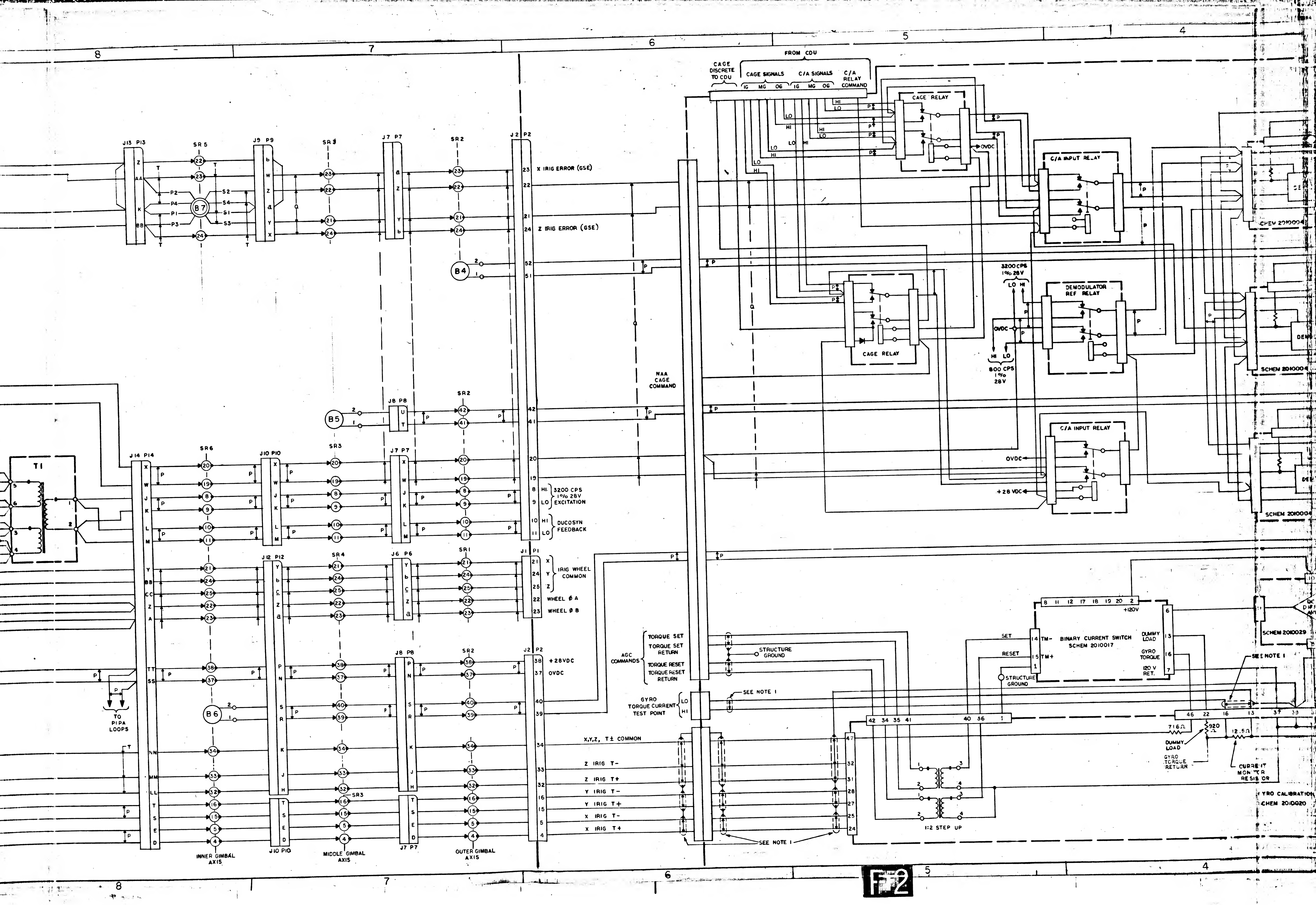
MANNED SPACECRAFT CENTER
HOUSTON, TEXAS

TWO WIRE MECHANIZATION
OF APOLLO STABILIZATION
LOOPS

CODE IDENT NO. —
SIZE J
NASA DRAWING NO. 2015564
SCALE — WT — SHEET 1 OF 1

2015564

REVISIONS
SYM DESCRIPTION DATE APPROVAL
15947



8
7
6
5
4
FROM CDU
CAGE DISCRETE TO CDU
CAGE SIGNALS
C/A SIGNALS
C/A RELAY COMMAND
IG MG OG
IG MG OG
CAGE RELAY
C/A INPUT RELAY
OVDC
CHEM 2010004
3200 CPS 1% 28V
LO HI
DEMODULATOR REF RELAY
CAGE RELAY
800 CPS 1% 28V
HI LO
SCHEM 2010004
NAA CAGE COMMAND
C/A INPUT RELAY
OVDC
+28 VDC
SCHEM 2010004
J13 P13
SR5
B7
J9 P9
SR3
J7 P7
SR2
J2 P2
X IRIG ERROR (GSE)
Z IRIG ERROR (GSE)
B4
J8 P8
B5
T1
J14 P14
SR6
J10 P10
3200 CPS 1% 28V EXCITATION
DUCOSYN FEEDBACK
J12 P12
SR4
J6 P6
SR1
J1 P1
IRIG WHEEL COMMON
WHEEL Ø A
WHEEL Ø B
+28VDC
OVDC
TO PIPA LOOPS
B6
INNER GIMBAL AXIS
J10 P10
MIDDLE GIMBAL AXIS
J7 P7
OUTER GIMBAL AXIS
AGC COMMANDS
TORQUE SET
TORQUE SET RETURN
TORQUE RESET
TORQUE RESET RETURN
STRUCTURE GROUND
GYRO TORQUE CURRENT TEST POINT
SEE NOTE 1
X,Y,Z, T± COMMON
Z IRIG T−
Z IRIG T+
Y IRIG T−
Y IRIG T+
X IRIG T−
X IRIG T+
SEE NOTE 1
1:2 STEP UP
BINARY CURRENT SWITCH SCHEM 2010017
SET
RESET
TM−
TM+
+120V
DUMMY LOAD
GYRO TORQUE
120 V RET.
STRUCTURE GROUND
SCHEM 2010029
SEE NOTE 1
716Ω
920 Ω
12.5Ω
DUMMY LOAD
GYRO TORQUE RETURN
CURRENT MONITOR RESISTOR
GYRO CALIBRATION SCHEM 2010020
F2

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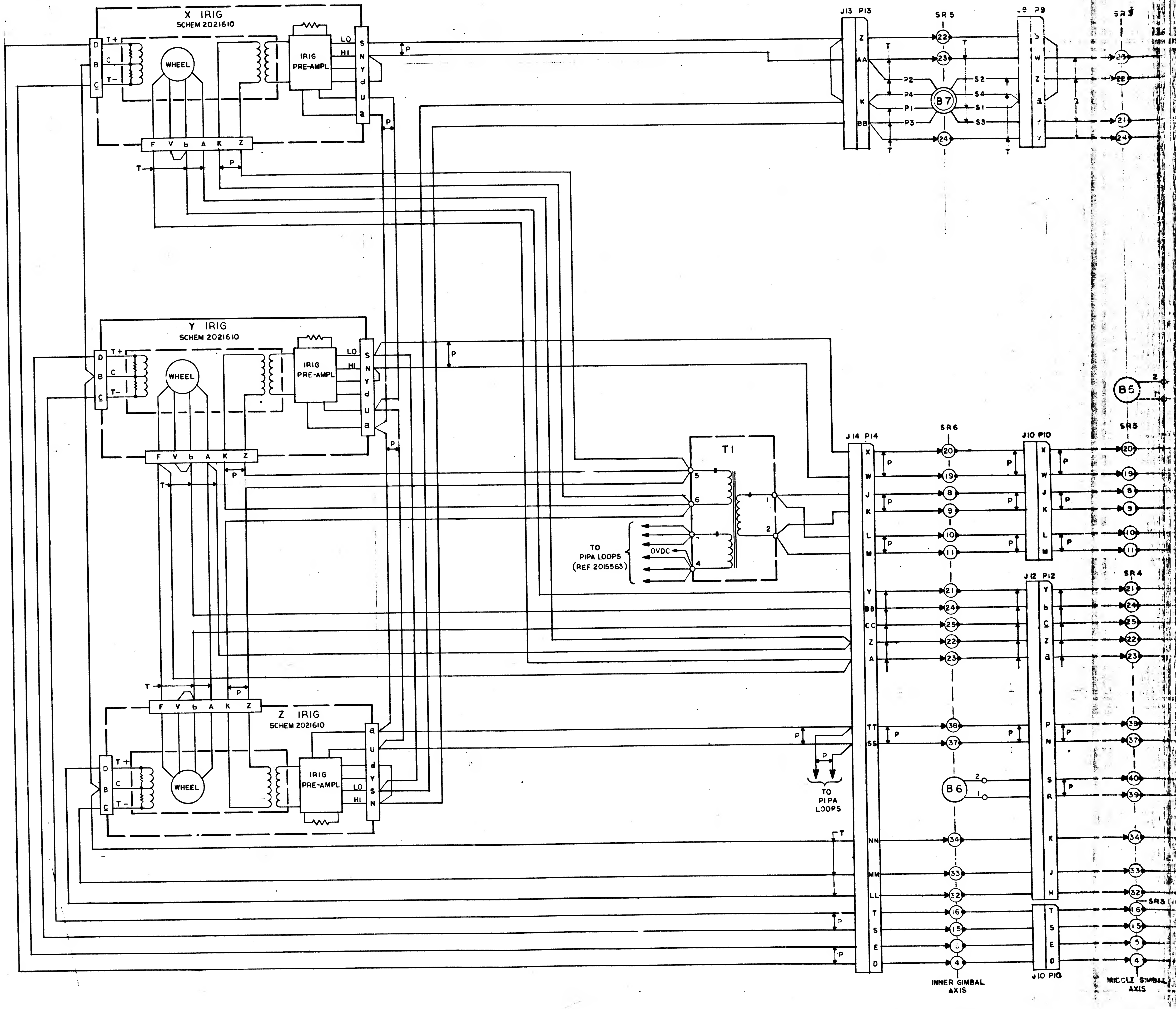
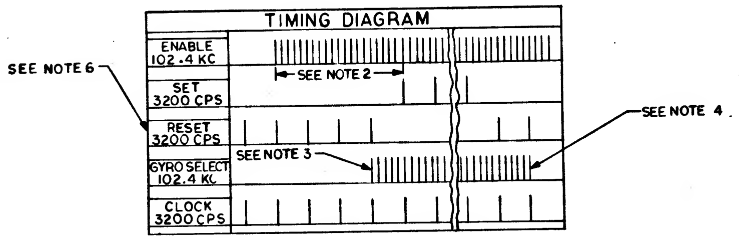
IMU

SCHEM 2018615



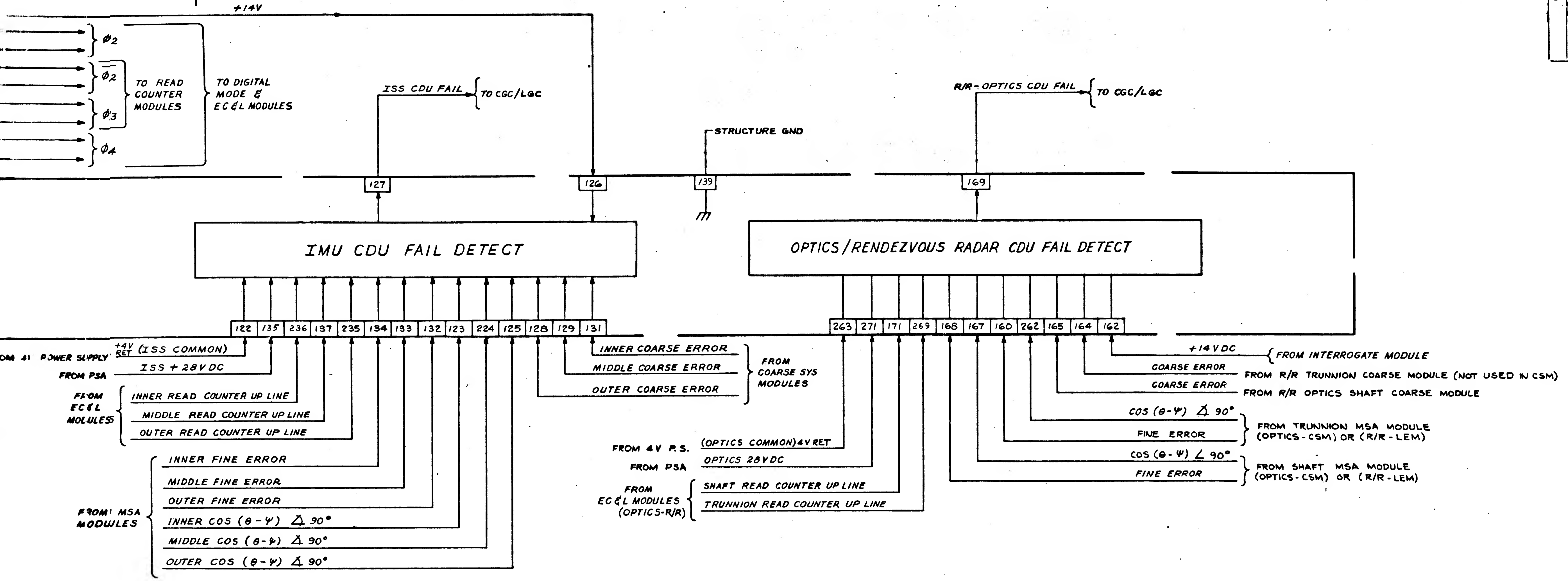


NOTES:

1. ALL NOTED WIRES TO BE MICRODOT TYPE 2-3938
2. GYRO TORQUE ENABLE SIGNAL MUST BE RECEIVED AT LEAST 20 MILLISECONDS PRIOR TO ANY TORQUE SET PULSE
3. GYRO SELECT SIGNAL MUST BE RECEIVED AT LEAST ONE CLOCK TIME (3200 CPS) PRIOR TO ANY TORQUE SET PULSES
4. GYRO RESET PULSE MUST BE GIVEN AT LEAST ONE CLOCK TIME (3200 CPS) PRIOR TO DE-ENERGIZING THE GYRO SELECT SIGNAL LINE
5. ALL INPUTS FROM THE COMPUTER ARE TO BE TWISTED SHIELDED PAIRS
6. CURRENT SWITCH MUST BE IN RESET CONDITION PRIOR TO RECEIVING GYRO TORQUE ENABLE SIGNAL FROM THE COMPUTER
7. A POSITIVE AGC TORQUE COMMAND (+$\Delta\theta$) SIGNAL PRODUCES TORQUE IN THE TM-WINDING OF THE GYRO RESULTING IN A POSITIVE ROTATION ABOUT THE GYRO INPUT AXIS
8. NO EXTERNAL LEADS SHALL BE CONNECTED TO EITHER THE +20VDC TERMINAL (PIN NO. 18) OR TO THE ± 20VDC RETURN TERMINAL (PIN NO. 17) ON THE BINARY CURRENT SWITCH
9. ERROR SIGNAL IN PHASE WITH DEMODULATOR REFERENCE RESULTS IN A POSITIVE TORQUE MOTOR VOLTAGE
10. INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY MIL-D-70327.

B Redrawn Rev A Per TDRR

SYM	DESCRIPTION	DATE	APPROVAL
B	REDRAWN PER TDRR 17147, which states that Rev. A was replaced. actually Rev A was destroyed when it was in the Rev.— Configuration.	FEB 3 '66	

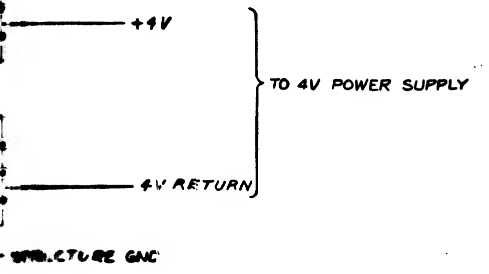


NOTES:

1. JUMPER CONNECTIONS MADE IN CDU HEADER TO INTERCONNECT INTERNAL MODULE CIRCUITRY. FOR DETAILS REFER TO CORRESPONDING MODULE SCHEMATIC.
2. STRUCTURE GROUND- TIE POINT TO WIRE WRAP HEADER ASSEMBLY.
3. SEE BLOCK II HEADER CONNECTOR DWG CSM 2010073, & LEM 6010001 FOR TEST POINT USAGE.
4. RESOLVER ANGLES θ AND SCALING DESIGNATIONS (ie. SIN 56¼°) SHOWN IN QUADRANT SELECT AND MSA MODULES, REPRESENT 16X RESOLVER OUTPUTS EXPRESSED IN ELECTRICAL DEGREES.

ABBREVIATIONS:

1. CDU - COUPLING DATA UNIT.
2. CGC - COMMAND MODULE GUIDANCE COMPUTER.
3. CSM - COMMAND AND SERVICE MODULE.
4. FB - FEEDBACK
5. FDAI - FLIGHT DIRECTOR ALTITUDE INDICATOR
6. G&C - GUIDANCE & CONTROL
7. ISS - INERTIAL SUB SYSTEM
8. LEM - LUNAR EXCURSION MODULE
9. LGC - LEM GUIDANCE COMPUTER
10. PSA - POWER & SERVO ASSEMBLY
11. R/R - RENDEVOUS RADAR
12. S/C - SPACE CRAFT
13. SPS - SERVICE PROPULSION
14. TVC - THRUST VECTOR CONTROL



DELINEATED ON THIS DRAWING:
COUPLING DATA UNIT (CDU) 2 WIRE MECH APPLICABLE FOR IMU & RENDEZVOUS RADAR CDU AXIS, LEM & CSM.

NEXT ASSY	USED ON	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS ± — DECIMALS ± — ANGLES ± — DO NOT SCALE THIS DRAWING MATERIAL — HEAT TREATMENT — FINAL FINISH —	MIT INSTRUMENTATION LAB CAMBRIDGE MASS DRAWN H. FERGUSON DATE 2-3-65 CHECKED APPROVAL 3-5-65 APPROVAL NASA APPROVAL 3-5-65 MIT APPROVAL
APPLICATION			

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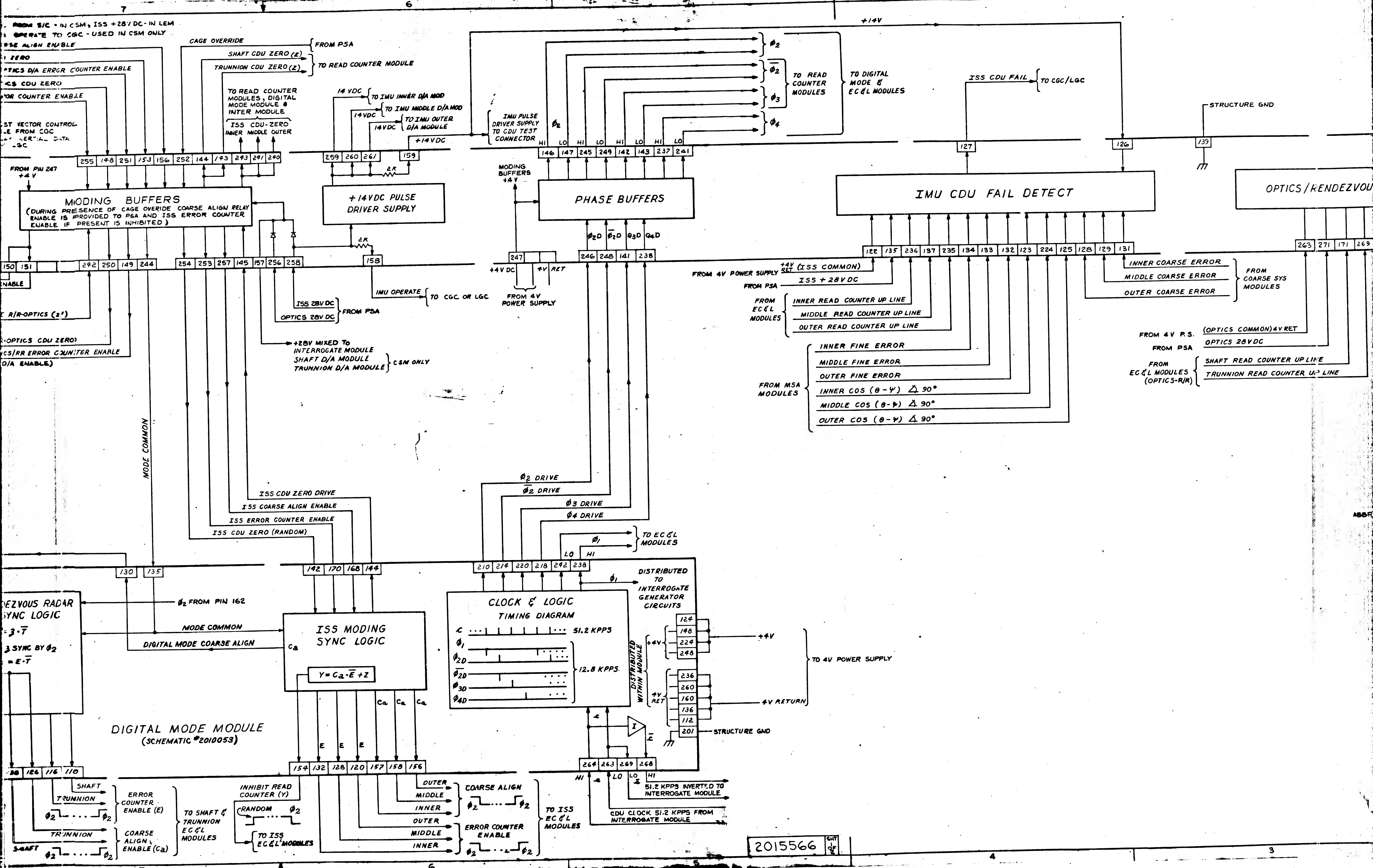
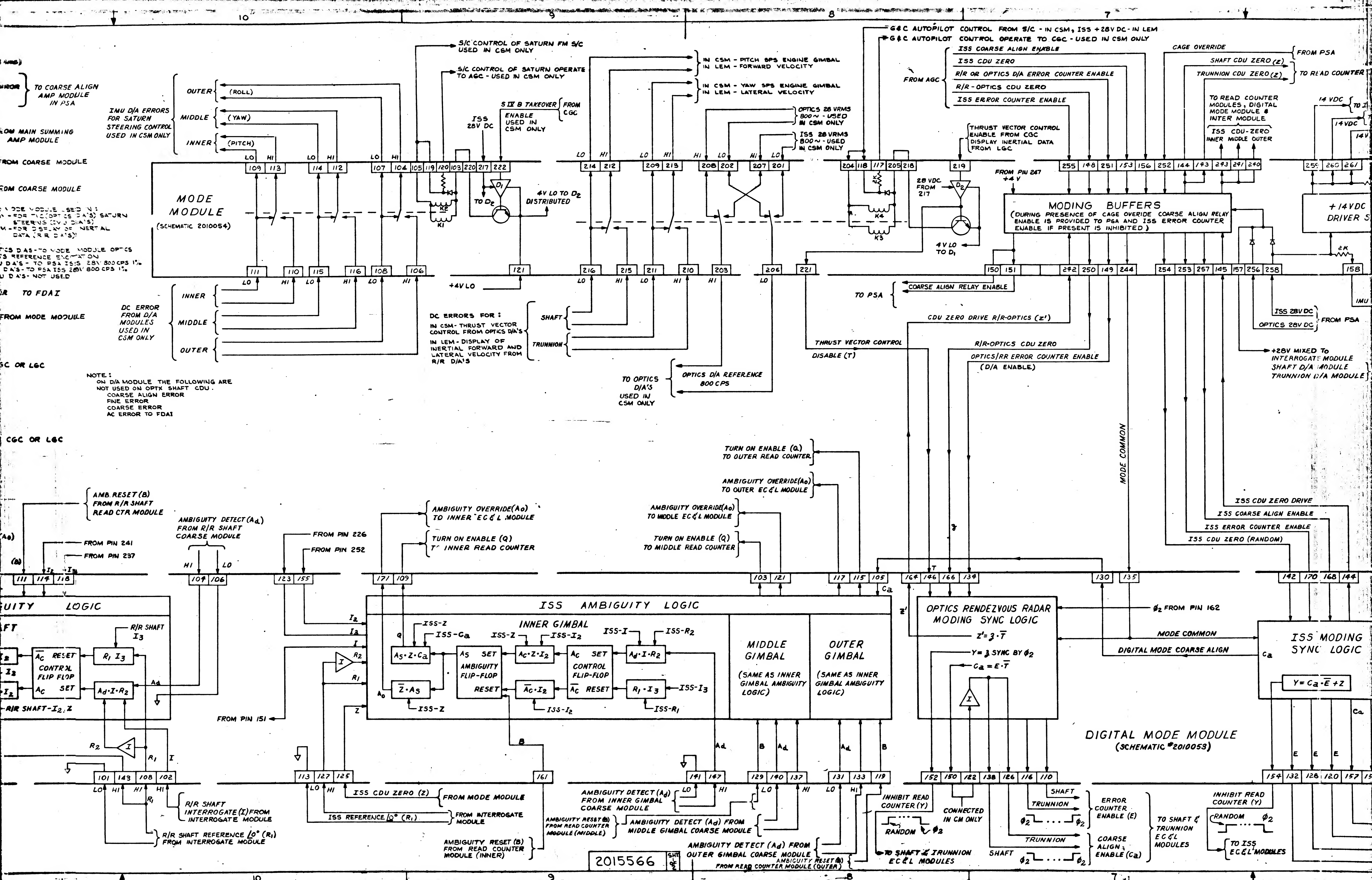
IMU-REND RADAR
CDU BLOCK DIAGRAM -
BLOCK II (2 LINE MECH)

CODE IDENT NO. | SIZE J | NASA DRAWING NO. 2015566
SCALE — | WT | SHEET 1 OF 2

2015566

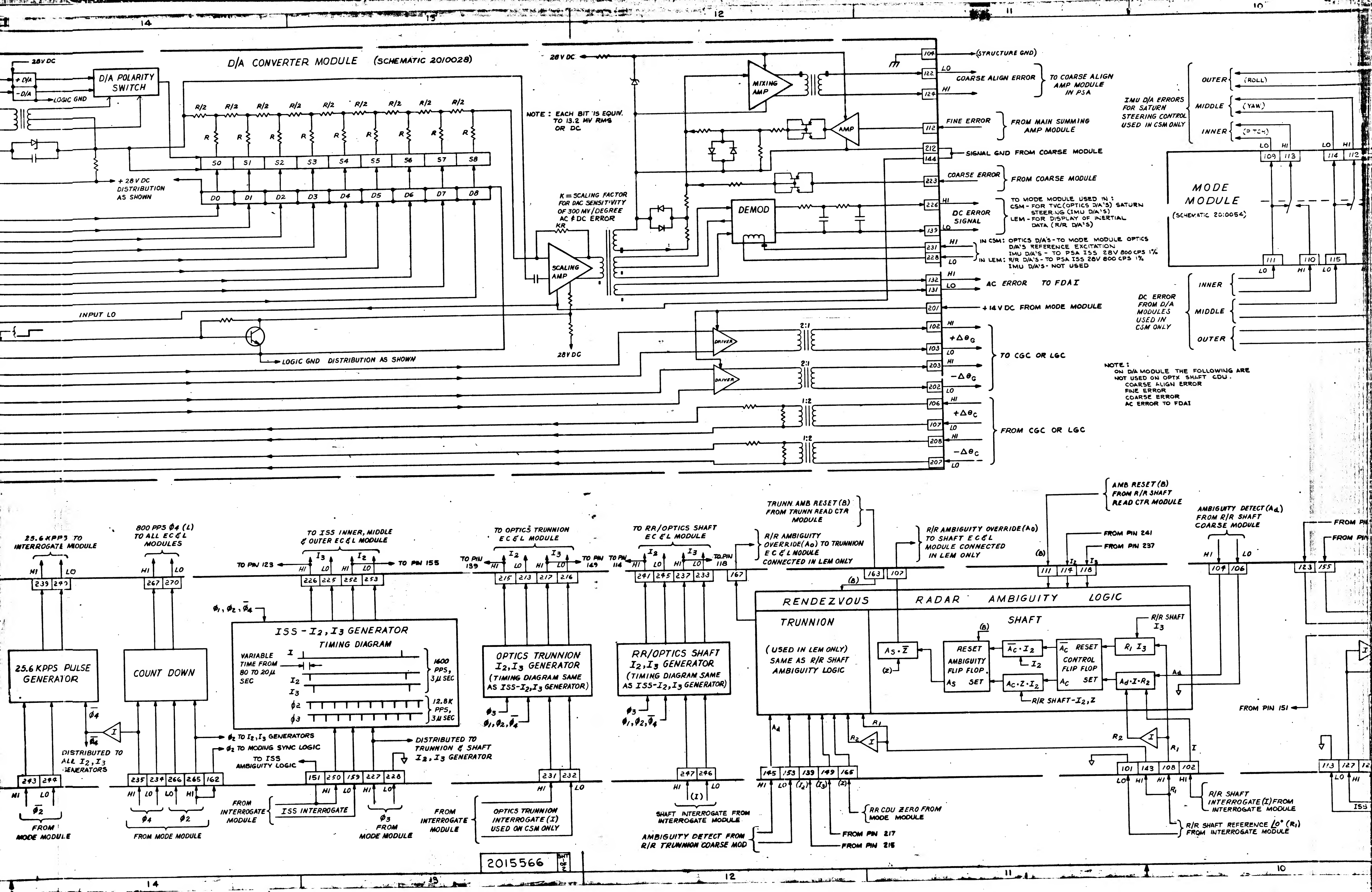


FROM S/C • IN CSM, ISS +28V DC - IN LEM
OPERATE TO CGC - USED IN CSM ONLY
COARSE ALIGN ENABLE
ZERO
OPTICS D/A ERROR COUNTER ENABLE
OPTICS CDU ZERO
ERROR COUNTER ENABLE
THRUST VECTOR CONTROL
FROM CGC
VERTICAL DATA
CGC
CAGE OVERRIDE
SHAFT CDU ZERO (2)
TRUNNION CDU ZERO (2)
FROM PSA
TO READ COUNTER MODULE
TO READ COUNTER MODULES, DIGITAL MODE MODULE & INTER MODULE
ISS CDU-ZERO
INNER MIDDLE OUTER
14 VDC
TO IMU INNER D/A MOD
TO IMU MIDDLE D/A MOD
TO IMU OUTER D/A MODULE
+14VDC
IMU PULSE DRIVER SUPPLY TO CDU TEST CONNECTOR
+14V
φ2
TO READ COUNTER MODULES
φ3
φ4
TO DIGITAL MODE & EC&L MODULES
ISS CDU FAIL
TO CGC/LGC
STRUCTURE GND
HI LO HI LO HI LO HI LO
255 148 251 153 156 252 144 143 243 241 240
259 260 261 159
146 147 245 249 142 143 237 241
127 126 139
FROM PIN 247 +4V
MODING BUFFERS
(DURING PRESENCE OF CAGE OVERIDE COARSE ALIGN RELAY ENABLE IS PROVIDED TO PSA AND ISS ERROR COUNTER ENABLE IF PRESENT IS INHIBITED)
2K
+14VDC PULSE DRIVER SUPPLY
MODING BUFFERS +4V
PHASE BUFFERS
IMU CDU FAIL DETECT
OPTICS/RENDEZVOU
φ2D φ̄2D φ3D φ4D
150 151 292 250 149 244 254 253 257 145 157 256 258 158
247 4V RET
246 248 141 238
+4V DC
FROM 4V POWER SUPPLY
122 135 236 137 235 134 133 132 123 224 125 128 129 131
263 271 171 269
ENABLE
R/R-OPTICS (2)
R-OPTICS CDU ZERO
OPTICS/RR ERROR COUNTER ENABLE
D/A ENABLE)
ISS 28V DC
OPTICS 28V DC
FROM PSA
IMU OPERATE
TO CGC OR LGC
+28V MIXED TO INTERROGATE MODULE SHAFT D/A MODULE TRUNNION D/A MODULE
CSM ONLY
FROM 4V POWER SUPPLY +4V RET (ISS COMMON)
FROM PSA ISS +28VDC
FROM EC&L MODULES
INNER READ COUNTER UP LINE
MIDDLE READ COUNTER UP LINE
OUTER READ COUNTER UP LINE
INNER COARSE ERROR
MIDDLE COARSE ERROR
OUTER COARSE ERROR
FROM COARSE SYS MODULES
FROM MSA MODULES
INNER FINE ERROR
MIDDLE FINE ERROR
OUTER FINE ERROR
INNER COS (θ-ψ) Δ 90°
MIDDLE COS (θ-ψ) Δ 90°
OUTER COS (θ-ψ) Δ 90°
FROM 4V P.S. (OPTICS COMMON) 4V RET
FROM PSA OPTICS 28VDC
FROM EC&L MODULES (OPTICS-R/R)
SHAFT READ COUNTER UP LINE
TRUNNION READ COUNTER UP LINE
MODE COMMON
ISS CDU ZERO DRIVE
ISS COARSE ALIGN ENABLE
ISS ERROR COUNTER ENABLE
ISS CDU ZERO (RANDOM)
φ2 DRIVE
φ̄2 DRIVE
φ3 DRIVE
φ4 DRIVE
φ1
TO EC&L MODULES
LO HI
130 135
142 170 168 144
210 214 220 218 242 238
DISTRIBUTED TO INTERROGATE GENERATOR CIRCUITS
RENDEZVOUS RADAR SYNC LOGIC
= 3·T̄
SYNC BY φ2
= E·T̄
φ2 FROM PIN 162
MODE COMMON
DIGITAL MODE COARSE ALIGN
Ca
ISS MODING SYNC LOGIC
Y = Ca·Ē + Z
CLOCK & LOGIC
TIMING DIAGRAM
C
φ1
φ2D
φ̄2D
φ3D
φ4D
51.2 KPPS
12.8 KPPS
DISTRIBUTED WITHIN MODULE
+4V
4V RET
124 148 224 248
236 260 160 136 112 201
+4V
4V RETURN
STRUCTURE GND
TO 4V POWER SUPPLY
I
DIGITAL MODE MODULE
(SCHEMATIC #2010053)
E E E
Ca Ca Ca
138 126 116 110
154 132 128 120 157 158 156
264 263 269 268
HI LO LO HI
SHAFT
TRUNNION
ERROR COUNTER ENABLE (E)
COARSE ALIGN ENABLE (Ca)
TO SHAFT & TRUNNION EC&L MODULES
INHIBIT READ COUNTER (Y)
RANDOM
TO ISS EC&L MODULES
OUTER
MIDDLE
INNER
COARSE ALIGN
ERROR COUNTER ENABLE
TO ISS EC&L MODULES
51.2 KPPS INVERTED TO INTERROGATE MODULE
CDU CLOCK 51.2 KPPS FROM INTERROGATE MODULE
2015566
SHT
7 6 5 4 3

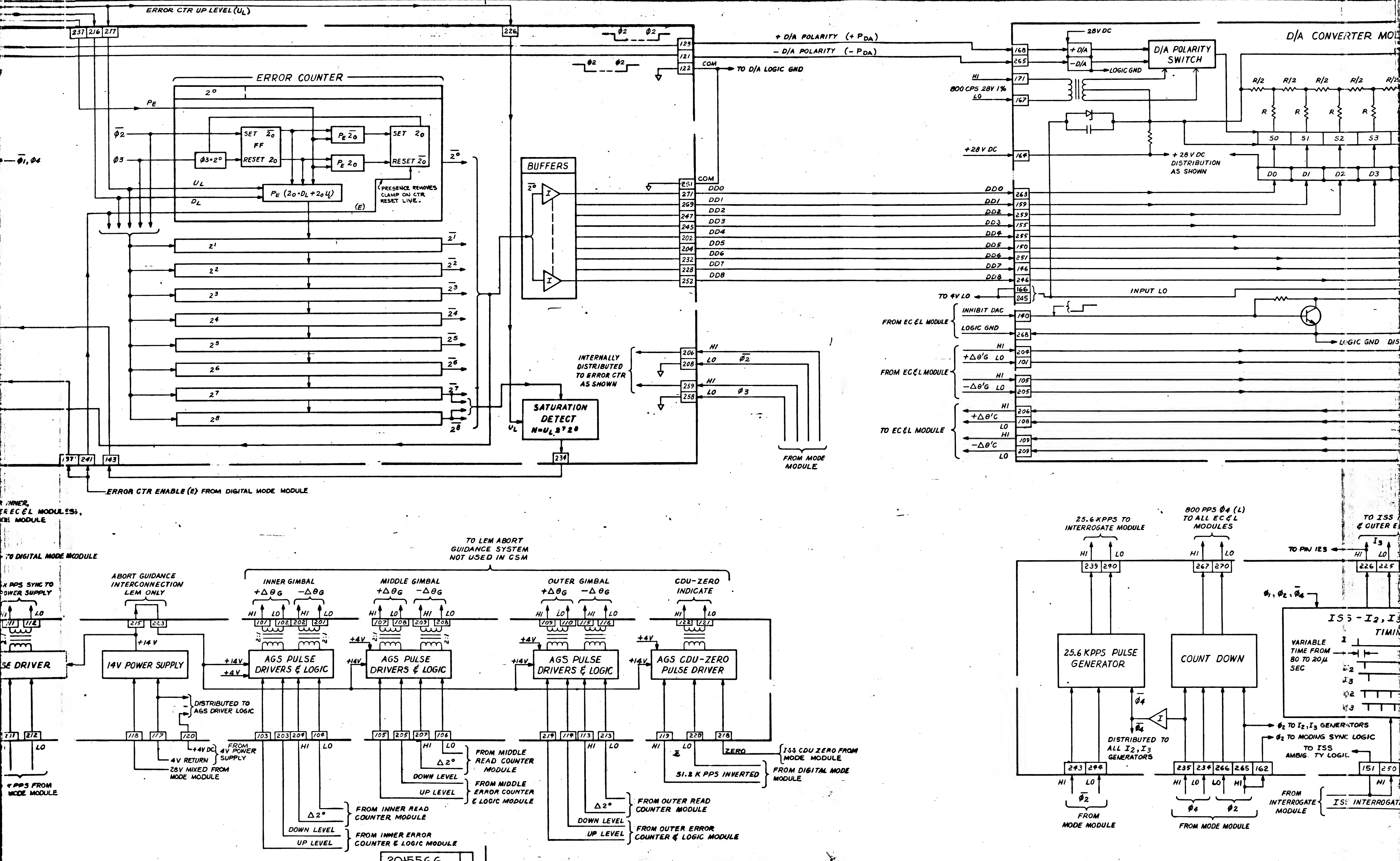


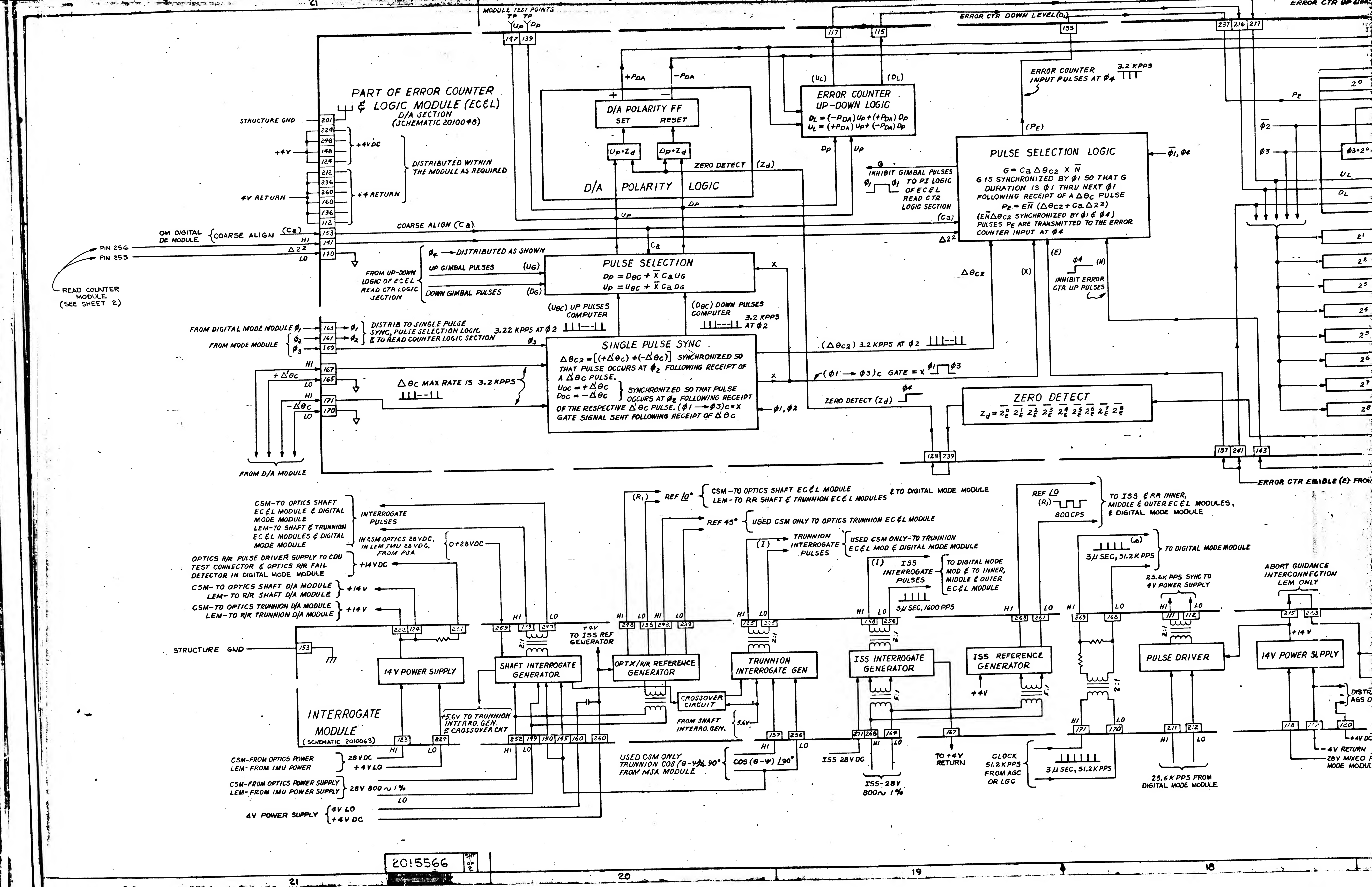
10
9
8
7
TO COARSE ALIGN AMP MODULE IN PSA
FROM MAIN SUMMING AMP MODULE
FROM COARSE MODULE
FROM COARSE MODULE
TO FDAI
FROM MODE MODULE
CGC OR LGC
CGC OR LGC
OUTER
MIDDLE
INNER
(ROLL)
(YAW)
(PITCH)
IMU D/A ERRORS FOR SATURN STEERING CONTROL USED IN CSM ONLY
S/C CONTROL OF SATURN FM S/C USED IN CSM ONLY
S/C CONTROL OF SATURN OPERATE TO AGC - USED IN CSM ONLY
S IV B TAKEOVER ENABLE USED IN CSM ONLY
FROM CGC
ISS 28V DC
IN CSM - PITCH SPS ENGINE GIMBAL
IN LEM - FORWARD VELOCITY
IN CSM - YAW SPS ENGINE GIMBAL
IN LEM - LATERAL VELOCITY
OPTICS 28 VRMS 800~ - USED IN CSM ONLY
ISS 28 VRMS 800~ - USED IN CSM ONLY
G&C AUTOPILOT CONTROL FROM S/C - IN CSM, ISS +28V DC - IN LEM
G&C AUTOPILOT CONTROL OPERATE TO CGC - USED IN CSM ONLY
FROM AGC
ISS COARSE ALIGN ENABLE
ISS CDU ZERO
R/R OR OPTICS D/A ERROR COUNTER ENABLE
R/R - OPTICS CDU ZERO
ISS ERROR COUNTER ENABLE
CAGE OVERRIDE
SHAFT CDU ZERO (Z)
TRUNNION CDU ZERO (Z)
FROM PSA
TO READ COUNTER
TO READ COUNTER MODULES, DIGITAL MODE MODULE & INTER MODULE
ISS CDU-ZERO INNER MIDDLE OUTER
14 VDC
THRUST VECTOR CONTROL ENABLE FROM CGC DISPLAY INERTIAL DATA FROM LGC
LO HI
109 113 114 112 107 104 105 119 120 103 220 217 222
214 212 209 213 208 202 207 201
204 118 117 205 218 219
255 148 251 153 156 252 144 193 293 291 240
259 260 261
MODE MODULE
(SCHEMATIC 2010054)
K1 K2 K3 K4
TO D2
D1 D2
4V LO TO D2 DISTRIBUTED
28 VDC FROM 217
4V LO TO D1
FROM PIN 247 +4 V
MODING BUFFERS
(DURING PRESENCE OF CAGE OVERIDE COARSE ALIGN RELAY ENABLE IS PROVIDED TO PSA AND ISS ERROR COUNTER ENABLE IF PRESENT IS INHIBITED)
+14VDC DRIVER
2K
111 110 115 116 108 106 121 216 215 211 210 203 206 221
150 151 292 250 149 244 254 253 257 145 157 256 258 158
+4V LO
DC ERROR FROM D/A MODULES USED IN CSM ONLY
DC ERRORS FOR : IN CSM - THRUST VECTOR CONTROL FROM OPTICS D/A'S IN LEM - DISPLAY OF INERTIAL FORWARD AND LATERAL VELOCITY FROM R/R D/A'S
SHAFT
TRUNNION
TO PSA
COARSE ALIGN RELAY ENABLE
CDU ZERO DRIVE R/R-OPTICS (Z')
THRUST VECTOR CONTROL DISABLE (T)
R/R-OPTICS CDU ZERO
OPTICS/RR ERROR COUNTER ENABLE (D/A ENABLE)
TO OPTICS D/A'S USED IN CSM ONLY
OPTICS D/A REFERENCE 800 CPS
ISS 28V DC
OPTICS 28V DC
FROM PSA
IMU
+28V MIXED TO INTERROGATE MODULE SHAFT D/A MODULE TRUNNION D/A MODULE
NOTE: ON D/A MODULE THE FOLLOWING ARE NOT USED ON OPTX SHAFT CDU. COARSE ALIGN ERROR FINE ERROR COARSE ERROR AC ERROR TO FDAI
MODE COMMON
TURN ON ENABLE (Q) TO OUTER READ COUNTER
AMBIGUITY OVERRIDE (A0) TO OUTER EC&L MODULE
AMBIGUITY OVERRIDE (A0) TO INNER EC&L MODULE
TURN ON ENABLE (Q) TO INNER READ COUNTER
AMBIGUITY OVERRIDE (A0) TO MIDDLE EC&L MODULE
TURN ON ENABLE (Q) TO MIDDLE READ COUNTER
ISS CDU ZERO DRIVE
ISS COARSE ALIGN ENABLE
ISS ERROR COUNTER ENABLE
ISS CDU ZERO (RANDOM)
AMB. RESET (B) FROM R/R SHAFT READ CTR MODULE
AMBIGUITY DETECT (Ad) FROM R/R SHAFT COARSE MODULE
FROM PIN 241
FROM PIN 237
FROM PIN 226
FROM PIN 252
111 114 118 104 106 123 155 171 109 103 121 117 115 105 164 146 166 134 130 135 142 170 168 144
AMBIGUITY LOGIC
R/R SHAFT I3
Ac RESET
CONTROL FLIP FLOP
Ac SET
R1 I3
Ad·I·R2
R/R SHAFT-I2, Z
ISS AMBIGUITY LOGIC
INNER GIMBAL
MIDDLE GIMBAL
OUTER GIMBAL
(SAME AS INNER GIMBAL AMBIGUITY LOGIC)
ISS-Z
ISS-Ca
ISS-I2
ISS-I
ISS-R2
ISS-I3
ISS-R1
As·Z·Ca
As SET AMBIGUITY FLIP-FLOP RESET
Ac·Z·I2
Ac SET CONTROL FLIP-FLOP Ac RESET
Ad·I·R2
Z·As
Ac·I2
R1·I3
FROM PIN 151
OPTICS RENDEZVOUS RADAR MODING SYNC LOGIC
Z' = 3·T
Y = 3 SYNC BY φ2
Ca = E·T
φ2 FROM PIN 162
MODE COMMON
DIGITAL MODE COARSE ALIGN
ISS MODING SYNC LOGIC
Y = Ca·E + Z
DIGITAL MODE MODULE
(SCHEMATIC #2010053)
101 143 108 102
113 127 125 161 141 147 129 140 137 131 133 119 152 150 122 138 126 116 110 154 132 128 120 157
R/R SHAFT INTERROGATE (I) FROM INTERROGATE MODULE
R/R SHAFT REFERENCE /0° (R1) FROM INTERROGATE MODULE
ISS CDU ZERO (Z)
FROM MODE MODULE
ISS REFERENCE /0° (R1)
FROM INTERROGATE MODULE
AMBIGUITY RESET (B) FROM READ COUNTER MODULE (INNER)
AMBIGUITY DETECT (Ad) FROM INNER GIMBAL COARSE MODULE
AMBIGUITY RESET (B) FROM READ COUNTER MODULE (MIDDLE)
AMBIGUITY DETECT (Ad) FROM MIDDLE GIMBAL COARSE MODULE
AMBIGUITY DETECT (Ad) FROM OUTER GIMBAL COARSE MODULE
AMBIGUITY RESET (B) FROM READ COUNTER MODULE (OUTER)
INHIBIT READ COUNTER (Y)
CONNECTED IN CM ONLY
RANDOM φ2
TO SHAFT & TRUNNION EC&L MODULES
SHAFT
TRUNNION
ERROR COUNTER ENABLE (E)
COARSE ALIGN ENABLE (Ca)
TO SHAFT & TRUNNION EC&L MODULES
INHIBIT READ COUNTER (Y)
RANDOM φ2
TO ISS EC&L MODULES
2015566
SHT 2 OF 2

F-4

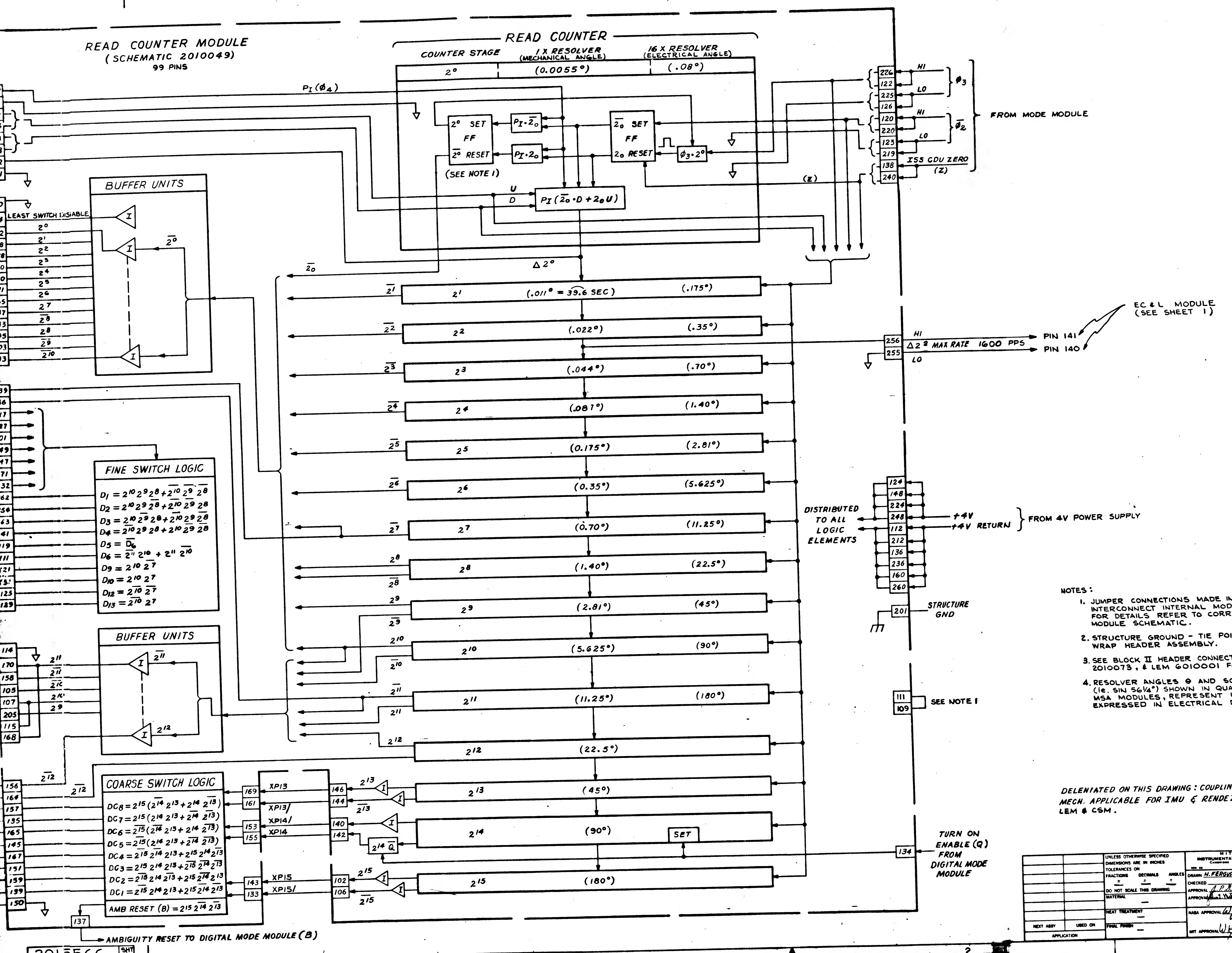

14
13
12
11
10
D/A CONVERTER MODULE (SCHEMATIC 2010028)
28V DC
+D/A
-D/A
D/A POLARITY SWITCH
LOGIC GND
+28V DC DISTRIBUTION AS SHOWN
R/2
R
S0 S1 S2 S3 S4 S5 S6 S7 S8
D0 D1 D2 D3 D4 D5 D6 D7 D8
NOTE: EACH BIT IS EQUIV. TO 13.2 MV RMS OR DC
K = SCALING FACTOR FOR DAC SENSITIVITY OF 300 MV/DEGREE AC & DC ERROR
KR
SCALING AMP
INPUT LO
LOGIC GND DISTRIBUTION AS SHOWN
28V DC
MIXING AMP
AMP
DEMOD
DRIVER
2:1
1:2
(STRUCTURE GND)
104
122
124
112
212
144
223
226
139
231
228
132
131
201
102
103
203
202
106
107
208
207
LO
HI
COARSE ALIGN ERROR
TO COARSE ALIGN AMP MODULE IN PSA
FINE ERROR
FROM MAIN SUMMING AMP MODULE
SIGNAL GND FROM COARSE MODULE
COARSE ERROR
FROM COARSE MODULE
DC ERROR SIGNAL
TO MODE MODULE USED IN: CSM - FOR TVC (OPTICS D/A'S) SATURN STEERING (IMU D/A'S) LEM - FOR DISPLAY OF INERTIAL DATA (R/R D/A'S)
IN CSM: OPTICS D/A'S - TO MODE MODULE OPTICS D/A'S REFERENCE EXCITATION IMU D/A'S - TO PSA ISS 28V 800 CPS 1%
IN LEM: R/R D/A'S - TO PSA ISS 28V 800 CPS 1% IMU D/A'S - NOT USED
AC ERROR TO FDAI
+14V DC FROM MODE MODULE
+Δθ_G
-Δθ_G
TO CGC OR LGC
+Δθ_C
-Δθ_C
FROM CGC OR LGC
IMU D/A ERRORS FOR SATURN STEERING CONTROL USED IN CSM ONLY
OUTER (ROLL)
MIDDLE (YAW)
INNER (PITCH)
109 113 114 112
MODE MODULE (SCHEMATIC 2010054)
111 110 115
DC ERROR FROM D/A MODULES USED IN CSM ONLY
INNER
MIDDLE
OUTER
NOTE: ON D/A MODULE THE FOLLOWING ARE NOT USED ON OPTX SHAFT CDU. COARSE ALIGN ERROR FINE ERROR COARSE ERROR AC ERROR TO FDAI
25.6 KPPS TO INTERROGATE MODULE
239 240
25.6 KPPS PULSE GENERATOR
Φ̄4
I
DISTRIBUTED TO ALL I2, I3 GENERATORS
243 244
Φ2
FROM MODE MODULE
800 PPS Φ4 (L) TO ALL EC&L MODULES
267 270
COUNT DOWN
235 234 266 265 162
Φ2 TO I2, I3 GENERATORS
Φ2 TO MODING SYNC LOGIC
TO ISS AMBIGUITY LOGIC
Φ4
FROM MODE MODULE
TO ISS INNER, MIDDLE & OUTER EC&L MODULE
TO PIN 123
TO PIN 155
226 225 252 253
Φ1, Φ2, Φ̄4
ISS-I2, I3 GENERATOR
TIMING DIAGRAM
VARIABLE TIME FROM 80 TO 20μ SEC
1600 PPS, 3μ SEC
12.8K PPS, 3μ SEC
151 250 159 227 228
DISTRIBUTED TO TRUNNION & SHAFT I2, I3 GENERATOR
FROM INTERROGATE MODULE
ISS INTERROGATE
Φ3 FROM MODE MODULE
TO OPTICS TRUNNION EC&L MODULE
TO PIN 139
TO PIN 149
215 213 217 216
OPTICS TRUNNION I2, I3 GENERATOR (TIMING DIAGRAM SAME AS ISS-I2, I3 GENERATOR)
231 232
FROM INTERROGATE MODULE
OPTICS TRUNNION INTERROGATE (I) USED ON CSM ONLY
TO RR/OPTICS SHAFT EC&L MODULE
TO PIN 114
TO PIN 118
241 245 237 233
RR/OPTICS SHAFT I2, I3 GENERATOR (TIMING DIAGRAM SAME AS ISS-I2, I3 GENERATOR)
247 246
SHAFT INTERROGATE FROM INTERROGATE MODULE
AMBIGUITY DETECT FROM R/R TRUNNION COARSE MOD
TRUNN. AMB RESET (B) FROM TRUNN READ CTR MODULE
R/R AMBIGUITY OVERRIDE (A0) TO TRUNNION EC&L MODULE CONNECTED IN LEM ONLY
167 163 107
R/R AMBIGUITY OVERRIDE (A0) TO SHAFT EC&L MODULE CONNECTED IN LEM ONLY
AMB RESET (B) FROM R/R SHAFT READ CTR MODULE
FROM PIN 241
FROM PIN 237
111 114 118
AMBIGUITY DETECT (Ad) FROM R/R SHAFT COARSE MODULE
104 106
123 155
FROM PIN
RENDEZVOUS RADAR AMBIGUITY LOGIC
TRUNNION
(USED IN LEM ONLY) SAME AS R/R SHAFT AMBIGUITY LOGIC
SHAFT
As·Z̄
RESET AMBIGUITY FLIP FLOP
Āc·I2
Ac·Z·I2
CONTROL FLIP FLOP
R1 I3
Ad·I·R2
R/R SHAFT I3
R/R SHAFT-I2, Z
FROM PIN 151
145 153 139 149 165
RR CDU ZERO FROM MODE MODULE
FROM PIN 217
FROM PIN 215
101 143 108 102
R/R SHAFT INTERROGATE (I) FROM INTERROGATE MODULE
R/R SHAFT REFERENCE 0° (R1) FROM INTERROGATE MODULE
113 127
ISS
2015566
SHT 1 OF 2

F-3


ERROR CTR UP LEVEL (U_L)
ERROR COUNTER
P_E
$\bar{\phi}_2$
ϕ_3
$\bar{\phi}_1, \phi_4$
SET $\bar{2}_0$ FF RESET 2_0
$\phi_3 \cdot 2^0$
$P_E \bar{2}_0$
$P_E 2_0$
SET 2_0 RESET $\bar{2}_0$
$P_E (2_0 \cdot D_L + \bar{2}_0 U_L)$
U_L
D_L
(E)
PRESENCE REMOVES CLAMP ON CTR RESET LINE.
$\overline{2^0}$ $\overline{2^1}$ $\overline{2^2}$ $\overline{2^3}$ $\overline{2^4}$ $\overline{2^5}$ $\overline{2^6}$ $\overline{2^7}$ $\overline{2^8}$
BUFFERS
SATURATION DETECT $N = U_L 2^7 2^8$
ERROR CTR ENABLE (E) FROM DIGITAL MODE MODULE
+ D/A POLARITY (+ P_{DA})
− D/A POLARITY (− P_{DA})
COM
TO D/A LOGIC GND
DD0 DD1 DD2 DD3 DD4 DD5 DD6 DD7 DD8
INTERNALLY DISTRIBUTED TO ERROR CTR AS SHOWN
HI LO $\bar{\phi}_2$
HI LO ϕ_3
FROM MODE MODULE
D/A CONVERTER MO
28V DC
+D/A −D/A
D/A POLARITY SWITCH
LOGIC GND
HI 800 CPS 28V 1% LO
+28 V DC
+ 28 V DC DISTRIBUTION AS SHOWN
R/2 R/2 R/2 R/2 R
S0 S1 S2 S3
D0 D1 D2 D3
TO 4V LO
INPUT LO
FROM EC&L MODULE
INHIBIT DAC
LOGIC GND
LOGIC GND DIS
FROM EC&L MODULE +Δθ'G −Δθ'G HI LO
TO EC&L MODULE +Δθ'C −Δθ'C HI LO
237 216 217 226 123 121 122 251 271 269 247 245 202 204 232 228 252 206 208 259 258 234 137 241 143
168 265 171 167 164 263 159 259 155 255 150 251 146 246 166 245 140 268 204 101 105 205 206 108 109 209
INNER, ER EC&L MODULES, DE MODULE
TO DIGITAL MODE MODULE
K PPS SYNC TO POWER SUPPLY
SE DRIVER
PPS FROM MODE MODULE
ABORT GUIDANCE INTERCONNECTION LEM ONLY
+14 V
14V POWER SUPPLY
DISTRIBUTED TO AGS DRIVER LOGIC
+4V DC 4V POWER SUPPLY FROM
4V RETURN
28V MIXED FROM MODE MODULE
TO LEM ABORT GUIDANCE SYSTEM NOT USED IN CSM
INNER GIMBAL +Δθ G −Δθ G
MIDDLE GIMBAL +Δθ G −Δθ G
OUTER GIMBAL +Δθ G −Δθ G
CDU-ZERO INDICATE
AGS PULSE DRIVERS & LOGIC
AGS CDU-ZERO PULSE DRIVER
+14V +4V
2:1
Δ2°
DOWN LEVEL
UP LEVEL
FROM INNER READ COUNTER MODULE
FROM INNER ERROR COUNTER & LOGIC MODULE
FROM MIDDLE READ COUNTER MODULE
FROM MIDDLE ERROR COUNTER & LOGIC MODULE
FROM OUTER READ COUNTER MODULE
FROM OUTER ERROR COUNTER & LOGIC MODULE
ZERO
ISS CDU ZERO FROM MODE MODULE
51.2 K PPS INVERTED
FROM DIGITAL MODE MODULE
111 112 215 223 118 117 120 211 212 107 102 202 201 103 203 209 104 107 108 203 208 105 205 207 106 109 110 115 116 219 114 113 213 122 121 119 220 218
25.6 KPPS TO INTERROGATE MODULE
800 PPS ϕ_4 (L) TO ALL EC&L MODULES
25.6 KPPS PULSE GENERATOR
COUNT DOWN
$\bar{\phi}_4$
DISTRIBUTED TO ALL I_2, I_3 GENERATORS
$\bar{\phi}_2$ FROM MODE MODULE
ϕ_4 ϕ_2 FROM MODE MODULE
239 240 267 270 243 244 235 234 266 265 162
TO ISS & OUTER E
TO PIN 123
226 225
$\phi_1, \phi_2, \bar{\phi}_4$
ISS - I_2, I_3 TIMIN
VARIABLE TIME FROM 80 TO 20μ SEC
ϕ_2 TO I_2, I_3 GENERATORS
ϕ_2 TO MODING SYNC LOGIC
TO ISS AMBIG. TY LOGIC
FROM INTERROGATE MODULE
ISS INTERROGAT
151 250
2015566
18 17 16 15 14


MODULE TEST POINTS
TP TP
Up Dp
147 139
PART OF ERROR COUNTER & LOGIC MODULE (EC&L)
D/A SECTION
(SCHEMATIC 2010048)
STRUCTURE GND
201
224
248
148
124
+4VDC
+4V
212
236
260
160
136
112
+4 RETURN
4V RETURN
DISTRIBUTED WITHIN THE MODULE AS REQUIRED
OM DIGITAL DE MODULE
COARSE ALIGN (Ca)
HI
Δ2²
LO
153
141
170
PIN 256
PIN 255
READ COUNTER MODULE (SEE SHEET 2)
D/A POLARITY FF
SET RESET
+P_DA
-P_DA
Up·Zd
Dp·Zd
ZERO DETECT (Zd)
D/A POLARITY LOGIC
Dp
Up
COARSE ALIGN (Ca)
Ca
ERROR COUNTER UP-DOWN LOGIC
D_L = (-P_DA) Up + (+P_DA) Dp
U_L = (+P_DA) Up + (-P_DA) Dp
(UL)
(DL)
117
115
133
ERROR CTR DOWN LEVEL (DL)
237 216 217
ERROR CTR UP LEVEL
ERROR COUNTER INPUT PULSES AT φ4
3.2 KPPS
(PE)
PE
φ̄2
φ3
φ3·2°
UL
DL
2°
PULSE SELECTION LOGIC
G = Ca Δθc2 X N̄
G IS SYNCHRONIZED BY φ1 SO THAT G DURATION IS φ1 THRU NEXT φ1 FOLLOWING RECEIPT OF A Δθc PULSE
PE = EN̄ (Δθc2 + CaΔ2²)
(EN̄Δθc2 SYNCHRONIZED BY φ1 & φ4)
PULSES PE ARE TRANSMITTED TO THE ERROR COUNTER INPUT AT φ4
φ̄1, φ4
G
INHIBIT GIMBAL PULSES TO PI LOGIC OF EC&L READ CTR LOGIC SECTION
φ1 φ1
(Ca)
Δ2²
Δθc2
(X)
(E)
φ4 (H)
INHIBIT ERROR CTR UP PULSES
2¹
2²
2³
2⁴
2⁵
2⁶
2⁷
2⁸
φ4 → DISTRIBUTED AS SHOWN
UP GIMBAL PULSES (UG)
DOWN GIMBAL PULSES (DG)
FROM UP-DOWN LOGIC OF EC&L READ CTR LOGIC SECTION
PULSE SELECTION
Dp = Dθc + X̄ Ca UG
Up = Uθc + X̄ Ca DG
X
(Uθc) UP PULSES COMPUTER
(Dθc) DOWN PULSES COMPUTER
3.2 KPPS AT φ2
FROM DIGITAL MODE MODULE φ1
FROM MODE MODULE φ2 φ3
163
161
159
φ1
φ2
DISTRIB TO SINGLE PULSE SYNC, PULSE SELECTION LOGIC & TO READ COUNTER LOGIC SECTION
3.22 KPPS AT φ2
φ3
SINGLE PULSE SYNC
Δθc2 = [(+Δθc) + (-Δθc)] SYNCHRONIZED SO THAT PULSE OCCURS AT φ2 FOLLOWING RECEIPT OF A Δθc PULSE.
Uθc = +Δθc
Dθc = -Δθc
SYNCHRONIZED SO THAT PULSE OCCURS AT φ2 FOLLOWING RECEIPT OF THE RESPECTIVE Δθc PULSE. (φ1 → φ3)c = X GATE SIGNAL SENT FOLLOWING RECEIPT OF Δθc
(Δθc2) 3.2 KPPS AT φ2
(φ1 → φ3)c GATE = X φ1 φ3
φ1, φ2
HI
+Δθc
167
165
HI
-Δθc
171
170
LO
Δθc MAX RATE IS 3.2 KPPS
FROM D/A MODULE
ZERO DETECT (Zd)
φ4
ZERO DETECT
Zd = 2°E 2¹E 2²E 2³E 2⁴E 2⁵E 2⁶E 2⁷E 2⁸E
129 239
137 241 143
ERROR CTR ENABLE (E) FROM
CSM-TO OPTICS SHAFT EC&L MODULE & DIGITAL MODE MODULE
LEM-TO SHAFT & TRUNNION EC&L MODULES & DIGITAL MODE MODULE
INTERROGATE PULSES
IN CSM OPTICS 28VDC, IN LEM IMU 28VDC, FROM PSA
0+28VDC
OPTICS R/R PULSE DRIVER SUPPLY TO CDU TEST CONNECTOR & OPTICS R/R FAIL DETECTOR IN DIGITAL MODE MODULE
+14VDC
CSM-TO OPTICS SHAFT D/A MODULE
LEM-TO R/R SHAFT D/A MODULE
+14V
CSM-TO OPTICS TRUNNION D/A MODULE
LEM-TO R/R TRUNNION D/A MODULE
+14V
STRUCTURE GND
153
222 124
221
14V POWER SUPPLY
INTERROGATE MODULE
(SCHEMATIC 2010063)
123
229
HI LO
CSM-FROM OPTICS POWER
LEM-FROM IMU POWER
28VDC
+4V LO
CSM-FROM OPTICS POWER SUPPLY
LEM-FROM IMU POWER SUPPLY
28V 800~ 1%
LO
4V POWER SUPPLY
4V LO
+4V DC
259
139
247
HI LO
+4V TO ISS REF GENERATOR
2:1
SHAFT INTERROGATE GENERATOR
+5.6V TO TRUNNION INTERRO. GEN. & CROSSOVER CKT
258 149 150 145 160 260
HI LO
(R1)
REF 0°
CSM-TO OPTICS SHAFT EC&L MODULE
LEM-TO RR SHAFT & TRUNNION EC&L MODULES
& TO DIGITAL MODE MODULE
REF 45°
USED CSM ONLY TO OPTICS TRUNNION EC&L MODULE
HI LO HI LO
243 138 242 239
OPTX/R/R REFERENCE GENERATOR
CROSSOVER CIRCUIT
FROM SHAFT INTERRO. GEN.
5.6V
USED CSM ONLY TRUNNION COS (θ-ψ) 90°
FROM MSA MODULE
COS (θ-ψ) 90°
(I)
TRUNNION INTERROGATE PULSES
USED CSM ONLY-TO TRUNNION EC&L MOD & DIGITAL MODE MODULE
HI LO
125 335
2:1
TRUNNION INTERROGATE GEN
137 236
HI LO
(I) ISS INTERROGATE PULSES
TO DIGITAL MODE MOD & TO INNER, MIDDLE & OUTER EC&L MODULE
3μ SEC, 1600 PPS
HI LO
158 256
2:1
ISS INTERROGATE GENERATOR
5:1
271 268 164
HI LO
ISS 28V DC
ISS-28V 800~ 1%
167
TO +4V RETURN
REF 0
(R1)
800 CPS
TO ISS & RR INNER, MIDDLE & OUTER EC&L MODULES, & DIGITAL MODE MODULE
HI LO
263 261
ISS REFERENCE GENERATOR
+4V
5:1
(a)
3μ SEC, 51.2K PPS
TO DIGITAL MODE MODULE
HI LO
269 168
2:1
HI LO
171 170
CLOCK 51.2 KPPS FROM AGC OR LGC
3μ SEC, 51.2K PPS
25.6K PPS SYNC TO 4V POWER SUPPLY
HI LO
111 112
2:1
PULSE DRIVER
211 212
HI LO
25.6K PPS FROM DIGITAL MODE MODULE
ABORT GUIDANCE INTERCONNECTION LEM ONLY
215 213
+14V
14V POWER SUPPLY
DISTR AGS D
118 117 120
+4V DC
-4V RETURN
-28V MIXED MODE MODUL
2015566
SHT 1 OF 2
21
20
19
18

SYM	DESCRIPTION	DATE	APPROVAL
B	THIS SHEET ADDED PER TDRR 17147 Actually entire document was redrawn, and the Rev — was assigned. No Rev. A was processed	FEB 3 65	CK


READ COUNTER MODULE
(SCHEMATIC 2010049)
99 PINS
READ COUNTER
COUNTER STAGE
1 X RESOLVER (MECHANICAL ANGLE)
16 X RESOLVER (ELECTRICAL ANGLE)
2°
(0.0055°)
(.08°)
$P_I(\phi_4)$
2^0 SET FF $\overline{2^0}$ RESET
(SEE NOTE 1)
$P_I \cdot \overline{2_0}$
$P_I \cdot 2_0$
$\overline{2_0}$ SET FF 2_0 RESET
$\phi_3 \cdot 2^0$
$P_I(\overline{2_0} \cdot D + 2_0 U)$
U
D
(Z)
HI
LO
ϕ_3
$\overline{\phi_2}$
226
122
225
126
120
220
123
219
138
240
ISS CDU ZERO (Z)
FROM MODE MODULE
BUFFER UNITS
LEAST SWITCH DISABLE
$\overline{2_0}$
$\Delta 2^0$
2^1 (.011° = 39.6 SEC) (.175°)
2^2 (.022°) (.35°)
2^3 (.044°) (.70°)
2^4 (.087°) (1.40°)
2^5 (0.175°) (2.81°)
2^6 (0.35°) (5.625°)
2^7 (0.70°) (11.25°)
2^8 (1.40°) (22.5°)
2^9 (2.81°) (45°)
2^{10} (5.625°) (90°)
2^{11} (11.25°) (180°)
2^{12} (22.5°)
2^{13} (45°)
2^{14} (90°)
SET
2^{15} (180°)
256
255
HI
$\Delta 2^8$ MAX RATE 1600 PPS
LO
PIN 141
PIN 140
EC & L MODULE (SEE SHEET 1)
DISTRIBUTED TO ALL LOGIC ELEMENTS
124
148
224
248
112
212
136
236
160
260
+4V
+4V RETURN
FROM 4V POWER SUPPLY
201
STRUCTURE GND
111
109
SEE NOTE 1
134
TURN ON ENABLE (Q) FROM DIGITAL MODE MODULE
FINE SWITCH LOGIC
$D_1 = 2^{10}2^9\overline{2^8} + \overline{2^{10}}\,\overline{2^9}\,\overline{2^8}$
$D_2 = 2^{10}2^9\overline{2^8} + \overline{2^{10}}2^9 2^8$
$D_3 = 2^{10}\overline{2^9}2^8 + \overline{2^{10}}2^9\overline{2^8}$
$D_4 = \overline{2^{10}}2^9 2^8 + 2^{10}2^9\overline{2^8}$
$D_5 = \overline{D_6}$
$D_6 = \overline{2^{11}}2^{10} + 2^{11}\overline{2^{10}}$
$D_9 = 2^{10}\overline{2^7}$
$D_{10} = 2^{10}2^7$
$D_{12} = \overline{2^{10}}\,\overline{2^7}$
$D_{13} = \overline{2^{10}}2^7$
BUFFER UNITS
COARSE SWITCH LOGIC
$DC_8 = 2^{15}(\overline{2^{14}}2^{13} + 2^{14}\overline{2^{13}})$
$DC_7 = 2^{15}(2^{14}2^{13} + \overline{2^{14}}\,\overline{2^{13}})$
$DC_6 = \overline{2^{15}}(\overline{2^{14}}2^{13} + 2^{14}\overline{2^{13}})$
$DC_5 = \overline{2^{15}}(2^{14}2^{13} + \overline{2^{14}}\,\overline{2^{13}})$
$DC_4 = 2^{15}2^{14}2^{13} + \overline{2^{15}}\,\overline{2^{14}}\,\overline{2^{13}}$
$DC_3 = 2^{15}2^{14}\overline{2^{13}} + \overline{2^{15}}\,\overline{2^{14}}2^{13}$
$DC_2 = \overline{2^{15}}2^{14}2^{13} + 2^{15}\overline{2^{14}}\,\overline{2^{13}}$
$DC_1 = 2^{15}\overline{2^{14}}2^{13} + \overline{2^{15}}2^{14}\overline{2^{13}}$
AMB RESET (B) = $2^{15}\,\overline{2^{14}}\,\overline{2^{13}}$
XP13
XP13/
XP14/
XP14
XP15
XP15/
169
161
153
155
143
133
146
144
140
142
102
106
137
AMBIGUITY RESET TO DIGITAL MODE MODULE (B)

NOTES:

1. JUMPER CONNECTIONS MADE IN CDU HEADER TO INTERCONNECT INTERNAL MODULE CIRCUITRY. FOR DETAILS REFER TO CORRESPONDING MODULE SCHEMATIC.
2. STRUCTURE GROUND - TIE POINT TO WIRE WRAP HEADER ASSEMBLY.
3. SEE BLOCK II HEADER CONNECTOR DWG CSM 2010073, & LEM 6010001 FOR TEST POINT USAGE.
4. RESOLVER ANGLES Θ AND SCALING DESIGNATIONS (ie. SIN 56¼°) SHOWN IN QUADRANT SELECT AND MSA MODULES, REPRESENT 16X RESOLVER OUTPUTS EXPRESSED IN ELECTRICAL DEGREES.

DELENIATED ON THIS DRAWING: COUPLING DATA UNIT (CDU) 2 WIRE MECH. APPLICABLE FOR IMU & RENDEZVOUS RADAR CDU AXIS, LEM & CSM.

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS ± DECIMALS ± ANGLES ±
DO NOT SCALE THIS DRAWING
MATERIAL —
HEAT TREATMENT —
FINAL FINISH —

MIT
INSTRUMENTATION LAB
CAMBRIDGE MASS
DRAWN H. FERGUSON DATE 2-3-65
CHECKED
APPROVAL J. P. Gilmore 2-3-65
APPROVAL
NASA APPROVAL W J Rhine 2-5-65
MIT APPROVAL

MANNED SPACECRAFT CENTER
HOUSTON, TEXAS

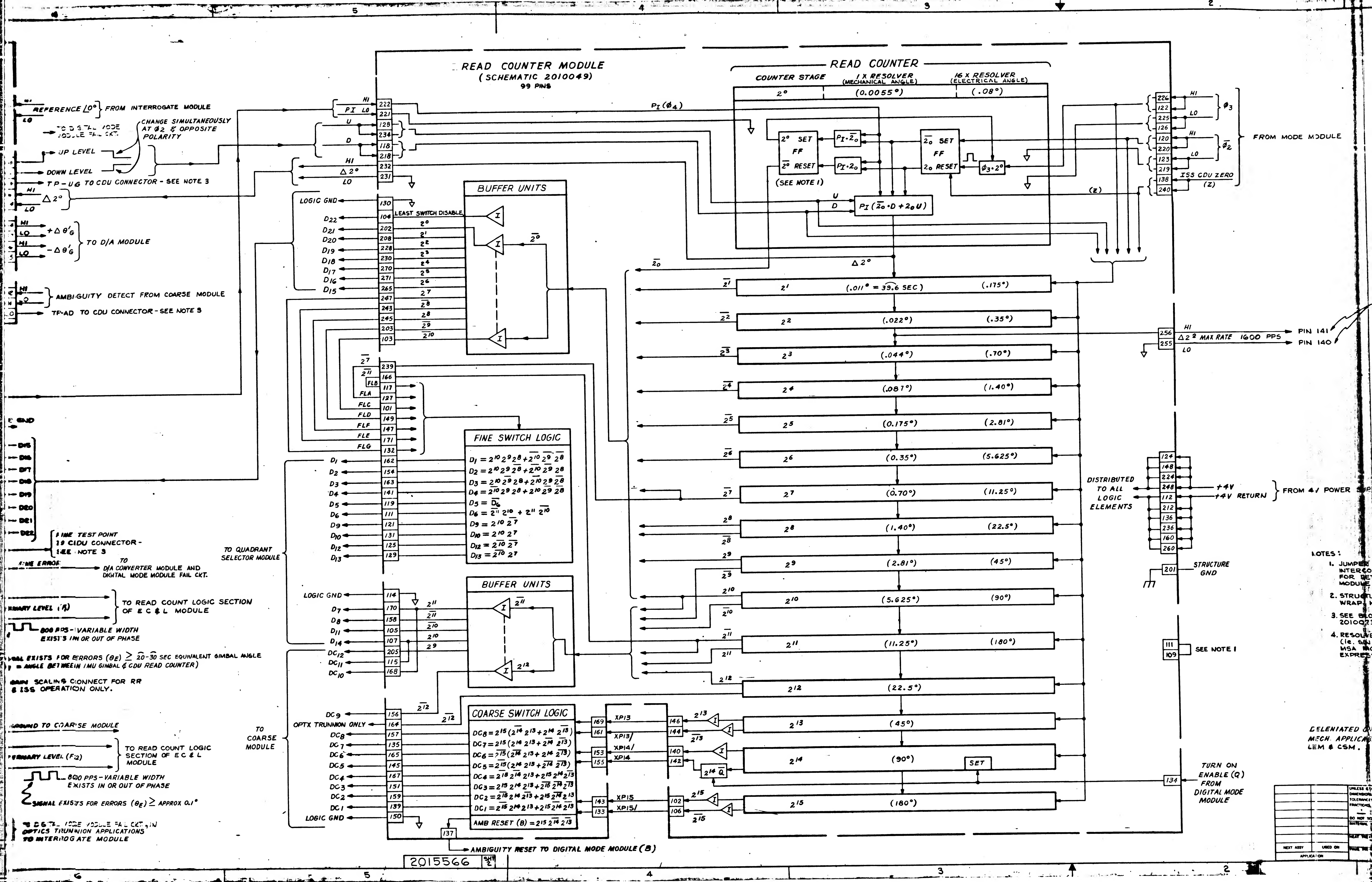
IMU-REND RADAR
CDU BLOCK DIAGRAM-
BLOCK II (2 LINE MECH)

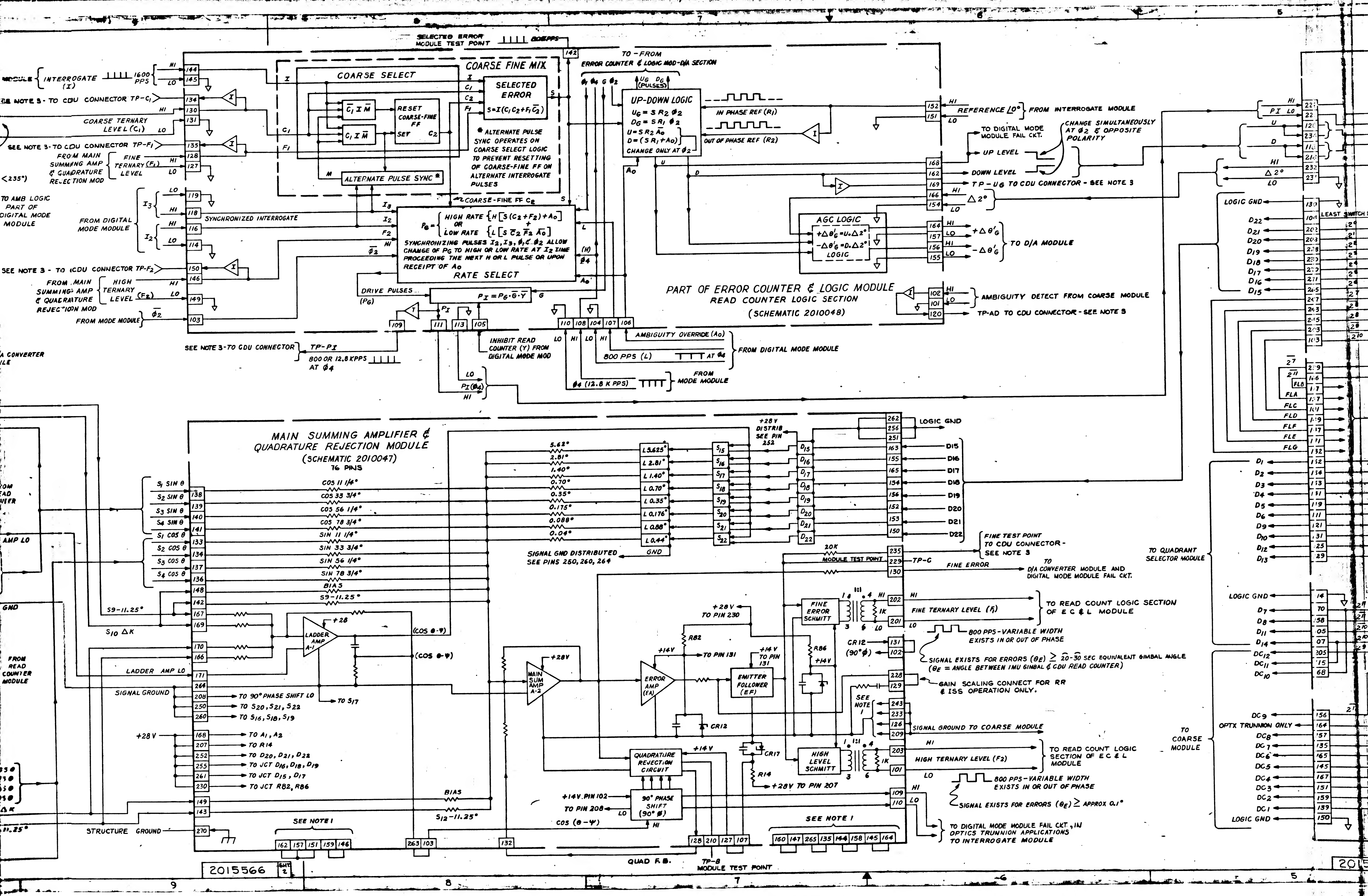
CODE IDENT NO.
SIZE J
NASA DRAWING NO. 2015566
SCALE —
WT
SHEET 2 OF 2

2015566

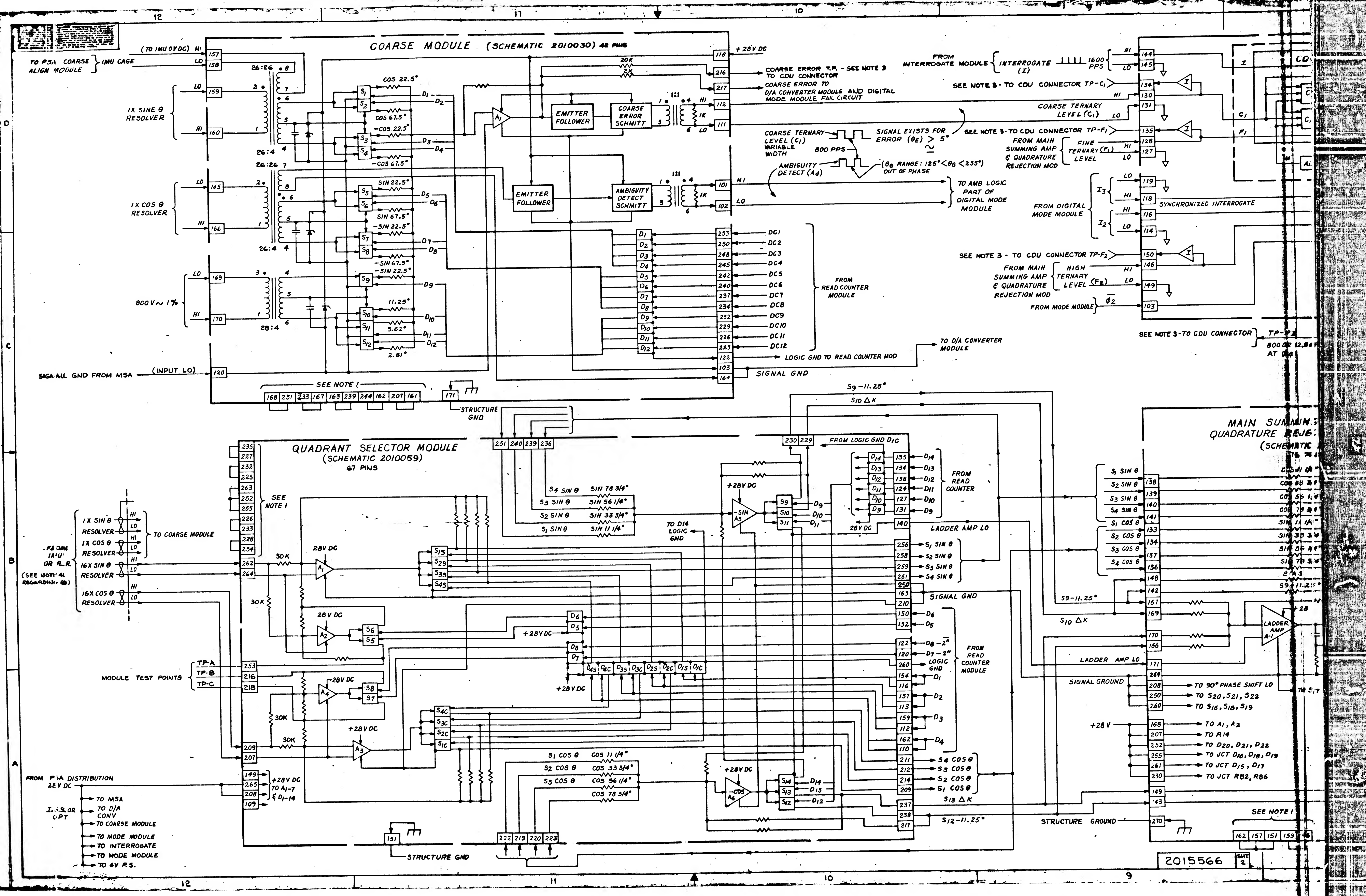
2015566 SHT 2

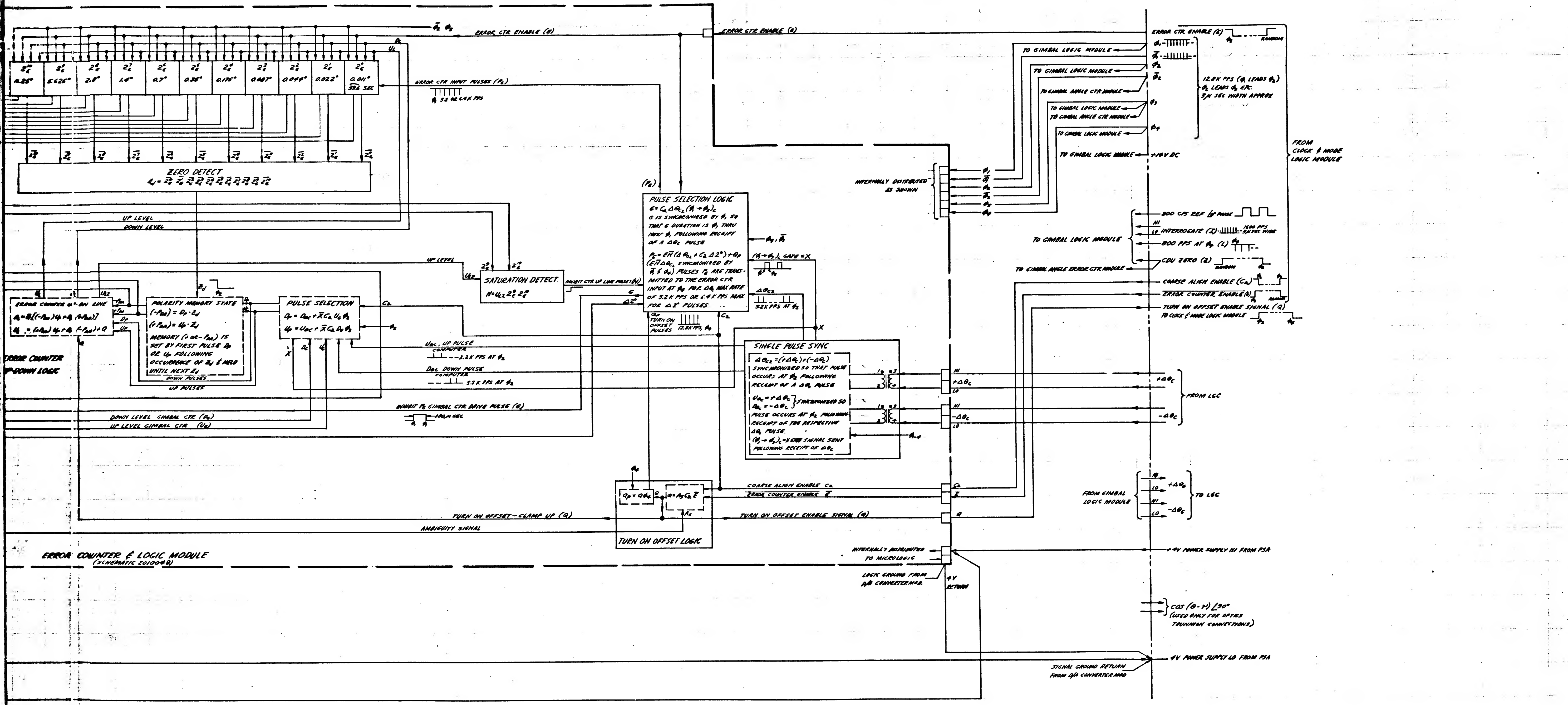
F4


READ COUNTER MODULE
(SCHEMATIC 2010049)
99 PINS
READ COUNTER
COUNTER STAGE
1 X RESOLVER (MECHANICAL ANGLE)
16 X RESOLVER (ELECTRICAL ANGLE)
2° (0.0055°) (.08°)
REFERENCE /0° FROM INTERROGATE MODULE
TO DIGITAL MODE MODULE FAIL CKT.
CHANGE SIMULTANEOUSLY AT Ø2 & OPPOSITE POLARITY
UP LEVEL
DOWN LEVEL
TP-UG TO CDU CONNECTOR - SEE NOTE 3
Δ2°
+Δθ'G
-Δθ'G
TO D/A MODULE
AMBIGUITY DETECT FROM COARSE MODULE
TP-AD TO CDU CONNECTOR - SEE NOTE 3
PI(Ø4)
2° SET FF 2° RESET
(SEE NOTE 1)
PI·2̄o
PI·2o
2̄o SET FF 2o RESET
Ø3·2°
PI(2̄o·D+2oU)
Ø3
Ø̄2
FROM MODE MODULE
ISS CDU ZERO (Z)
BUFFER UNITS
LOGIC GND
LEAST SWITCH DISABLE
FINE SWITCH LOGIC
D1 = 2^10 2^9 2̄^8 + 2̄^10 2̄^9 2^8
D5 = D̄6
D6 = 2̄^11 2^10 + 2^11 2̄^10
D9 = 2^10 2̄^7
D10 = 2^10 2^7
D12 = 2̄^10 2̄^7
D13 = 2̄^10 2^7
TO QUADRANT SELECTOR MODULE
2^1 (.011° = 39.6 SEC) (.175°)
2^2 (.022°) (.35°)
2^3 (.044°) (.70°)
2^4 (.087°) (1.40°)
2^5 (0.175°) (2.81°)
2^6 (0.35°) (5.625°)
2^7 (0.70°) (11.25°)
2^8 (1.40°) (22.5°)
2^9 (2.81°) (45°)
2^10 (5.625°) (90°)
2^11 (11.25°) (180°)
2^12 (22.5°)
2^13 (45°)
2^14 (90°) SET
2^15 (180°)
Δ2^2 MAX RATE 1600 PPS
PIN 141
PIN 140
DISTRIBUTED TO ALL LOGIC ELEMENTS
+4V
+4V RETURN
FROM 4V POWER SUPPLY
STRUCTURE GND
SEE NOTE 1
TURN ON ENABLE (Q) FROM DIGITAL MODE MODULE
FINE TEST POINT TO CDU CONNECTOR - SEE NOTE 3
FINE ERROR TO D/A CONVERTER MODULE AND DIGITAL MODE MODULE FAIL CKT.
PRIMARY LEVEL (F1)
TO READ COUNT LOGIC SECTION OF E C & L MODULE
800 PPS - VARIABLE WIDTH EXISTS IN OR OUT OF PHASE
SIGNAL EXISTS FOR ERRORS (θE) ≥ 20-30 SEC EQUIVALENT GIMBAL ANGLE
θE = ANGLE BETWEEN IMU GIMBAL & CDU READ COUNTER)
GAIN SCALING CONNECT FOR RR & ISS OPERATION ONLY.
GROUND TO COARSE MODULE
PRIMARY LEVEL (F2)
TO READ COUNT LOGIC SECTION OF E C & L MODULE
800 PPS - VARIABLE WIDTH EXISTS IN OR OUT OF PHASE
SIGNAL EXISTS FOR ERRORS (θE) ≥ APPROX 0.1°
TO DIGITAL MODE MODULE FAIL CKT, IN OPTICS TRUNNION APPLICATIONS TO INTERROGATE MODULE
TO COARSE MODULE
OPTX TRUNNION ONLY
COARSE SWITCH LOGIC
DC8 = 2^15(2̄^14 2^13 + 2^14 2̄^13)
DC7 = 2^15(2^14 2^13 + 2̄^14 2̄^13)
DC6 = 2̄^15(2̄^14 2^13 + 2^14 2̄^13)
DC5 = 2̄^15(2^14 2^13 + 2̄^14 2̄^13)
DC4 = 2^15 2^14 2^13 + 2̄^15 2̄^14 2̄^13
DC3 = 2^15 2^14 2^13 + 2̄^15 2̄^14 2̄^13
DC2 = 2̄^15 2^14 2^13 + 2^15 2̄^14 2^13
DC1 = 2̄^15 2^14 2^13 + 2^15 2^14 2̄^13
AMB RESET (B) = 2^15 2̄^14 2̄^13
XP13 XP13/ XP14/ XP14 XP15 XP15/
AMBIGUITY RESET TO DIGITAL MODE MODULE (B)
NOTES:
1. JUMPER INTERCO FOR DE MODULE
2. STRUCTU WRAP
3. SEE BLO 201002
4. RESOLVE (I.E. 6 MSA EXPRES
DELENIATED MECH. APPLICA LEM & CSM.
NEXT ASSY USED ON APPLICATION
6 5 4 3 2



SELECTED ERROR MODULE TEST POINT 800PPS
142
TO-FROM ERROR COUNTER & LOGIC MOD-D/A SECTION
INTERROGATE (I) 1600 PPS
COARSE FINE MIX
COARSE SELECT
SELECTED ERROR
S=I(C1C2+F1C̄2)
RESET COARSE-FINE FF
SET
ALTERNATE PULSE SYNC *
* ALTERNATE PULSE SYNC OPERATES ON COARSE SELECT LOGIC TO PREVENT RESETTING OF COARSE-FINE FF ON ALTERNATE INTERROGATE PULSES
COARSE-FINE FF C2
SEE NOTE 3-TO CDU CONNECTOR TP-C1
COARSE TERNARY LEVEL (C1)
SEE NOTE 3-TO CDU CONNECTOR TP-F1
FROM MAIN SUMMING AMP & QUADRATURE REJECTION MOD
FINE TERNARY (F1) LEVEL
TO AMB LOGIC PART OF DIGITAL MODE MODULE
FROM DIGITAL MODE MODULE
SYNCHRONIZED INTERROGATE
SEE NOTE 3 - TO CDU CONNECTOR TP-F2
FROM MAIN SUMMING AMP & QUADRATURE REJECTION MOD
HIGH TERNARY LEVEL (F2)
FROM MODE MODULE
UP-DOWN LOGIC
UG = S R2 φ2
DG = S R1 φ2
U = S R2 Ā0
D = (S R1 + A0)
CHANGE ONLY AT φ2
IN PHASE REF (R1)
OUT OF PHASE REF (R2)
REFERENCE ∠0° FROM INTERROGATE MODULE
TO DIGITAL MODE MODULE FAIL CKT.
CHANGE SIMULTANEOUSLY AT φ2 & OPPOSITE POLARITY
UP LEVEL
DOWN LEVEL
TP-UG TO CDU CONNECTOR - SEE NOTE 3
Δ2°
AGC LOGIC
+Δθ'G = U·Δ2°
-Δθ'G = D·Δ2°
LOGIC
+Δθ'G
-Δθ'G
TO D/A MODULE
PG = HIGH RATE {H[S(C2+F2)+A0]} OR LOW RATE {L[S C̄2 F̄2 Ā0]}
SYNCHRONIZING PULSES I2, I3, φ1 & φ2 ALLOW CHANGE OF PG TO HIGH OR LOW RATE AT I2 TIME PROCEEDING THE NEXT H OR L PULSE OR UPON RECEIPT OF A0
RATE SELECT
DRIVE PULSES (PG)
PI = PG·Ḡ·Ȳ
PART OF ERROR COUNTER & LOGIC MODULE
READ COUNTER LOGIC SECTION
(SCHEMATIC 2010048)
AMBIGUITY DETECT FROM COARSE MODULE
TP-AD TO CDU CONNECTOR - SEE NOTE 3
SEE NOTE 3-TO CDU CONNECTOR TP-PI
800 OR 12.8 KPPS AT φ4
INHIBIT READ COUNTER (Y) FROM DIGITAL MODE MOD
AMBIGUITY OVERRIDE (A0)
800 PPS (L) AT φ4
FROM DIGITAL MODE MODULE
φ4 (12.8 K PPS)
FROM MODE MODULE
LOGIC GND
LEAST SWITCH
TO QUADRANT SELECTOR MODULE
MAIN SUMMING AMPLIFIER & QUADRATURE REJECTION MODULE
(SCHEMATIC 2010047)
76 PINS
S1 SIN θ
S2 SIN θ
S3 SIN θ
S4 SIN θ
S1 COS θ
S2 COS θ
S3 COS θ
S4 COS θ
COS 11 1/4°
COS 33 3/4°
COS 56 1/4°
COS 78 3/4°
SIN 11 1/4°
SIN 33 3/4°
SIN 56 1/4°
SIN 78 3/4°
BIAS
S9-11.25°
S10 ΔK
5.62°
2.81°
1.40°
0.70°
0.35°
0.175°
0.088°
0.04°
L 5.625°
L 2.81°
L 1.40°
L 0.70°
L 0.35°
L 0.176°
L 0.88°
L 0.44°
+28 V DISTRIB SEE PIN 252
SIGNAL GND DISTRIBUTED SEE PINS 250, 260, 264
FINE TEST POINT TO CDU CONNECTOR - SEE NOTE 3
20K
MODULE TEST POINT
TP-C
FINE ERROR
TO D/A CONVERTER MODULE AND DIGITAL MODE MODULE FAIL CKT.
LADDER AMP A-1
(COS θ-ψ)
LADDER AMP LO
SIGNAL GROUND
TO 90° PHASE SHIFT LO
TO S20, S21, S22
TO S16, S18, S19
TO S17
+28 V
TO A1, A2
TO R14
TO D20, D21, D22
TO JCT D16, D18, D19
TO JCT D15, D17
TO JCT R82, R86
STRUCTURE GROUND
MAIN SUM AMP A-2
ERROR AMP (EA)
EMITTER FOLLOWER (EF)
+28V TO PIN 230
TO PIN 131
R82
R86
CR12
CR17
R14
+28V TO PIN 207
FINE ERROR SCHMITT
FINE TERNARY LEVEL (F1)
TO READ COUNT LOGIC SECTION OF EC&L MODULE
800 PPS-VARIABLE WIDTH EXISTS IN OR OUT OF PHASE
CR12 (90°φ)
SIGNAL EXISTS FOR ERRORS (θE) ≥ 20-30 SEC EQUIVALENT GIMBAL ANGLE (θE = ANGLE BETWEEN IMU GIMBAL & CDU READ COUNTER)
GAIN SCALING CONNECT FOR RR & ISS OPERATION ONLY.
SEE NOTE 1
SIGNAL GROUND TO COARSE MODULE
HIGH LEVEL SCHMITT
HIGH TERNARY LEVEL (F2)
TO READ COUNT LOGIC SECTION OF EC&L MODULE
SIGNAL EXISTS FOR ERRORS (θE) ≥ APPROX 0.1°
QUADRATURE REJECTION CIRCUIT
90° PHASE SHIFT (90° φ)
+14V PIN 102
TO PIN 208
COS (θ-ψ)
BIAS
S12-11.25°
TO DIGITAL MODE MODULE FAIL CKT, IN OPTICS TRUNNION APPLICATIONS TO INTERROGATE MODULE
QUAD F.B.
TP-8 MODULE TEST POINT
TO COARSE MODULE
OPTX TRUNNION ONLY
LOGIC GND

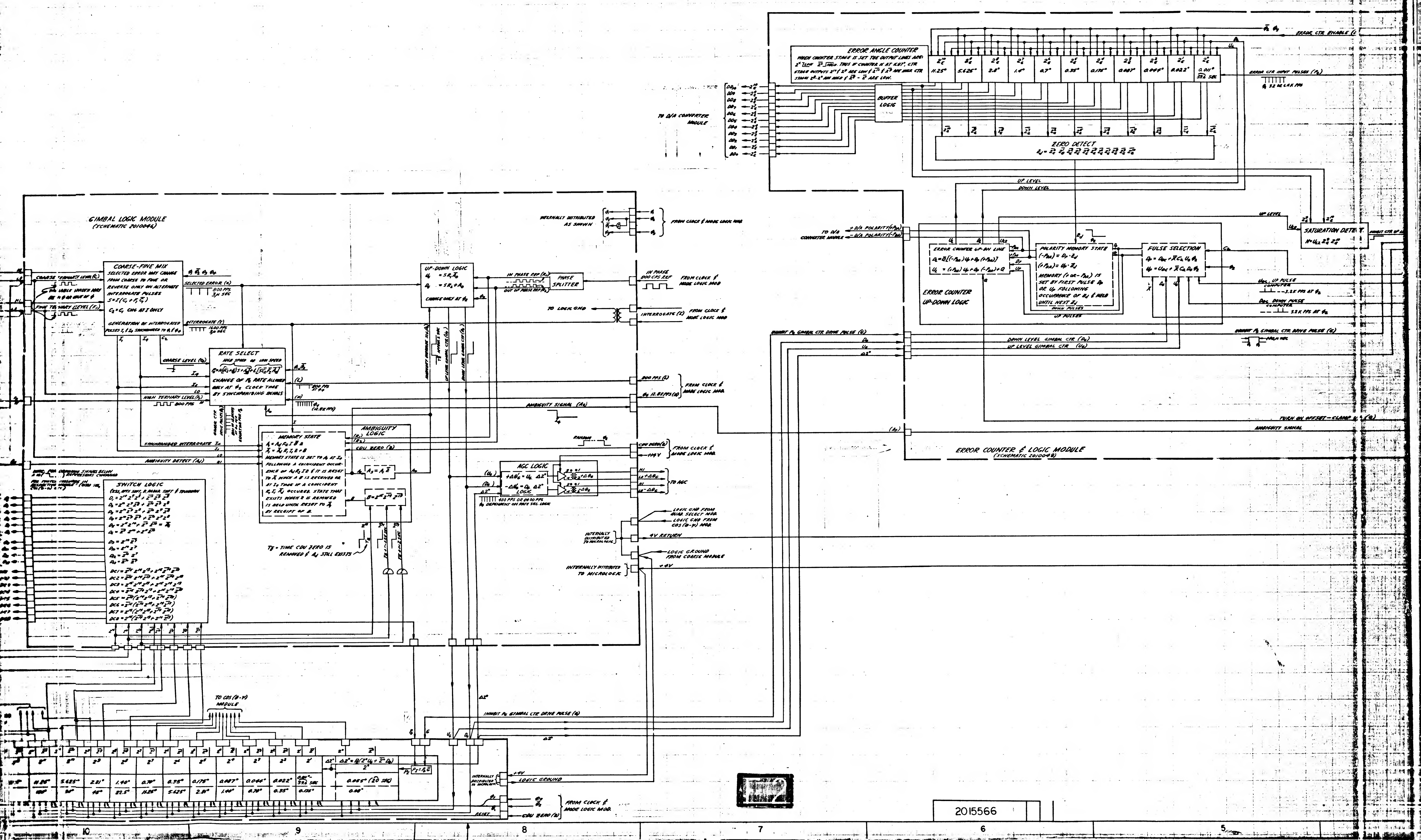

COARSE MODULE (SCHEMATIC 2010030) 42 PINS
(TO IMU 0°/DC) HI
TO PSA COARSE ALIGN MODULE
IMU CAGE
1X SINE θ RESOLVER
1X COS θ RESOLVER
800V ~ 1%
26:26
26:4
28:4
COS 22.5°
COS 67.5°
-COS 22.5°
-COS 67.5°
SIN 22.5°
SIN 67.5°
-SIN 22.5°
-SIN 67.5°
11.25°
5.62°
2.81°
A1
EMITTER FOLLOWER
COARSE ERROR SCHMITT
AMBIGUITY DETECT SCHMITT
1:1
1K
+28V DC
COARSE ERROR T.P. - SEE NOTE 3 TO CDU CONNECTOR
COARSE ERROR TO D/A CONVERTER MODULE AND DIGITAL MODE MODULE FAIL CIRCUIT
COARSE TERNARY LEVEL (C1) VARIABLE WIDTH
800 PPS
SIGNAL EXISTS FOR ERROR (θE) > 5°
AMBIGUITY DETECT (Ad)
(θG RANGE: 125° < θG < 235°) OUT OF PHASE
TO AMB LOGIC PART OF DIGITAL MODE MODULE
DC1 DC2 DC3 DC4 DC5 DC6 DC7 DC8 DC9 DC10 DC11 DC12
FROM READ COUNTER MODULE
LOGIC GND TO READ COUNTER MOD
TO D/A CONVERTER MODULE
SIGNAL GND
SIGNAL GND FROM MSA
(INPUT LO)
SEE NOTE 1
STRUCTURE GND
FROM INTERROGATE MODULE
INTERROGATE (I)
1600 PPS
SEE NOTE 3 - TO CDU CONNECTOR TP-C1
COARSE TERNARY LEVEL (C1)
SEE NOTE 3 - TO CDU CONNECTOR TP-F1
FROM MAIN SUMMING AMP & QUADRATURE REJECTION MOD
FINE TERNARY (F1) LEVEL
FROM DIGITAL MODE MODULE
I3
I2
SYNCHRONIZED INTERROGATE
SEE NOTE 3 - TO CDU CONNECTOR TP-F2
HIGH TERNARY LEVEL (F2)
FROM MODE MODULE
φ2
SEE NOTE 3 - TO CDU CONNECTOR
TP-P
800 OR 12.8 KPPS AT
QUADRANT SELECTOR MODULE (SCHEMATIC 2010059) 67 PINS
SEE NOTE 1
1X SIN θ RESOLVER
1X COS θ RESOLVER
16X SIN θ RESOLVER
16X COS θ RESOLVER
TO COARSE MODULE
FROM IMU OR R.R.
(SEE NOTE 4 REGARDING θ)
MODULE TEST POINTS
TP-A
TP-B
TP-C
30K
28V DC
A1 A2 A3 A4 A5 A6
S4 SIN θ — SIN 78 3/4°
S3 SIN θ — SIN 56 1/4°
S2 SIN θ — SIN 33 3/4°
S1 SIN θ — SIN 11 1/4°
S1 COS θ — COS 11 1/4°
S2 COS θ — COS 33 3/4°
S3 COS θ — COS 56 1/4°
COS 78 3/4°
TO D14 LOGIC GND
FROM LOGIC GND D1C
S9 -11.25°
S10 ΔK
S13 ΔK
S12 -11.25°
FROM READ COUNTER
LADDER AMP LO
SIGNAL GND
FROM READ COUNTER MODULE
LOGIC GND
S4 COS θ
S3 COS θ
S2 COS θ
S1 COS θ
FROM PSA DISTRIBUTION 28V DC
I.S.S. OR OPT
+28V DC TO A1-7 & D1-14
TO MSA
TO D/A CONV
TO COARSE MODULE
TO MODE MODULE
TO INTERROGATE
TO MODE MODULE
TO 4V P.S.
STRUCTURE GND
MAIN SUMMING QUADRATURE REJECTION (SCHEMATIC
LADDER AMP A-1
LADDER AMP LO
SIGNAL GROUND
TO 90° PHASE SHIFT LO
TO S20, S21, S22
TO S16, S18, S19
+28V
TO A1, A2
TO R14
TO D20, D21, D22
TO JCT D16, D18, D19
TO JCT D15, D17
TO JCT R82, R86
STRUCTURE GROUND
SEE NOTE 1
12
11
10
9
D
C
B
A
2015566
SHT 2


ERROR CTR ENABLE (E)
$\bar{\phi}_2$
D_L
U_L
2^{10}_E 11.25°
2^9_E 5.625°
2^8_E 2.8°
2^7_E 1.4°
2^6_E 0.7°
2^5_E 0.35°
2^4_E 0.175°
2^3_E 0.087°
2^2_E 0.044°
2^1_E 0.022°
2^0_E 0.011° 39.6 SEC
ERROR CTR INPUT PULSES (P_E)
ϕ_4 3.2 OR 6.4K PPS
ZERO DETECT
$Z_d = \bar{2}^0_E \bar{2}^1_E \bar{2}^2_E \bar{2}^3_E \bar{2}^4_E \bar{2}^5_E \bar{2}^6_E \bar{2}^7_E \bar{2}^8_E \bar{2}^9_E \bar{2}^{10}_E$
UP LEVEL
DOWN LEVEL
ERROR COUNTER UP-DN LINE
$D_L = \bar{Q}[(-P_{DA})U_P + D_P(+P_{DA})]$
$U_L = (+P_{DA})U_P + D_P(-P_{DA}) + Q$
ERROR COUNTER UP-DOWN LOGIC
U_{L2}
$-P_M$
$+P_M$
D_P
U_P
Z_d
ϕ_2
POLARITY MEMORY STATE
$(-P_{DA}) = D_P \cdot Z_d$
$(+P_{DA}) = U_P \cdot Z_d$
MEMORY (+ OR − P_{DA}) IS SET BY FIRST PULSE D_P OR U_P FOLLOWING OCCURRENCE OF Z_d & HELD UNTIL NEXT Z_d
DOWN PULSES
UP PULSES
PULSE SELECTION
$D_P = D_{OC} + \bar{X} C_2 U_G \phi_2$
$U_P = U_{OC} + \bar{X} C_2 D_G \phi_2$
C_2
$\bar{X}$
D_G
U_G
UP LEVEL
U_{L2}
2^9_E
2^{10}_E
SATURATION DETECT
$N = U_{L2} 2^9_E 2^{10}_E$
INHIBIT CTR UP LINE PULSES (N)
G
$\Delta 2°$
U_{OC}, UP PULSE COMPUTER
3.2K PPS AT ϕ_2
D_{OC} DOWN PULSE COMPUTER
3.2K PPS AT ϕ_2
INHIBIT P_E GIMBAL CTR DRIVE PULSE (G)
100μ SEC
DOWN LEVEL GIMBAL CTR (D_G)
UP LEVEL GIMBAL CTR (U_G)
(P_E)
PULSE SELECTION LOGIC
$G = C_2 \Delta\theta_{C2} (\phi_1 \rightarrow \phi_3)_C$
G IS SYNCHRONIZED BY ϕ_1 SO THAT G DURATION IS ϕ_1 THRU NEXT ϕ_1 FOLLOWING RECEIPT OF A $\Delta\theta_C$ PULSE
$P_E = E\bar{N}(\Delta\theta_{C2} + C_2 \Delta 2°) + Q_P$
($E\bar{N}\Delta\theta_{C2}$ SYNCHRONIZED BY $\bar{\phi}_1$ & ϕ_4). PULSES P_E ARE TRANSMITTED TO THE ERROR CTR INPUT AT ϕ_4 FOR $\Delta\theta_C$ MAX RATE OF 3.2K PPS OR 6.4K PPS MAX FOR $\Delta 2°$ PULSES
$\phi_4, \bar{\phi}_1$
$(\phi_1 \rightarrow \phi_3)_C$ GATE = X
$\Delta\theta_{C2}$
3.2K PPS AT ϕ_2
Q_P TURN ON OFFSET PULSES
12.8K PPS, ϕ_4
X
SINGLE PULSE SYNC
$\Delta\theta_{C2} = (+\Delta\theta_C) + (-\Delta\theta_C)$
SYNCHRONIZED SO THAT PULSE OCCURS AT ϕ_2 FOLLOWING RECEIPT OF A $\Delta\theta_C$ PULSE
$U_{OC} = +\Delta\theta_C$
$D_{OC} = -\Delta\theta_C$
SYNCHRONIZED SO PULSE OCCURS AT ϕ_2 FOLLOWING RECEIPT OF THE RESPECTIVE $\Delta\theta_C$ PULSE.
$(\phi_1 \rightarrow \phi_3)_C$ = X GATE SIGNAL SENT FOLLOWING RECEIPT OF $\Delta\theta_C$
ϕ_{1-4}
1
2
3
4
HI
$+\Delta\theta_C$
LO
HI
$-\Delta\theta_C$
LO
ϕ_4
$Q_P = Q\phi_4$
Q
$Q = A_S C_2 \bar{E}$
A_S
TURN ON OFFSET LOGIC
COARSE ALIGN ENABLE C_2
ERROR COUNTER ENABLE $\bar{E}$
TURN ON OFFSET ENABLE SIGNAL (Q)
TURN ON OFFSET—CLAMP UP (Q)
AMBIGUITY SIGNAL
ERROR COUNTER & LOGIC MODULE
(SCHEMATIC 2010048)
INTERNALLY DISTRIBUTED AS SHOWN
ϕ_1
$\bar{\phi}_1$
ϕ_2
$\bar{\phi}_2$
ϕ_3
ϕ_4
C_2
$\bar{E}$
Q
INTERNALLY DISTRIBUTED TO MICROLOGIC
LOGIC GROUND FROM D/A CONVERTER MOD.
4V RETURN
ERROR CTR ENABLE (E)
ϕ_2
RANDOM
TO GIMBAL LOGIC MODULE
TO GIMBAL LOGIC MODULE
TO GIMBAL ANGLE CTR MODULE
TO GIMBAL LOGIC MODULE
TO GIMBAL ANGLE CTR MODULE
TO GIMBAL LOGIC MODULE
TO GIMBAL LOGIC MODULE
+14V DC
12.8K PPS (ϕ_1 LEADS ϕ_2) ϕ_2 LEADS ϕ_3 ETC. 3μ SEC WIDTH APPROX
FROM CLOCK & MODE LOGIC MODULE
800 CPS REF 0° PHASE
HI
LO
INTERROGATE (I)
1600 PPS 3μ SEC WIDE
800 PPS AT ϕ_4 (L)
CDU ZERO (Z)
RANDOM
TO GIMBAL LOGIC MODULE
TO GIMBAL ANGLE ERROR CTR MODULE
COARSE ALIGN ENABLE (C_2)
ERROR COUNTER ENABLE ($\bar{E}$)
TURN ON OFFSET ENABLE SIGNAL (Q)
TO CLOCK & MODE LOGIC MODULE
$+\Delta\theta_C$
$-\Delta\theta_C$
FROM LGC
FROM GIMBAL LOGIC MODULE
HI
LO
$+\Delta\theta_G$
HI
LO
$-\Delta\theta_G$
TO LGC
+4V POWER SUPPLY HI FROM PSA
COS (θ−ψ) ∠90°
(USED ONLY FOR OPTICS TRUNNION CONNECTIONS)
4V POWER SUPPLY LO FROM PSA
SIGNAL GROUND RETURN FROM D/A CONVERTER MOD

DELINEATED ON THIS SHEET: COUPLING DATA UNIT (CDU) 2 WIRE MECH. FOR IMU & REND. RDR. SHAFT AXIS.

NEXT ASSY	USED ON	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS ± DECIMALS ± ANGLES ± DO NOT SCALE THIS DRAWING	M I T INSTRUMENTATION LAB CAMBRIDGE, MASS.	MANNED SPACECRAFT CENTER HOUSTON, TEXAS
APPLICATION		MATERIAL — HEAT TREATMENT — FINAL FINISH —	DRAWN THENO DATE 6-5-64 CHECKED J. Gilmore 6-12-64 APPROVAL J. Gilmore 6-28-64 APPROVAL John E. Miller 6-29-64 NASA APPROVAL MIT APPROVAL	(IMU/REND. RDR-SHAFT) CDU BLOCK DIAGRAM BLOCK II (2 LINE MECH)
				CODE IDENT NO. — SIZE J — NASA DRAWING NO. 2015566 SCALE — WT — SHEET 2 OF 2

MASTER


ERROR ANGLE COUNTER
WHEN COUNTER STAGE IS SET THE OUTPUT LINES ARE: 2^x LOW $\bar{2}^x$ HIGH. THUS IF COUNTER IS AT K.87°, CTR STAGE OUTPUTS 2^0 & 2^9 ARE LOW & $\bar{2}^{10}$ & $\bar{2}^9$ ARE HIGH. CTR STAGES 2^8-2^0 ARE HIGH & $\bar{2}^8$ - $\bar{2}^0$ ARE LOW.
11.25°
5.625°
2.8°
1.4°
0.7°
0.35°
0.175°
0.087°
0.044°
0.022°
0.011° 39.6 SEC
BUFFER LOGIC
ZERO DETECT
TO D/A CONVERTER MODULE
ERROR CTR ENABLE
ERROR CTR INPUT PULSES (P_E)
ϕ_1 3.2 OR 6.4K PPS
UP LEVEL
DOWN LEVEL
SATURATION DETECT
+ D/A POLARITY (+P_{DA})
− D/A POLARITY (−P_{DA})
ERROR COUNTER UP-DN LINE
$D_L = \bar{Z}[(-P_{DA})U_P + D_P(+P_{DA})]$
$U_L = (+P_{DA})U_P + D_P(-P_{DA}) + Q$
POLARITY MEMORY STATE
$(-P_{DA}) = D_P \cdot Z_d$
$(+P_{DA}) = U_P \cdot Z_d$
MEMORY (+ OR − P_{DA}) IS SET BY FIRST PULSE D_P OR U_P FOLLOWING OCCURRENCE OF Z_d & HELD UNTIL NEXT Z_d
DOWN PULSES
UP PULSES
FULSE SELECTION
$D_P = D_{OC} + \bar{X} C_2 U_G \phi_2$
$U_P = U_{OC} + \bar{X} C_2 D_G \phi_2$
ERROR COUNTER UP-DOWN LOGIC
U_{OC}, UP PULSE COMPUTER
3.2K PPS AT ϕ_2
D_{OC}, DOWN PULSE COMPUTER
3.2K PPS AT ϕ_2
INHIBIT P_G GIMBAL CTR DRIVE PULSE (G)
DOWN LEVEL GIMBAL CTR (D_G)
UP LEVEL GIMBAL CTR (U_G)
TURN ON OFFSET — CLAMP
AMBIGUITY SIGNAL
ERROR COUNTER & LOGIC MODULE (SCHEMATIC 2010048)
GIMBAL LOGIC MODULE (SCHEMATIC 2010046)
INTERNALLY DISTRIBUTED AS SHOWN
FROM CLOCK & MODE LOGIC MOD.
COARSE-FINE MIX
SELECTED ERROR MAY CHANGE FROM COARSE TO FINE OR REVERSE ONLY ON ALTERNATE INTERROGATE PULSES
$S = I(C_1 + F_1 \bar{C}_1)$
$C_2 = C_1$ CHG AT I ONLY
GENERATION OF INTERROGATED PULSES I, & I_4 SYNCHRONIZED TO ϕ_1 & ϕ_4
COARSE TERNARY LEVEL (C_1)
VARIABLE WIDTH MAY BE IN Φ OR OUT OF Φ
FINE TERNARY LEVEL (F_1)
SELECTED ERROR (S)
800 PPS 3μ SEC
INTERROGATE (I)
1600 PPS 3μ SEC
UP-DOWN LOGIC
$U_G = SR_1\bar{A}_0$
$D_G = SR_2 + A_0$
CHANGE ONLY AT ϕ_2
IN PHASE REF (R_1)
OUT OF PHASE REF (R_2)
PHASE SPLITTER
IN PHASE 800 CPS REF
TO LOGIC GND
INTERROGATE (I)
RATE SELECT
HIGH SPEED OR LOW SPEED
CHANGE OF P_G RATE ALLOWED ONLY AT ϕ_2 CLOCK TIME BY SYNCHRONIZING SIGNALS
COARSE LEVEL (C_2)
HIGH TERNARY LEVEL (F_2)
800 PPS
800 PPS AT ϕ_4
ϕ_4 (12.8K PPS)
800 PPS (L)
ϕ_4 12.8K PPS (H)
AMBIGUITY SIGNAL (A_S)
AMBIGUITY OVERRIDE SIG (A_0)
UP LEVEL GIMBAL CTR (U_G)
DOWN LEVEL GIMBAL CTR (D_G)
GIMBAL CTR DRIVE PULSES (P_G)
800 OR 12.8K PPS AT ϕ_4 PER EQUATION FOR P_G
SYNCHRONIZED INTERROGATE I_4
AMBIGUITY DETECT (A_d)
MEMORY STATE
$A_1 = A_d F_2 I \bar{B} \bar{Z}$
$\bar{A}_1 = \bar{A}_d R_1 I_4 Z + B$
MEMORY STATE IS SET TO A_1 AT I_4 FOLLOWING A COINCIDENT OCCURENCE OF $A_d R_2 I Z$ & IT IS RESET TO $\bar{A}_1$ WHEN A B IS RECEIVED OR AT I_4 TIME IF A COINCIDENT $R_1 I_4 \bar{A}_d$ OCCURED. STATE THAT EXISTS WHEN Z IS REMOVED IS HELD UNTIL RESET TO $\bar{A}_1$ BY RECEIPT OF B.
AMBIGUITY LOGIC
CDU ZERO (Z)
$A_S = A_1 \bar{Z}$
$B = 2^{15} \bar{2}^{14} \bar{2}^{13}$
T_Z = TIME CDU ZERO IS REMOVED & A_d STILL EXISTS
RANDOM
AGC LOGIC
$+\Delta\theta_G = U_G \Delta 2^0$
$-\Delta\theta_G = D_G \Delta 2^0$
400 PPS OR 6400 PPS ϕ_4 DEPENDENT ON RATE SEL. LOGIC
TO AGC
LOGIC GND FROM QUAD. SELECT MOD.
LOGIC GND FROM COS (θ-ψ) MOD.
INTERNALLY DISTRIBUTED TO MICROLOGIC
4V RETURN
LOGIC GROUND FROM COARSE MODULE
INTERNALLY DISTRIBUTED TO MICROLOGIC
+4V
SWITCH LOGIC
$D_1 = 2^{10} 2^9 2^8 + \bar{2}^{10} \bar{2}^9 2^8$
$D_5 = 2^{12} 2^{10} + \bar{2}^{12} \bar{2}^{10} = \bar{A}_2$
$DC1 = \bar{2}^{15} 2^{14} 2^{13} + 2^{15} \bar{2}^{14} \bar{2}^{13}$
$DC8 = 2^{15}(\bar{2}^{14} 2^{13} + 2^{14} \bar{2}^{13})$
TO COS (θ-ψ) MODULE
INHIBIT P_G GIMBAL CTR DRIVE PULSE (G)
$\Delta 2^0$
$\Delta 2^0 = P_I(2^0 U_G + \bar{2}^0 D_G)$
$P_I = P_G \bar{G}$
11.25°
5.625°
2.81°
1.40°
0.70°
0.35°
0.175°
0.087°
0.044°
0.022°
0.011° 39.6 SEC
0.055° (20 SEC)
90°
45°
22.5°
11.25°
5.625°
2.81°
1.40°
0.70°
0.35°
0.175°
LOGIC GROUND
RESET
CDU ZERO (Z)
FROM CLOCK & MODE LOGIC MOD.

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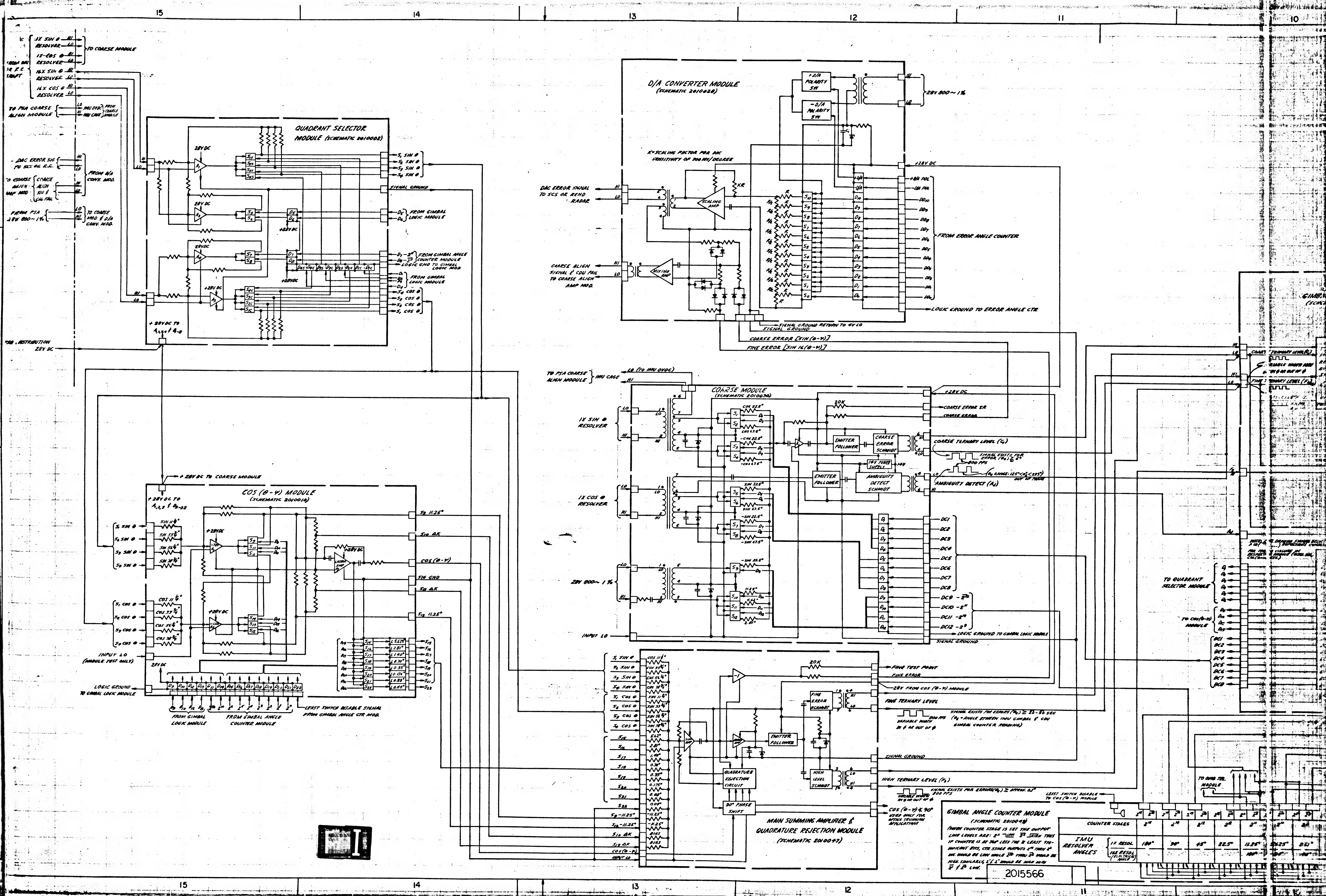


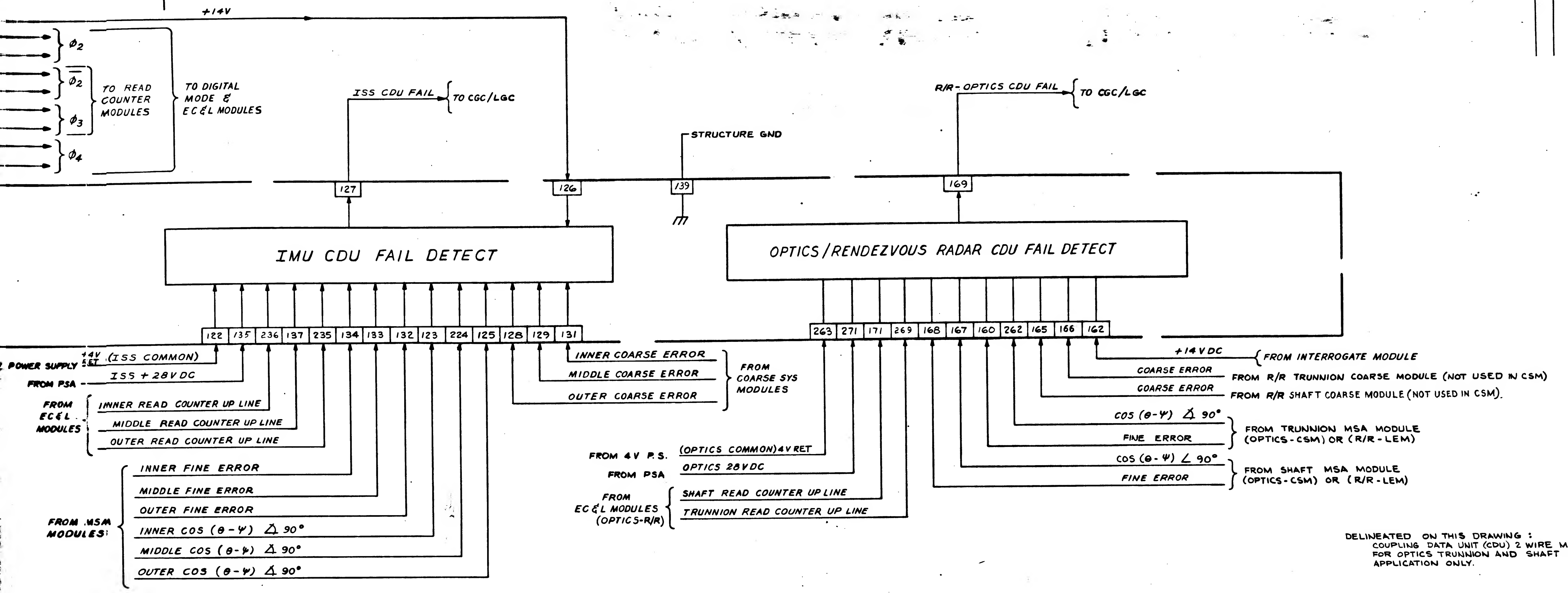
GIMBAL ANGLE COUNTER MODULE
(SCHEMATIC 2010048)

(WHEN COUNTER STAGE IS SET THE OUTPUT LINE LEVELS ARE: 2^x LOW $\overline{2^x}$ HIGH THUS IF COUNTER IS AT 360° LESS THE 2 LEAST SIGNIFICANT BITS, CTR STAGE OUTPUTS 2^{15} THRU 2^3 INC. WOULD BE LOW WHILE $\overline{2^{15}}$ THRU $\overline{2^3}$ WOULD BE HIGH. SIMILARLY, 2^1 & 2^0 WOULD BE HIGH WITH $\overline{2^1}$ & $\overline{2^0}$ LOW.

COUNTER STAGES		2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9
IMU RESOLVER ANGLES	1X RESOL.	180°	90°	45°	22.5°	11.25°	5.625°	2.81°
	16X RESOL (ELECTRICAL ANGLE)					180°	90°	45°

2015566

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL



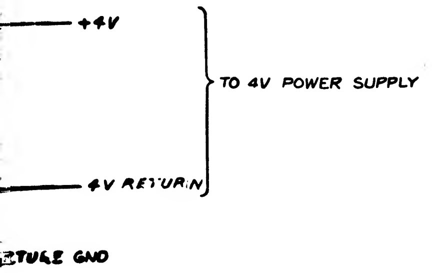
DELINEATED ON THIS DRAWING :
COUPLING DATA UNIT (CDU) 2 WIRE MECH APPLICABLE FOR OPTICS TRUNNION AND SHAFT AXIS CSM APPLICATION ONLY.

NOTES :

1. JUMPER CONNECTIONS MADE IN CDU HEADER TO INTERCONNECT INTERNAL MODULE CIRCUITRY. FOR DETAILS REFER TO CORRESPONDING MODULE SCHEMATIC.
2. STRUCTURE GROUND- TIE POINT TO WIRE WRAP HEADER ASSEMBLY.
3. SEE BLOCK II HEADER CONNECTOR DWG CSM 2010073, & LEM 6010001 FOR TEST POINT USAGE.
4. RESOLVER ANGLES θ AND SCALING DESIGNATIONS (ie. SIN 56¼°) SHOWN IN QUADRANT SELECT AND MSA MODULES, REP 16X & 64X RESOLVER OUTPUTS EXPRESSED IN ELECTRICAL DEGREES.
5. LINE OF SIGHT ANGLE IS EQUAL TO TWO TIMES THE MECHANICAL ANGLE.
6. AMBIGUITY LOGIC AND DETECTION NOT USED IN OPTICS TRUNNION APPLICATION.
7. SHEET 1, SHOWS THE OPTICS SHAFT & TRUNNION MODING, INTERROGATE FUNCTIONS, ETC. AND THE D/A FUNCTION. THE D/A FUNCTION IS IDENTICAL EXCEPT FOR SCALING.
   SHEET 2, SHOWS THE OPTICS TRUNNION A/D FUNCTION 2.5 $\widehat{SEC}$ MECHANICAL TRUNNION ANGLE LEAST SIGNIFICANT BIT.
   SHEET 3, SHOWS THE OPTICS SHAFT A/D FUNCTION 20 $\widehat{SEC}$ MECHANICAL SHAFT ANGLE LEAST SIGNIFICANT BIT.
8. COMPUTER PULSE WEIGHT OPTICS CDU - CGC.
   A) OPTICS OPERATION SHAFT (MECHANICAL):
      $\pm\Delta\theta_G$ (CDU TO CGC) $\simeq$ 40 $\widehat{SEC}$
      $\pm\Delta\theta_C$ (CGC TO CDU) $\cong$ 160 $\widehat{SEC}$
   TRUNNION (LINE OF SIGHT):
      $\pm\Delta\theta_G$ (CDU TO CGC) $\simeq$ 10 $\widehat{SEC}$
      $\pm\Delta\theta_C$ (CGC TO CDU) $\simeq$ 40 $\widehat{SEC}$
   B) TVC OPERATION: (USING D/A DC ERROR SIGNALS)
      PITCH SPS ENGINE GIMBAL (SHAFT D/A): $\pm\Delta\theta_C$ (CGC TO CDU) $\simeq$ 160 $\widehat{SEC}$
      YAW SPS ENGINE GIMBAL (TRUNNION D/A): $\pm\Delta\theta_C$ (CGC TO CDU) $\simeq$ 160 $\widehat{SEC}$

ABBREVIATIONS :

1. CDU - COUPLING DATA UNIT.
2. CGC - COMMAND MODULE GUIDANCE COMPUTER.
3. CSM - COMMAND AND SERVICE MODULE.
4. FB - FEEDBACK
5. FDAI - FLIGHT DIRECTOR ATTITUDE INDICATOR
6. G&C - GUIDANCE & CONTROL
7. ISS - INERTIAL SUB SYSTEM
8. LEM - LUNAR EXCURSION MODULE
9. LGC - LEM GUIDANCE COMPUTER
10. PSA - POWER & SERVO ASSEMBLY
11. R/R - RENDEVOUS RADAR
12. S/C - SPACE CRAFT
13. SPS - SERVICE PROPULSION
14. TVC - THRUST VECTOR CONTROL
15. MV - MILLIVOLTS
16. TY - TIE POINT FOR WIRE-WRAP INTERCONNECT
17. NC - NO CONNECTION



6

NEXT ASSY	USED ON	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS — DECIMALS — ANGLES —	MIT INSTRUMENTATION LAB CAMBRIDGE MASS
APPLICATION		DO NOT SCALE THIS DRAWING	DRAWN J Koss DATE 3-8-64
		MATERIAL —	CHECKED J Gilmore 3-12-65
		HEAT TREATMENT —	APPROVAL J Gilmore 3-19-65
		FINAL FINISH —	APPROVAL 3-19-65
			NASA APPROVAL 3-29-65
			MIT APPROVAL 23 Mar 65

MANNED SPACECRAFT CENTER
HOUSTON, TEXAS

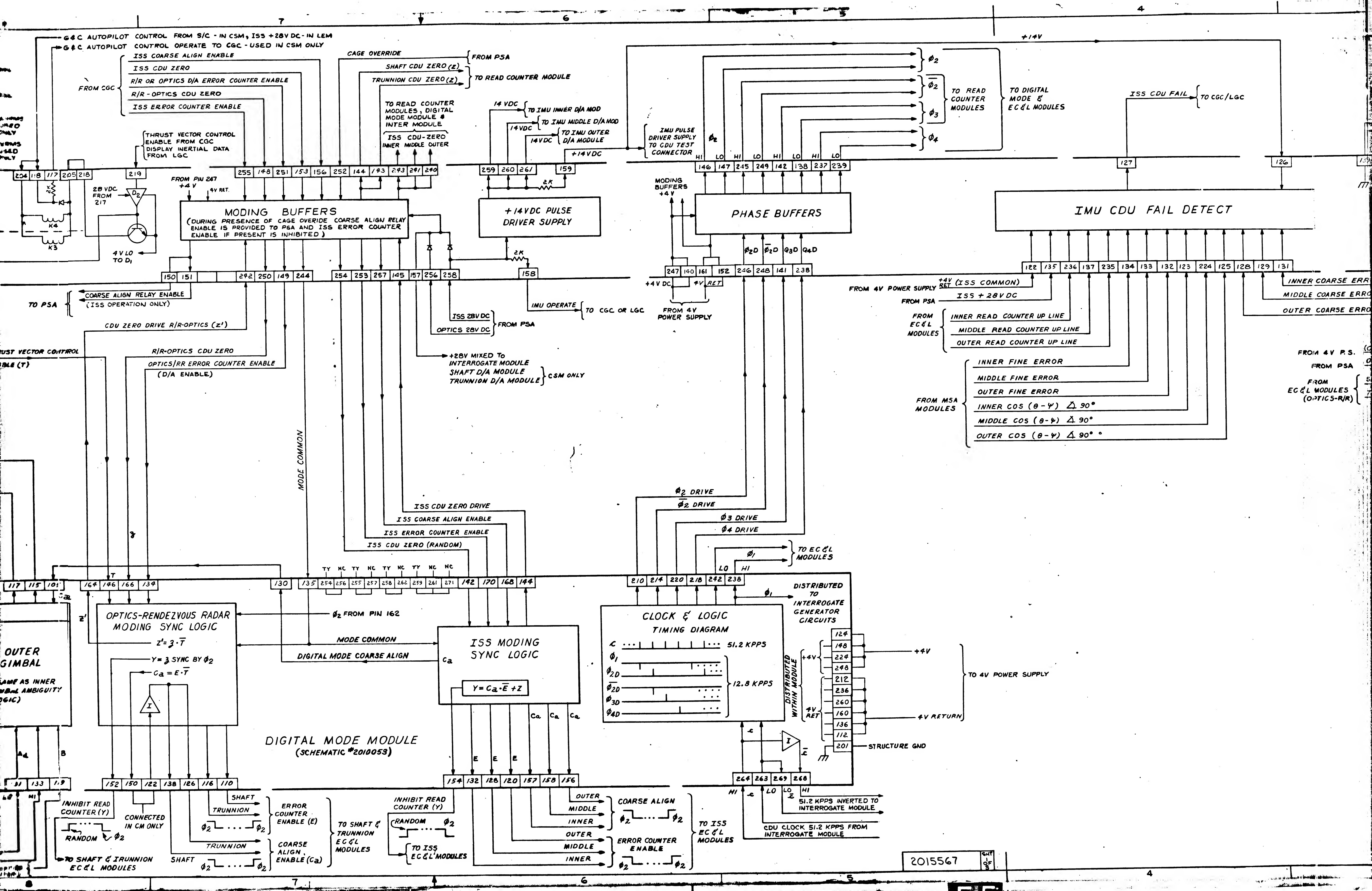
OPTICS TRUNNION & SHAFT
CDU BLOCK DIAGRAM
BLOCK II (2 LINE MECH)

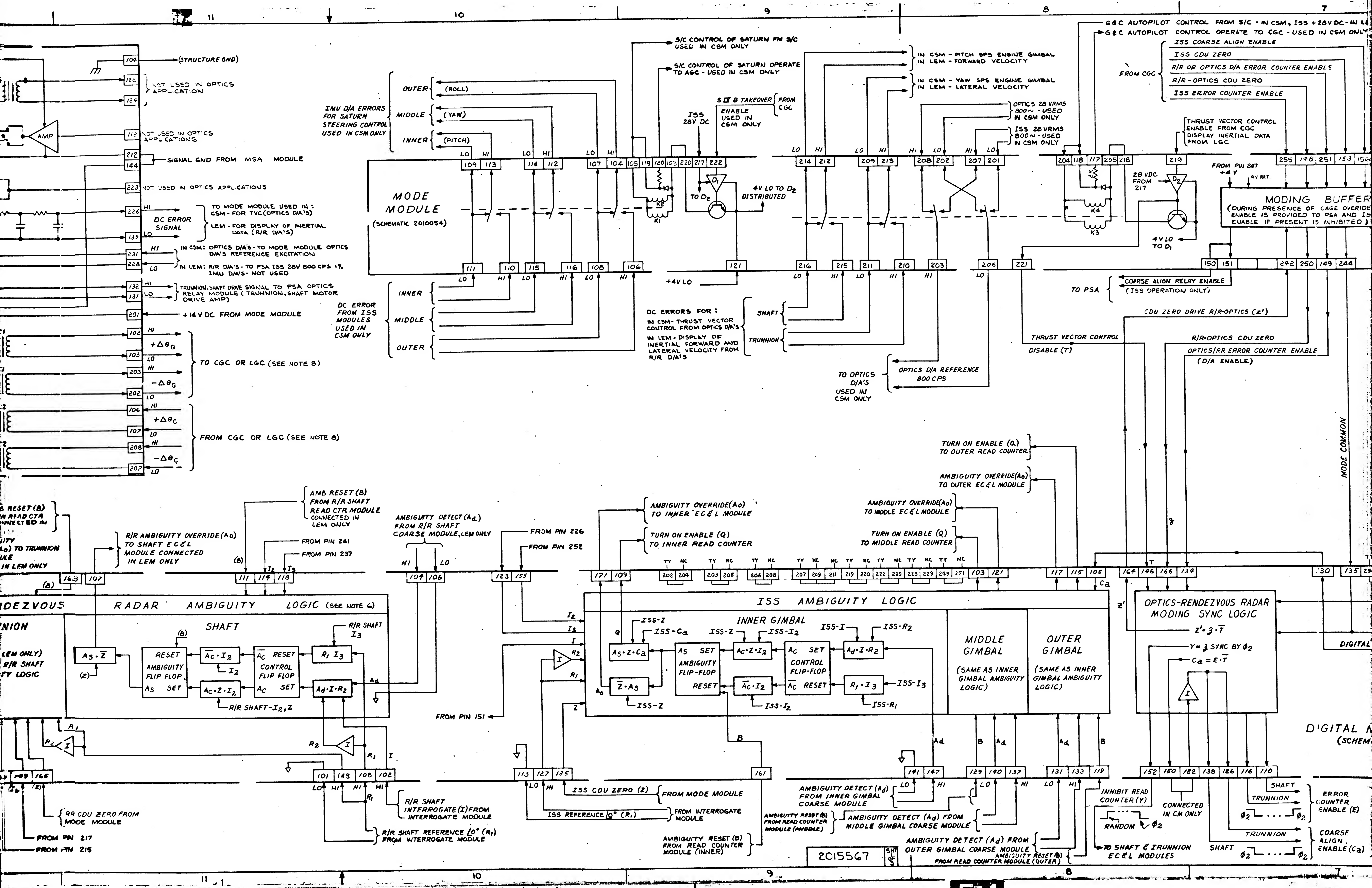
CODE IDENT NO	SIZE	NASA DRAWING NO
	J	2015567
SCALE —	WT	SHEET 1 OF 3

20'5567 SHT 1 OF 3

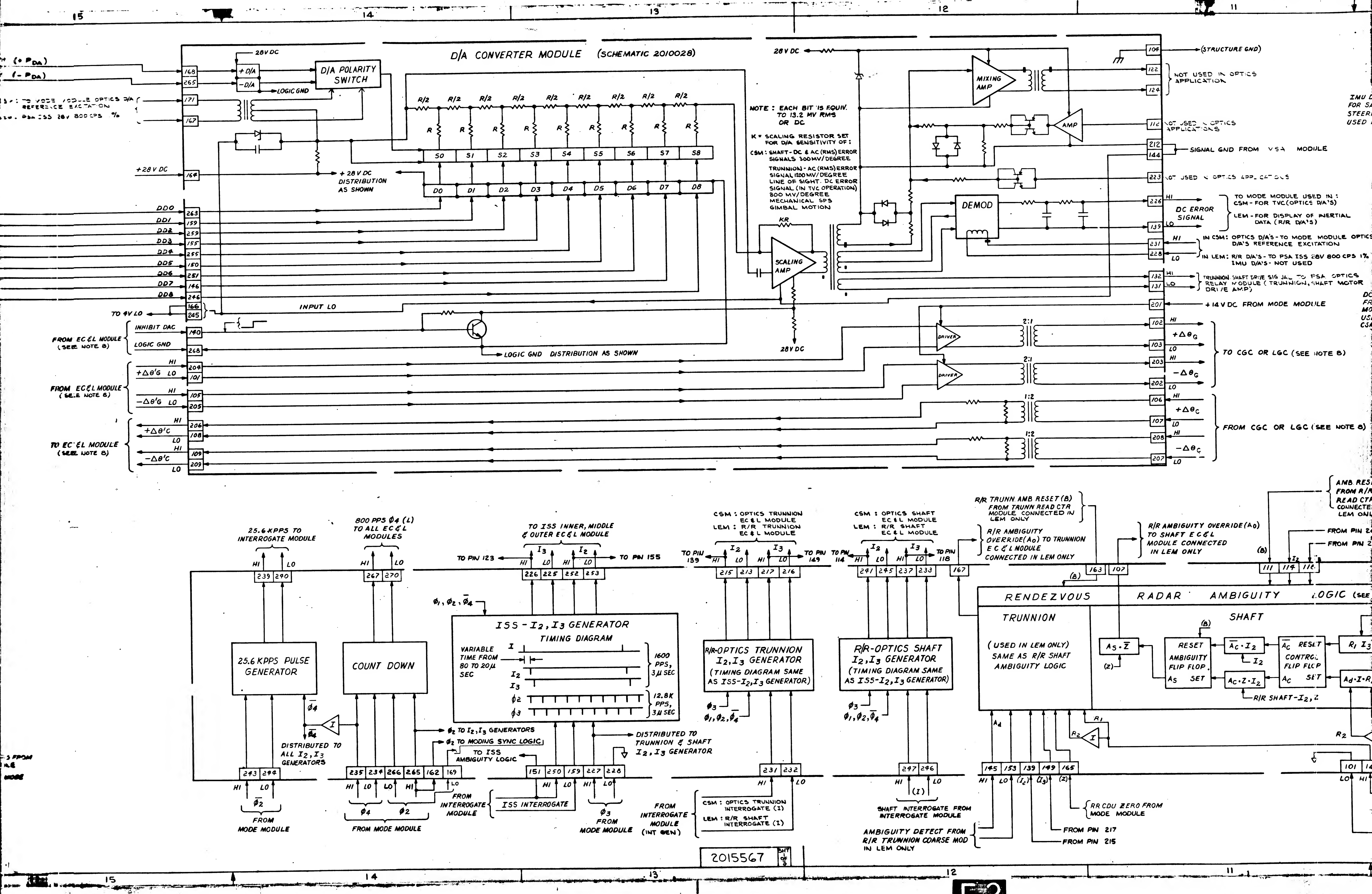
GILMORE

E-6


G&C AUTOPILOT CONTROL FROM S/C - IN CSM, ISS +28V DC - IN LEM
G&C AUTOPILOT CONTROL OPERATE TO CGC - USED IN CSM ONLY
ISS COARSE ALIGN ENABLE
ISS CDU ZERO
R/R OR OPTICS D/A ERROR COUNTER ENABLE
R/R - OPTICS CDU ZERO
ISS ERROR COUNTER ENABLE
FROM CGC
THRUST VECTOR CONTROL ENABLE FROM CGC
DISPLAY INERTIAL DATA FROM LGC
CAGE OVERRIDE
FROM PSA
SHAFT CDU ZERO (Z)
TRUNNION CDU ZERO (Z)
TO READ COUNTER MODULE
TO READ COUNTER MODULES, DIGITAL MODE MODULE & INTER MODULE
ISS CDU-ZERO
INNER MIDDLE OUTER
14 VDC
TO IMU INNER D/A MOD
TO IMU MIDDLE D/A MOD
TO IMU OUTER D/A MODULE
+14VDC
IMU PULSE DRIVER SUPPLY TO CDU TEST CONNECTOR
+14V
TO READ COUNTER MODULES
TO DIGITAL MODE & EC&L MODULES
ISS CDU FAIL
TO CGC/LGC
28 VDC FROM 217
FROM PIN 247 +4V
4V RET
4V LO TO D1
K4
K3
MODING BUFFERS
(DURING PRESENCE OF CAGE OVERIDE COARSE ALIGN RELAY ENABLE IS PROVIDED TO PSA AND ISS ERROR COUNTER ENABLE IF PRESENT IS INHIBITED)
+14VDC PULSE DRIVER SUPPLY
2K
MODING BUFFERS +4V
PHASE BUFFERS
IMU CDU FAIL DETECT
TO PSA
COARSE ALIGN RELAY ENABLE (ISS OPERATION ONLY)
CDU ZERO DRIVE R/R-OPTICS (Z')
THRUST VECTOR CONTROL ENABLE (T)
R/R-OPTICS CDU ZERO
OPTICS/RR ERROR COUNTER ENABLE (D/A ENABLE)
ISS 28V DC
OPTICS 28V DC
FROM PSA
IMU OPERATE
TO CGC OR LGC
+28V MIXED TO INTERROGATE MODULE
SHAFT D/A MODULE
TRUNNION D/A MODULE
CSM ONLY
+4V DC
4V RET
FROM 4V POWER SUPPLY
FROM 4V POWER SUPPLY
+4V RET (ISS COMMON)
FROM PSA
ISS +28VDC
FROM EC&L MODULES
INNER READ COUNTER UP LINE
MIDDLE READ COUNTER UP LINE
OUTER READ COUNTER UP LINE
FROM MSA MODULES
INNER FINE ERROR
MIDDLE FINE ERROR
OUTER FINE ERROR
INNER COS (θ-ψ) Δ 90°
MIDDLE COS (θ-ψ) Δ 90°
OUTER COS (θ-ψ) Δ 90°
INNER COARSE ERR
MIDDLE COARSE ERRO
OUTER COARSE ERRO
FROM 4V P.S.
FROM PSA
FROM EC&L MODULES (OPTICS-R/R)
MODE COMMON
ISS CDU ZERO DRIVE
ISS COARSE ALIGN ENABLE
ISS ERROR COUNTER ENABLE
ISS CDU ZERO (RANDOM)
φ2 DRIVE
φ̄2 DRIVE
φ3 DRIVE
φ4 DRIVE
φ1
TO EC&L MODULES
TY NC TY NC TY NC TY NC NC
OUTER GIMBAL
(SAME AS INNER GIMBAL AMBIGUITY LOGIC)
OPTICS-RENDEZVOUS RADAR MODING SYNC LOGIC
Z' = 3·T̄
Y = 3 SYNC BY φ2
Ca = E·T̄
φ2 FROM PIN 162
MODE COMMON
DIGITAL MODE COARSE ALIGN
ISS MODING SYNC LOGIC
Y = Ca·Ē + Z
CLOCK & LOGIC
TIMING DIAGRAM
51.2 KPPS
12.8 KPPS
DISTRIBUTED TO INTERROGATE GENERATOR CIRCUITS
DISTRIBUTED WITHIN MODULE
+4V
4V RET
+4V
4V RETURN
TO 4V POWER SUPPLY
STRUCTURE GND
DIGITAL MODE MODULE
(SCHEMATIC #2010053)
INHIBIT READ COUNTER (Y)
RANDOM φ2
CONNECTED IN CM ONLY
TO SHAFT & TRUNNION EC&L MODULES
SHAFT
TRUNNION
ERROR COUNTER ENABLE (E)
COARSE ALIGN ENABLE (Ca)
TO SHAFT & TRUNNION EC&L MODULES
INHIBIT READ COUNTER (Y)
RANDOM
TO ISS EC&L MODULES
OUTER
MIDDLE
INNER
COARSE ALIGN
ERROR COUNTER ENABLE
TO ISS EC&L MODULES
51.2 KPPS INVERTED TO INTERROGATE MODULE
CDU CLOCK 51.2 KPPS FROM INTERROGATE MODULE
HI LO
2015567
E5
7
6
5
4



11
10
9
8
7
(STRUCTURE GND)
NOT USED IN OPTICS APPLICATION
AMP
NOT USED IN OPTICS APPLICATIONS
SIGNAL GND FROM MSA MODULE
NOT USED IN OPTICS APPLICATIONS
DC ERROR SIGNAL
TO MODE MODULE USED IN: CSM - FOR TVC (OPTICS D/A'S)
LEM - FOR DISPLAY OF INERTIAL DATA (R/R D/A'S)
IN CSM: OPTICS D/A'S - TO MODE MODULE OPTICS D/A'S REFERENCE EXCITATION
IN LEM: R/R D/A'S - TO PSA ISS 28V 800 CPS 1% IMU D/A'S - NOT USED
TRUNNION, SHAFT DRIVE SIGNAL TO PSA OPTICS RELAY MODULE (TRUNNION, SHAFT MOTOR DRIVE AMP)
+14 V DC FROM MODE MODULE
+Δθ_G
-Δθ_G
TO CGC OR LGC (SEE NOTE 8)
+Δθ_C
-Δθ_C
FROM CGC OR LGC (SEE NOTE 8)
IMU D/A ERRORS FOR SATURN STEERING CONTROL USED IN CSM ONLY
OUTER (ROLL)
MIDDLE (YAW)
INNER (PITCH)
MODE MODULE
(SCHEMATIC 2010054)
DC ERROR FROM ISS MODULES USED IN CSM ONLY
INNER
MIDDLE
OUTER
S/C CONTROL OF SATURN FM S/C USED IN CSM ONLY
S/C CONTROL OF SATURN OPERATE TO AGC - USED IN CSM ONLY
S IV B TAKEOVER ENABLE USED IN CSM ONLY
FROM CGC
ISS 28V DC
TO D2
4V LO TO D2 DISTRIBUTED
K1
K2
+4V LO
DC ERRORS FOR:
IN CSM - THRUST VECTOR CONTROL FROM OPTICS D/A'S
IN LEM - DISPLAY OF INERTIAL FORWARD AND LATERAL VELOCITY FROM R/R D/A'S
SHAFT
TRUNNION
IN CSM - PITCH SPS ENGINE GIMBAL
IN LEM - FORWARD VELOCITY
IN CSM - YAW SPS ENGINE GIMBAL
IN LEM - LATERAL VELOCITY
OPTICS 28 VRMS 800~ - USED IN CSM ONLY
ISS 28 VRMS 800~ - USED IN CSM ONLY
TO OPTICS D/A'S USED IN CSM ONLY
OPTICS D/A REFERENCE 800 CPS
G&C AUTOPILOT CONTROL FROM S/C - IN CSM, ISS +28V DC - IN LE
G&C AUTOPILOT CONTROL OPERATE TO CGC - USED IN CSM ONLY
ISS COARSE ALIGN ENABLE
ISS CDU ZERO
R/R OR OPTICS D/A ERROR COUNTER ENABLE
R/R - OPTICS CDU ZERO
ISS ERROR COUNTER ENABLE
FROM CGC
THRUST VECTOR CONTROL ENABLE FROM CGC
DISPLAY INERTIAL DATA FROM LGC
28 VDC FROM 217
K3
K4
4V LO TO D1
FROM PIN 247 +4V
4V RET
MODING BUFFER
(DURING PRESENCE OF CAGE OVERIDE ENABLE IS PROVIDED TO PSA AND IS ENABLE IF PRESENT IS INHIBITED)
TO PSA
COARSE ALIGN RELAY ENABLE (ISS OPERATION ONLY)
CDU ZERO DRIVE R/R-OPTICS (Z')
THRUST VECTOR CONTROL DISABLE (T)
R/R-OPTICS CDU ZERO
OPTICS/RR ERROR COUNTER ENABLE (D/A ENABLE)
MODE COMMON
TURN ON ENABLE (Q) TO OUTER READ COUNTER
AMBIGUITY OVERRIDE (A0) TO OUTER EC&L MODULE
AMBIGUITY OVERRIDE (A0) TO INNER EC&L MODULE
AMBIGUITY OVERRIDE (A0) TO MIDDLE EC&L MODULE
TURN ON ENABLE (Q) TO INNER READ COUNTER
TURN ON ENABLE (Q) TO MIDDLE READ COUNTER
AMB RESET (B) FROM R/R SHAFT READ CTR MODULE CONNECTED IN LEM ONLY
R/R AMBIGUITY OVERRIDE (A0) TO SHAFT EC&L MODULE CONNECTED IN LEM ONLY
AMBIGUITY DETECT (Ad) FROM R/R SHAFT COARSE MODULE, LEM ONLY
FROM PIN 241
FROM PIN 237
FROM PIN 226
FROM PIN 252
RENDEZVOUS RADAR AMBIGUITY LOGIC (SEE NOTE 6)
TRUNNION
(LEM ONLY) R/R SHAFT AMBIGUITY LOGIC
SHAFT
RESET AMBIGUITY FLIP FLOP
CONTROL FLIP FLOP
R/R SHAFT I3
R/R SHAFT-I2, Z
ISS AMBIGUITY LOGIC
INNER GIMBAL
AMBIGUITY FLIP-FLOP
CONTROL FLIP-FLOP
MIDDLE GIMBAL (SAME AS INNER GIMBAL AMBIGUITY LOGIC)
OUTER GIMBAL (SAME AS INNER GIMBAL AMBIGUITY LOGIC)
OPTICS-RENDEZVOUS RADAR MODING SYNC LOGIC
Z' = 3·T
Y = 3 SYNC BY φ2
Ca = E·T
DIGITAL
DIGITAL M (SCHEM
FROM PIN 151
RR CDU ZERO FROM MODE MODULE
FROM PIN 217
FROM PIN 215
R/R SHAFT INTERROGATE (I) FROM INTERROGATE MODULE
R/R SHAFT REFERENCE /0° (R1) FROM INTERROGATE MODULE
ISS CDU ZERO (Z) FROM MODE MODULE
ISS REFERENCE /0° (R1) FROM INTERROGATE MODULE
AMBIGUITY RESET (B) FROM READ COUNTER MODULE (INNER)
AMBIGUITY DETECT (Ad) FROM INNER GIMBAL COARSE MODULE
AMBIGUITY RESET (B) FROM READ COUNTER MODULE (MIDDLE)
AMBIGUITY DETECT (Ad) FROM MIDDLE GIMBAL COARSE MODULE
AMBIGUITY DETECT (Ad) FROM OUTER GIMBAL COARSE MODULE
AMBIGUITY RESET (B) FROM READ COUNTER MODULE (OUTER)
INHIBIT READ COUNTER (Y)
RANDOM φ2
CONNECTED IN CM ONLY
TO SHAFT & TRUNNION EC&L MODULES
SHAFT
TRUNNION
ERROR COUNTER ENABLE (E)
COARSE ALIGN ENABLE (Ca)
2015567
SHT 1 OF 5
E-4


15
14
13
12
11
D/A CONVERTER MODULE (SCHEMATIC 2010028)
(+ P_DA)
(- P_DA)
28 V DC
+D/A
-D/A
D/A POLARITY SWITCH
LOGIC GND
+28 V DC
+28 V DC DISTRIBUTION AS SHOWN
R/2
R
S0 S1 S2 S3 S4 S5 S6 S7 S8
D0 D1 D2 D3 D4 D5 D6 D7 D8
DD0 DD1 DD2 DD3 DD4 DD5 DD6 DD7 DD8
TO 4V LO
INPUT LO
FROM EC&L MODULE (SEE NOTE 8)
INHIBIT DAC
LOGIC GND
LOGIC GND DISTRIBUTION AS SHOWN
+Δθ'G
-Δθ'G
+Δθ'C
-Δθ'C
TO EC&L MODULE (SEE NOTE 8)
HI
LO
NOTE: EACH BIT IS EQUIV. TO 13.2 MV RMS OR DC
K = SCALING RESISTOR SET FOR D/A SENSITIVITY OF:
CSM: SHAFT-DC & AC (RMS) ERROR SIGNALS 300MV/DEGREE
TRUNNION-AC (RMS) ERROR SIGNAL 1200MV/DEGREE
LINE OF SIGHT, DC ERROR SIGNAL (IN TVC OPERATION) 800 MV/DEGREE
MECHANICAL SPS GIMBAL MOTION
KR
SCALING AMP
28 V DC
MIXING AMP
AMP
DEMOD
DRIVER
2:1
1:2
STRUCTURE GND
NOT USED IN OPTICS APPLICATION
NOT USED IN OPTICS APPLICATIONS
SIGNAL GND FROM VSA MODULE
NOT USED IN OPTICS APPLICATIONS
DC ERROR SIGNAL
TO MODE MODULE USED IN: CSM - FOR TVC (OPTICS D/A'S)
LEM - FOR DISPLAY OF INERTIAL DATA (R/R D/A'S)
IN CSM: OPTICS D/A'S - TO MODE MODULE OPTICS D/A'S REFERENCE EXCITATION
IN LEM: R/R D/A'S - TO PSA ISS 28V 800 CPS 1%
IMU D/A'S - NOT USED
TRUNNION SHAFT DRIVE SIG. JAL. TO PSA OPTICS RELAY MODULE (TRUNNION, SHAFT MOTOR DRIVE AMP)
+14 V DC FROM MODE MODULE
+Δθ_G
-Δθ_G
+Δθ_C
-Δθ_C
TO CGC OR LGC (SEE NOTE 8)
FROM CGC OR LGC (SEE NOTE 8)
25.6 KPPS TO INTERROGATE MODULE
25.6 KPPS PULSE GENERATOR
φ4
DISTRIBUTED TO ALL I2, I3 GENERATORS
φ2
FROM MODE MODULE
800 PPS φ4 (L) TO ALL EC&L MODULES
COUNT DOWN
φ4
φ2
FROM MODE MODULE
φ2 TO I2, I3 GENERATORS
φ2 TO MODING SYNC LOGIC
TO ISS AMBIGUITY LOGIC
FROM INTERROGATE MODULE
ISS INTERROGATE
TO ISS INNER, MIDDLE & OUTER EC&L MODULE
TO PIN 123
TO PIN 155
φ1, φ2, φ̄4
ISS - I2, I3 GENERATOR
TIMING DIAGRAM
VARIABLE TIME FROM 80 TO 20μ SEC
1600 PPS, 3μ SEC
12.8K PPS, 3μ SEC
DISTRIBUTED TO TRUNNION & SHAFT I2, I3 GENERATOR
φ3 FROM MODE MODULE
CSM: OPTICS TRUNNION EC&L MODULE
LEM: R/R TRUNNION EC&L MODULE
TO PIN 139
TO PIN 149
R/R-OPTICS TRUNNION I2, I3 GENERATOR (TIMING DIAGRAM SAME AS ISS-I2, I3 GENERATOR)
FROM INTERROGATE MODULE (INT GEN)
CSM: OPTICS TRUNNION INTERROGATE (I)
LEM: R/R SHAFT INTERROGATE (I)
CSM: OPTICS SHAFT EC&L MODULE
LEM: R/R SHAFT EC&L MODULE
TO PIN 114
TO PIN 118
R/R-OPTICS SHAFT I2, I3 GENERATOR (TIMING DIAGRAM SAME AS ISS-I2, I3 GENERATOR)
SHAFT INTERROGATE FROM INTERROGATE MODULE
AMBIGUITY DETECT FROM R/R TRUNNION COARSE MOD IN LEM ONLY
R/R TRUNN AMB RESET (B) FROM TRUNN READ CTR MODULE CONNECTED IN LEM ONLY
R/R AMBIGUITY OVERRIDE (A0) TO TRUNNION EC&L MODULE CONNECTED IN LEM ONLY
R/R AMBIGUITY OVERRIDE (A0) TO SHAFT EC&L MODULE CONNECTED IN LEM ONLY
RENDEZVOUS RADAR AMBIGUITY LOGIC
TRUNNION
(USED IN LEM ONLY) SAME AS R/R SHAFT AMBIGUITY LOGIC
SHAFT
RESET AMBIGUITY FLIP FLOP
AS SET
RESET CONTROL FLIP FLOP
R/R SHAFT-I2
RR CDU ZERO FROM MODE MODULE
FROM PIN 217
FROM PIN 215
FROM PIN
AMB RESET FROM R/R READ CTR CONNECTED LEM ONLY

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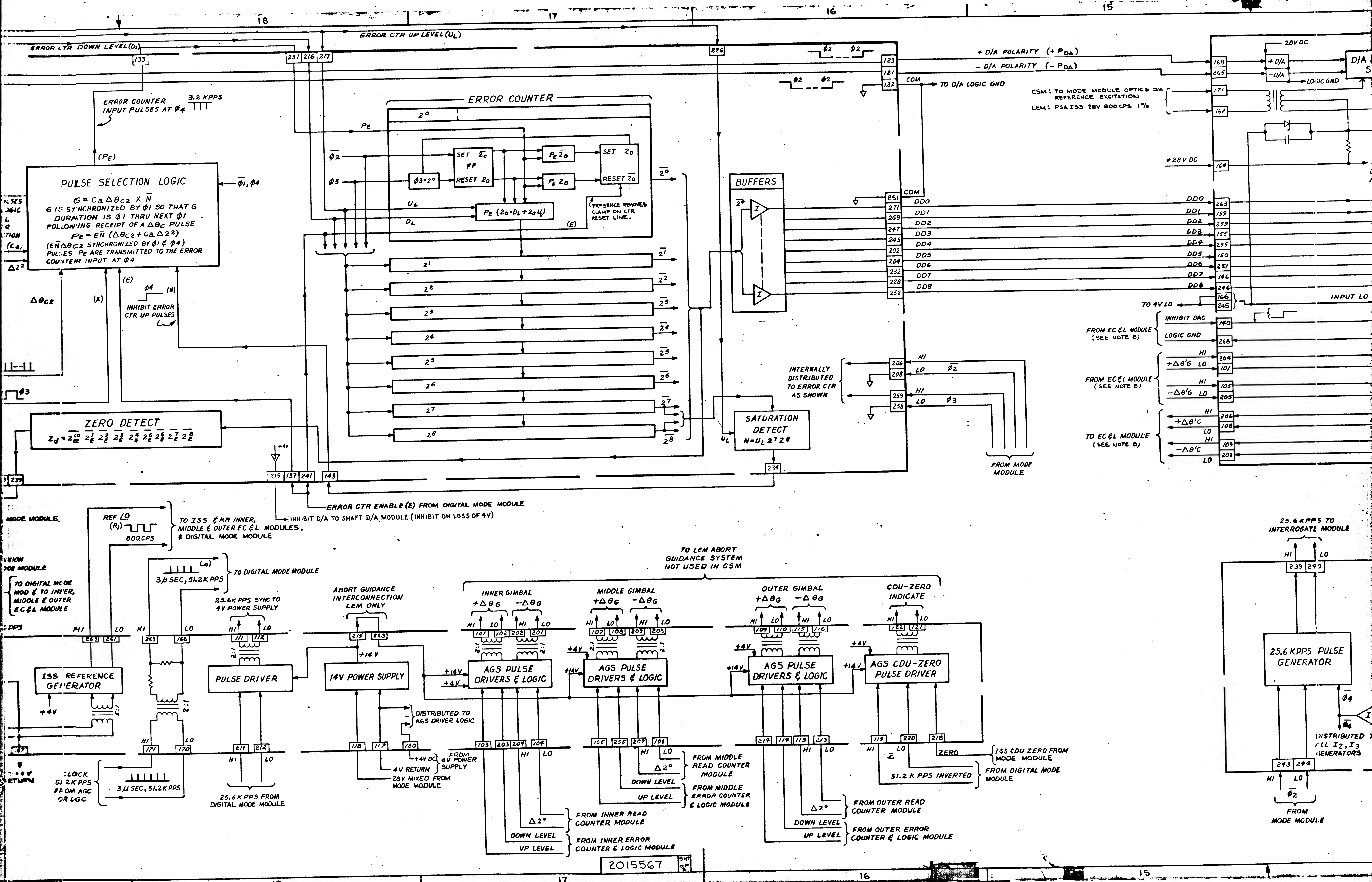
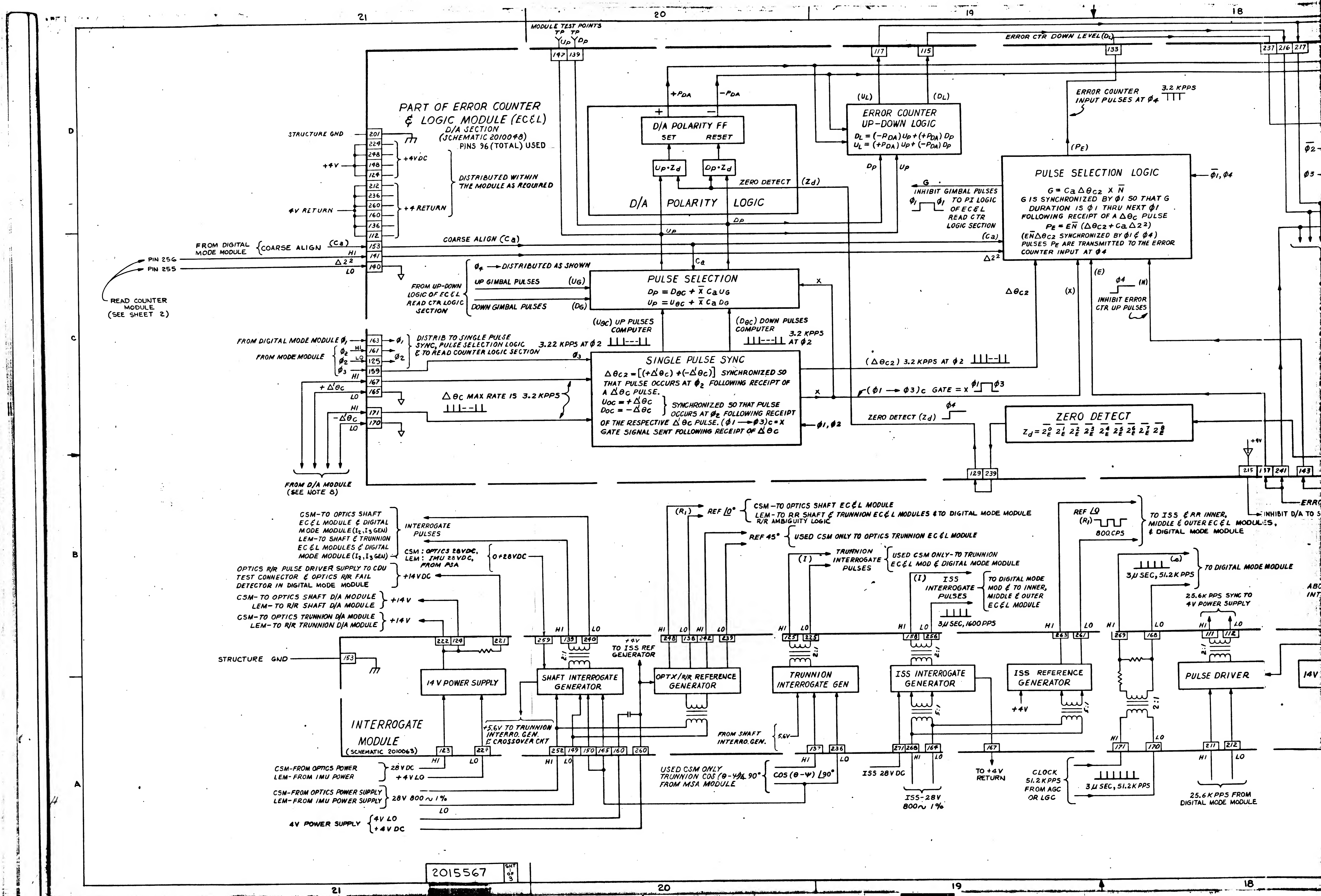
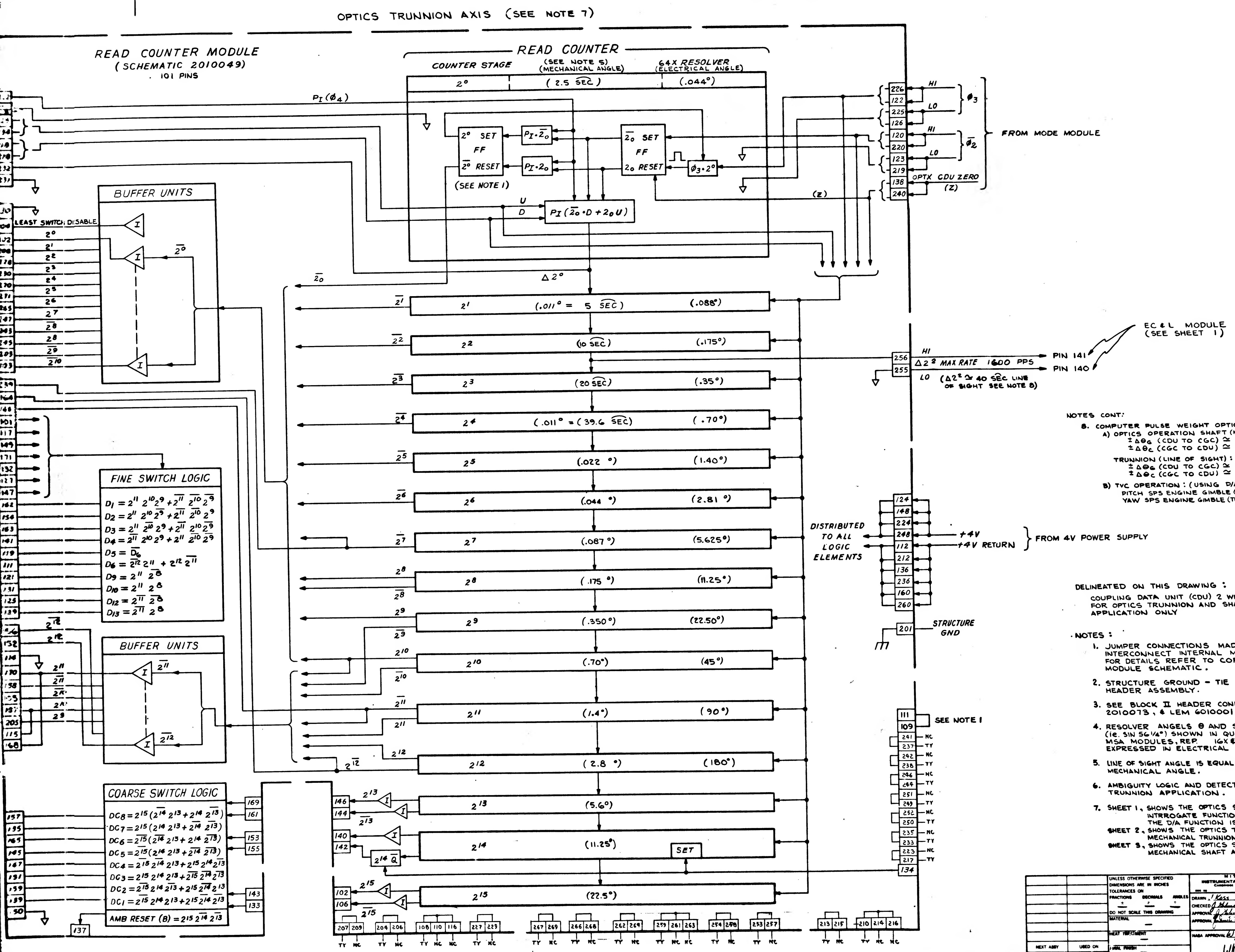
E3


18
17
16
15
ERROR CTR DOWN LEVEL (D_L)
ERROR CTR UP LEVEL (U_L)
133
237 216 217
226
ERROR COUNTER INPUT PULSES AT $\phi 4$
3.2 KPPS
(P_E)
PULSE SELECTION LOGIC
$G = C_a \Delta\theta_{C2} \times \overline{N}$
G IS SYNCHRONIZED BY $\phi 1$ SO THAT G DURATION IS $\phi 1$ THRU NEXT $\phi 1$ FOLLOWING RECEIPT OF A $\Delta\theta_C$ PULSE
$P_E = E\overline{N} (\Delta\theta_{C2} + C_a \Delta 2^2)$
($E\overline{N}\Delta\theta_{C2}$ SYNCHRONIZED BY $\phi 1$ & $\phi 4$)
PULSES P_E ARE TRANSMITTED TO THE ERROR COUNTER INPUT AT $\phi 4$
$\overline{\phi 1}, \phi 4$
$\Delta 2^2$
$\Delta\theta_{C2}$
(X)
(E)
$\phi 4$
(N)
INHIBIT ERROR CTR UP PULSES
$\phi 3$
ERROR COUNTER
2^0
P_E
$\overline{\phi 2}$
$\phi 3$
$\phi 3 \cdot 2^0$
SET $\overline{2_0}$ FF RESET 2_0
$P_E \overline{2_0}$
$P_E 2_0$
SET 2_0 RESET $\overline{2_0}$
U_L
D_L
$P_E (2_0 \cdot D_L + \overline{2_0} U_L)$
(E)
PRESENCE REMOVES CLAMP ON CTR RESET LINE.
2^1
2^2
2^3
2^4
2^5
2^6
2^7
2^8
ZERO DETECT
$Z_d = \overline{2_E^{10}}\ \overline{2_E^1}\ \overline{2_E^2}\ \overline{2_E^3}\ \overline{2_E^4}\ \overline{2_E^5}\ \overline{2_E^6}\ \overline{2_E^7}\ \overline{2_E^8}$
BUFFERS
$\overline{2^0}$
I
SATURATION DETECT
$N = U_L 2^7 2^8$
U_L
234
+4V
215 137 241 143
239
ERROR CTR ENABLE (E) FROM DIGITAL MODE MODULE
INHIBIT D/A TO SHAFT D/A MODULE (INHIBIT ON LOSS OF 4V)
$\phi 2$ $\phi 2$
$\phi 2$ $\phi 2$
123
121
122
COM
TO D/A LOGIC GND
+ D/A POLARITY (+ P_{DA})
− D/A POLARITY (− P_{DA})
COM
251 DD0
271 DD1
269 DD2
247 DD3
245 DD4
202 DD5
204 DD6
232 DD7
228 DD8
252
28VDC
168 +D/A
265 −D/A
LOGIC GND
D/A
CSM: TO MODE MODULE OPTICS D/A REFERENCE EXCITATION
LEM: PSA ISS 28V 800 CPS 1%
171
167
+28 V DC
164
DD0 263
DD1 159
DD2 259
DD3 155
DD4 255
DD5 150
DD6 251
DD7 146
DD8 246
166
245
TO 4V LO
INPUT LO
FROM EC & L MODULE (SEE NOTE 8)
INHIBIT DAC 140
LOGIC GND 268
FROM EC & L MODULE (SEE NOTE 8)
+Δθ'G HI 204 LO 101
−Δθ'G HI 105 LO 205
TO EC & L MODULE (SEE NOTE 8)
+Δθ'C HI 206 LO 108
−Δθ'C HI 109 LO 209
INTERNALLY DISTRIBUTED TO ERROR CTR AS SHOWN
206 HI
208 LO $\overline{\phi 2}$
259 HI
258 LO $\phi 3$
FROM MODE MODULE
MODE MODULE
REF LO (R_I)
800 CPS
TO ISS & RR INNER, MIDDLE & OUTER EC & L MODULES, & DIGITAL MODE MODULE
(a)
3μSEC, 51.2K PPS
TO DIGITAL MODE MODULE
TO DIGITAL MODE MOD & TO INNER, MIDDLE & OUTER EC & L MODULE
PPS
HI LO 263 267
ISS REFERENCE GENERATOR
+4V
2:1
HI LO 269 168
HI LO 171 170
2:1
CLOCK 51.2K PPS FROM AGC OR LGC
3μSEC, 51.2K PPS
25.6K PPS SYNC TO 4V POWER SUPPLY
HI LO 111 112
PULSE DRIVER
211 212 HI LO
25.6K PPS FROM DIGITAL MODE MODULE
ABORT GUIDANCE INTERCONNECTION LEM ONLY
215 223
+14V
14V POWER SUPPLY
118 117 120
DISTRIBUTED TO AGS DRIVER LOGIC
+4V DC
4V RETURN
28V MIXED FROM MODE MODULE
FROM 4V POWER SUPPLY
TO LEM ABORT GUIDANCE SYSTEM NOT USED IN CSM
INNER GIMBAL +Δθ G −Δθ G
HI LO HI LO 101 102 202 201
2:1
+14V
+4V
AGS PULSE DRIVERS & LOGIC
103 203 209 104
HI LO
Δ2°
DOWN LEVEL
UP LEVEL
FROM INNER READ COUNTER MODULE
FROM INNER ERROR COUNTER & LOGIC MODULE
MIDDLE GIMBAL +Δθ G −Δθ G
HI LO HI LO 107 108 203 208
+4V
+14V
AGS PULSE DRIVERS & LOGIC
105 205 207 106
HI LO
Δ2°
DOWN LEVEL
UP LEVEL
FROM MIDDLE READ COUNTER MODULE
FROM MIDDLE ERROR COUNTER & LOGIC MODULE
OUTER GIMBAL +Δθ G −Δθ G
HI LO HI LO 109 110 115 116
+4V
+14V
AGS PULSE DRIVERS & LOGIC
219 119 113 213
HI LO
Δ2°
DOWN LEVEL
UP LEVEL
FROM OUTER READ COUNTER MODULE
FROM OUTER ERROR COUNTER & LOGIC MODULE
CDU-ZERO INDICATE
HI LO 122 121
+4V
+14V
AGS CDU-ZERO PULSE DRIVER
119 220 218
HI Z LO
ZERO
ISS CDU ZERO FROM MODE MODULE
51.2 K PPS INVERTED
FROM DIGITAL MODE MODULE
25.6 KPPS TO INTERROGATE MODULE
HI LO 239 240
25.6 KPPS PULSE GENERATOR
$\phi 4$
DISTRIBUTED TO ALL I_2, I_3 GENERATORS
243 244
HI LO
$\phi 2$
FROM MODE MODULE
2015567
SHT 9 OF 9
F-2


21
20
19
18
D
C
B
A
MODULE TEST POINTS
TP TP
Up Dp
147 139
117
115
ERROR CTR DOWN LEVEL(D_L)
133
237 216 217
PART OF ERROR COUNTER
& LOGIC MODULE (EC&L)
D/A SECTION
(SCHEMATIC 2010048)
PINS 96 (TOTAL) USED
STRUCTURE GND
+4V
+4VDC
4V RETURN
+4 RETURN
DISTRIBUTED WITHIN THE MODULE AS REQUIRED
201 224 298 198 124 212 236 260 160 136 112 153 141 140
FROM DIGITAL MODE MODULE
COARSE ALIGN
(Ca)
HI
$\Delta 2^2$
LO
PIN 256
PIN 255
READ COUNTER MODULE (SEE SHEET 2)
$+P_{DA}$
$-P_{DA}$
D/A POLARITY FF
SET RESET
$U_P \cdot Z_d$
$D_P \cdot Z_d$
ZERO DETECT (Z_d)
D/A POLARITY LOGIC
UP
DP
COARSE ALIGN (Ca)
Ca
(UL)
(DL)
ERROR COUNTER
UP-DOWN LOGIC
$D_L = (-P_{DA})U_P + (+P_{DA})D_P$
$U_L = (+P_{DA})U_P + (-P_{DA})D_P$
Dp
Up
ERROR COUNTER INPUT PULSES AT ϕ_4
3.2 KPPS
(P_E)
PULSE SELECTION LOGIC
$\bar{\phi}_1, \phi_4$
$G = Ca\,\Delta\theta_{c2} \times \bar{N}$
G IS SYNCHRONIZED BY ϕ_1 SO THAT G DURATION IS ϕ_1 THRU NEXT ϕ_1 FOLLOWING RECEIPT OF A $\Delta\theta_c$ PULSE
$P_E = E\bar{N}\,(\Delta\theta_{c2} + Ca\,\Delta 2^2)$
($E\bar{N}\Delta\theta_{c2}$ SYNCHRONIZED BY ϕ_1 & ϕ_4)
PULSES P_E ARE TRANSMITTED TO THE ERROR COUNTER INPUT AT ϕ_4
G
INHIBIT GIMBAL PULSES TO PI LOGIC OF EC&L READ CTR LOGIC SECTION
ϕ_1 ϕ_1
(Ca)
$\Delta 2^2$
$\bar{\phi}_2$
ϕ_3
ϕ_4 → DISTRIBUTED AS SHOWN
FROM UP-DOWN LOGIC OF EC&L READ CTR LOGIC SECTION
UP GIMBAL PULSES (U_G)
DOWN GIMBAL PULSES (D_G)
PULSE SELECTION
$D_P = D_{\theta C} + \bar{X}\,Ca\,U_G$
$U_P = U_{\theta C} + \bar{X}\,Ca\,D_G$
X
$\Delta\theta_{c2}$
(X)
(E)
ϕ_4 (N)
INHIBIT ERROR CTR UP PULSES
($U_{\theta C}$) UP PULSES COMPUTER
($D_{\theta C}$) DOWN PULSES COMPUTER
3.2 KPPS AT ϕ_2
FROM DIGITAL MODE MODULE ϕ_1
FROM MODE MODULE ϕ_2 ϕ_2 ϕ_3
HI LO
163 161 125 159 167 165 171 170
ϕ_1
ϕ_2
DISTRIB TO SINGLE PULSE SYNC, PULSE SELECTION LOGIC & TO READ COUNTER LOGIC SECTION
3.22 KPPS AT ϕ_2
ϕ_3
$+\Delta\theta_c$
$-\Delta\theta_c$
HI LO
$\Delta\theta_c$ MAX RATE IS 3.2 KPPS
SINGLE PULSE SYNC
$\Delta\theta_{c2} = [(+\Delta\theta_c) + (-\Delta\theta_c)]$ SYNCHRONIZED SO THAT PULSE OCCURS AT ϕ_2 FOLLOWING RECEIPT OF A $\Delta\theta_c$ PULSE.
$U_{\theta C} = +\Delta\theta_c$
$D_{\theta C} = -\Delta\theta_c$
SYNCHRONIZED SO THAT PULSE OCCURS AT ϕ_2 FOLLOWING RECEIPT OF THE RESPECTIVE $\Delta\theta_c$ PULSE. $(\phi_1 \rightarrow \phi_3)c = X$ GATE SIGNAL SENT FOLLOWING RECEIPT OF $\Delta\theta_c$
ϕ_1, ϕ_2
($\Delta\theta_{c2}$) 3.2 KPPS AT ϕ_2
$(\phi_1 \rightarrow \phi_3)_c$ GATE = X
ZERO DETECT (Z_d)
ϕ_4
ZERO DETECT
$Z_d = \bar{2}^0_E\,\bar{2}^1_E\,\bar{2}^2_E\,\bar{2}^3_E\,\bar{2}^4_E\,\bar{2}^5_E\,\bar{2}^6_E\,\bar{2}^7_E\,\bar{2}^8_E$
129 239
+4V
215 137 241 143
ERRO
INHIBIT D/A TO S
FROM D/A MODULE (SEE NOTE 8)
CSM-TO OPTICS SHAFT EC&L MODULE & DIGITAL MODE MODULE (I_2, I_3 GEN) LEM-TO SHAFT & TRUNNION EC&L MODULES & DIGITAL MODE MODULE (I_2, I_3 GEN)
INTERROGATE PULSES
CSM: OPTICS 28VDC, LEM: IMU 28VDC, FROM PSA
0+28VDC
OPTICS R/R PULSE DRIVER SUPPLY TO CDU TEST CONNECTOR & OPTICS R/R FAIL DETECTOR IN DIGITAL MODE MODULE
+14VDC
CSM-TO OPTICS SHAFT D/A MODULE LEM-TO R/R SHAFT D/A MODULE
+14V
CSM-TO OPTICS TRUNNION D/A MODULE LEM-TO R/R TRUNNION D/A MODULE
+14V
222 129 221
STRUCTURE GND
153
14 V POWER SUPPLY
INTERROGATE MODULE
(SCHEMATIC 2010063)
123 227
HI LO
+5.6V TO TRUNNION INTERRO. GEN. & CROSSOVER CKT
259 135 240
HI LO
+4V TO ISS REF GENERATOR
2:1
SHAFT INTERROGATE GENERATOR
252 149 150 145 160 260
HI LO
(R1)
REF /0°
CSM-TO OPTICS SHAFT EC&L MODULE
LEM-TO RR SHAFT & TRUNNION EC&L MODULES & TO DIGITAL MODE MODULE R/R AMBIGUITY LOGIC
REF 45°
USED CSM ONLY TO OPTICS TRUNNION EC&L MODULE
HI LO HI LO
298 138 242 239
OPTX/R/R REFERENCE GENERATOR
FROM SHAFT INTERRO. GEN.
5.6V
USED CSM ONLY TRUNNION COS (θ-ψ) /90° FROM MSA MODULE
COS (θ-ψ) /90°
(I)
TRUNNION INTERROGATE PULSES
USED CSM ONLY-TO TRUNNION EC&L MOD & DIGITAL MODE MODULE
HI LO
125 225
2:1
TRUNNION INTERROGATE GEN
137 236
HI LO
(I) ISS INTERROGATE PULSES
TO DIGITAL MODE MOD & TO INNER, MIDDLE & OUTER EC&L MODULE
3μ SEC, 1600 PPS
HI LO
158 256
2:1
ISS INTERROGATE GENERATOR
5:1
271 268 164
HI LO
ISS 28V DC
ISS-28V 800~ 1%
REF /0 (R1)
800 CPS
TO ISS & RR INNER, MIDDLE & OUTER EC&L MODULES, & DIGITAL MODE MODULE
HI LO
263 261
ISS REFERENCE GENERATOR
+4V
5:1
167
TO +4V RETURN
(a)
3μ SEC, 51.2K PPS
TO DIGITAL MODE MODULE
HI LO
269 168
2:1
HI LO
171 170
CLOCK 51.2K PPS FROM AGC OR LGC
3μ SEC, 51.2K PPS
25.6K PPS SYNC TO 4V POWER SUPPLY
HI LO
111 112
2:1
PULSE DRIVER
211 212
HI LO
25.6K PPS FROM DIGITAL MODE MODULE
14V
ABC
INT
CSM-FROM OPTICS POWER LEM-FROM IMU POWER
28 V DC
+4 V LO
CSM-FROM OPTICS POWER SUPPLY LEM-FROM IMU POWER SUPPLY
28V 800 ~ 1%
LO
4V POWER SUPPLY
4V LO
+4 V DC
2015567
SHT 1 OF 3



NOTES CONT:

8. COMPUTER PULSE WEIGHT OPTICS CDU-CGC.
   A) OPTICS OPERATION SHAFT (MECHANICAL):
      $\pm\Delta\theta_G$ (CDU TO CGC) $\simeq$ 40 SEC
      $\pm\Delta\theta_C$ (CGC TO CDU) $\simeq$ 160 SEC
   TRUNNION (LINE OF SIGHT):
      $\pm\Delta\theta_G$ (CDU TO CGC) $\simeq$ 10 SEC
      $\pm\Delta\theta_C$ (CGC TO CDU) $\simeq$ 40 SEC
   B) TVC OPERATION: (USING D/A DC ERROR SIGNALS)
      PITCH SPS ENGINE GIMBLE (SHAFT D/A) $\pm\Delta\theta_C$ (CGC TO CDU) $\simeq$ 160 SEC
      YAW SPS ENGINE GIMBLE (TRUNNION D/A) $\pm\Delta\theta_C$ (CGC TO CDU) $\simeq$ 160 SEC

DELINEATED ON THIS DRAWING:

COUPLING DATA UNIT (CDU) 2 WIRE MECH APPLICABLE FOR OPTICS TRUNNION AND SHAFT AXIS CSM APPLICATION ONLY

NOTES:

1. JUMPER CONNECTIONS MADE IN CDU HEADER TO INTERCONNECT INTERNAL MODULE CIRCUITRY. FOR DETAILS REFER TO CORRESPONDING MODULE SCHEMATIC.
2. STRUCTURE GROUND - TIE POINT TO WIRE WRAP HEADER ASSEMBLY.
3. SEE BLOCK II HEADER CONNECTOR DWG CSM 2010073, & LEM 6010001 FOR TEST POINT USAGE.
4. RESOLVER ANGELS θ AND SCALING DESIGNATIONS (ie. SIN 56¼°) SHOWN IN QUADRANT SELECT AND MSA MODULES, REP. 16X & 64X RESOLVER OUTPUTS EXPRESSED IN ELECTRICAL DEGREES.
5. LINE OF SIGHT ANGLE IS EQUAL TO TWO TIMES THE MECHANICAL ANGLE.
6. AMBIGUITY LOGIC AND DETECTION NOT USED IN OPTICS TRUNNION APPLICATION.
7. SHEET 1, SHOWS THE OPTICS SHAFT & TRUNNION MODING, INTRROGATE FUNCTIONS, ETC. & THE D/A FUNCTION. THE D/A FUNCTION IS IDENTICAL EXCEPT FOR SCALING AS NOTED.
   SHEET 2, SHOWS THE OPTICS TRUNNION A/D FUNCTION 2.5 SEC MECHANICAL TRUNNION ANGLE LEAST SIGNIFICANT BIT.
   SHEET 3, SHOWS THE OPTICS SHAFT A/D FUNCTION 20 SEC MECHANICAL SHAFT ANGLE LEAST SIGNIFICANT BIT.

NEXT ASSY	USED ON	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS ± DECIMALS ± ANGLES ± DO NOT SCALE THIS DRAWING MATERIAL — HEAT TREATMENT — FINAL FINISH —	MIT INSTRUMENTATION LAB CAMBRIDGE MASS DRAWN J. Koss DATE 3-8-65 CHECKED J. Gilmore 3-12-65 APPROVAL J. Gilmore 3-19-65 APPROVAL 3/19/65 NASA APPROVAL W. J. R. 3-23-65 MIT APPROVAL 3/23/65	MANNED SPACECRAFT CENTER HOUSTON, TEXAS OPTICS TRUNNION & SHAFT CDU BLOCK DIAGRAM BLOCK II (2 LINE MECH) CODE IDENT NO. SIZE J NASA DRAWING NO. 2015567 SCALE — WT SHEET 2 OF 3
APPLICATION				

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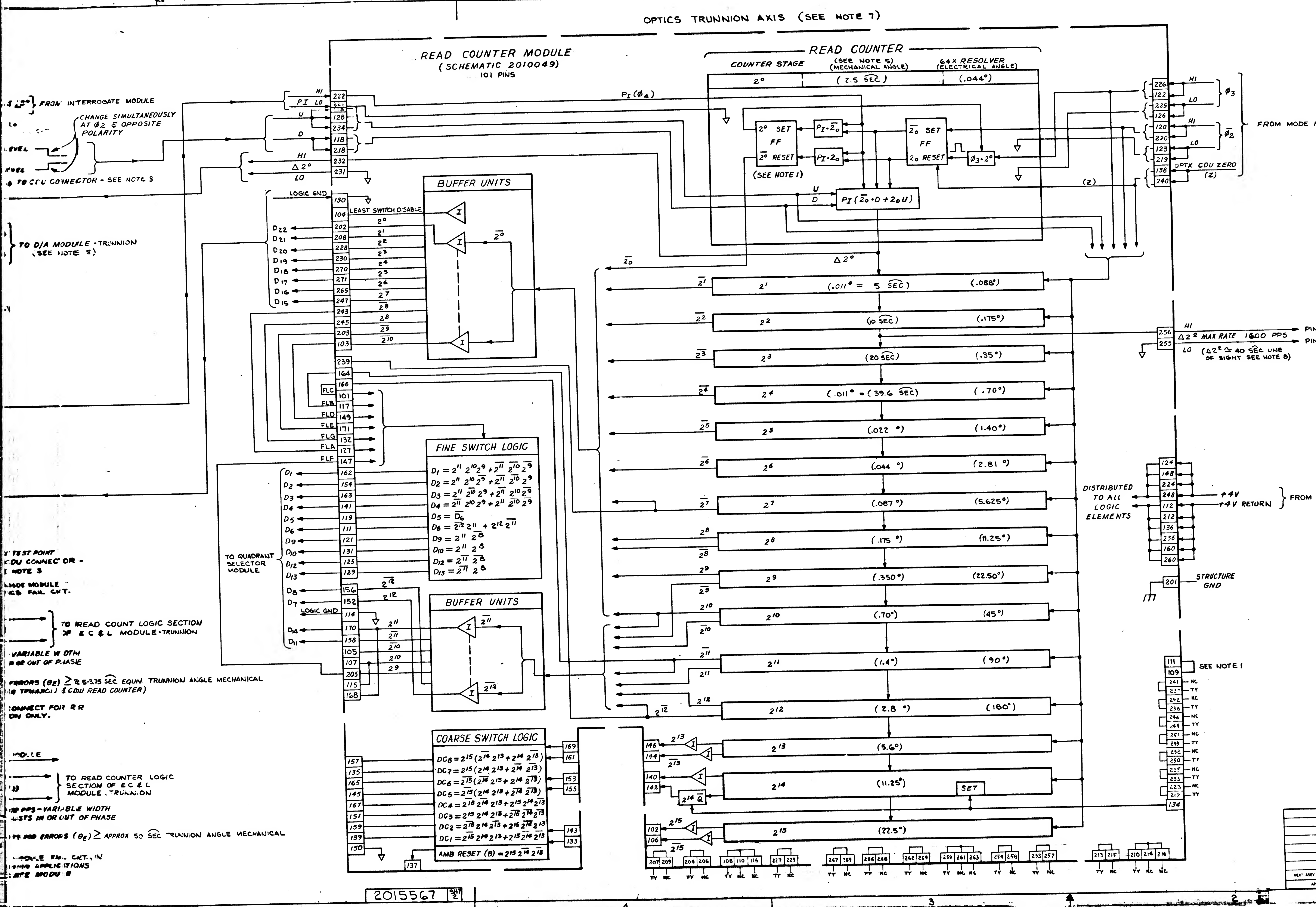
GILMORE


OPTICS TRUNNION AXIS (SEE NOTE 7)
READ COUNTER MODULE
(SCHEMATIC 2010049)
101 PINS
READ COUNTER
COUNTER STAGE
(SEE NOTE 5) (MECHANICAL ANGLE)
64X RESOLVER (ELECTRICAL ANGLE)
2° (2.5 SEC) (.044°)
FROM INTERROGATE MODULE
CHANGE SIMULTANEOUSLY AT Φ2 & OPPOSITE POLARITY
TO CDU CONNECTOR - SEE NOTE 3
PI(Φ4)
2° SET FF
2° RESET
(SEE NOTE 1)
2₀ SET FF
2₀ RESET
PI·2₀
Φ3·2°
PI(2₀·D + 2₀U)
Δ2°
Φ3
Φ2
FROM MODE MODULE
OPTX CDU ZERO (Z)
BUFFER UNITS
LEAST SWITCH DISABLE
LOGIC GND
TO D/A MODULE - TRUNNION (SEE NOTE 8)
D22 D21 D20 D19 D18 D17 D16 D15
2¹ (.011° = 5 SEC) (.088°)
2² (10 SEC) (.175°)
2³ (20 SEC) (.35°)
2⁴ (.011° = (39.6 SEC) (.70°)
2⁵ (.022 °) (1.40°)
2⁶ (.044 °) (2.81 °)
2⁷ (.087 °) (5.625°)
2⁸ (.175 °) (11.25°)
2⁹ (.350°) (22.50°)
2¹⁰ (.70°) (45°)
2¹¹ (1.4°) (90°)
2¹² (2.8 °) (180°)
2¹³ (5.6°)
2¹⁴ (11.25°) SET
2¹⁵ (22.5°)
EC & L MOD (SEE SHEET
PIN 141
PIN 140
Δ2² MAX RATE 1600 PPS
(Δ2² ≃ 40 SEC LINE OF SIGHT SEE NOTE 8)
FINE SWITCH LOGIC
D1 = 2¹¹ 2¹⁰ 2⁹ + 2¹¹ 2¹⁰ 2⁹
D2 = 2¹¹ 2¹⁰ 2⁹ + 2¹¹ 2¹⁰ 2⁹
D3 = 2¹¹ 2¹⁰ 2⁹ + 2¹¹ 2¹⁰ 2⁹
D4 = 2¹¹ 2¹⁰ 2⁹ + 2¹¹ 2¹⁰ 2⁹
D5 = D6
D6 = 2¹² 2¹¹ + 2¹² 2¹¹
D9 = 2¹¹ 2⁸
D10 = 2¹¹ 2⁸
D12 = 2¹¹ 2⁸
D13 = 2¹¹ 2⁸
TO QUADRANT SELECTOR MODULE
FLC FLB FLD FLE FLG FLA FLF
TO READ COUNT LOGIC SECTION OF EC & L MODULE-TRUNNION
COARSE SWITCH LOGIC
DC8 = 2¹⁵(2¹⁴ 2¹³ + 2¹⁴ 2¹³)
DC7 = 2¹⁵(2¹⁴ 2¹³ + 2¹⁴ 2¹³)
DC6 = 2¹⁵(2¹⁴ 2¹³ + 2¹⁴ 2¹³)
DC5 = 2¹⁵(2¹⁴ 2¹³ + 2¹⁴ 2¹³)
DC4 = 2¹⁵ 2¹⁴ 2¹³ + 2¹⁵ 2¹⁴ 2¹³
DC3 = 2¹⁵ 2¹⁴ 2¹³ + 2¹⁵ 2¹⁴ 2¹³
DC2 = 2¹⁵ 2¹⁴ 2¹³ + 2¹⁵ 2¹⁴ 2¹³
DC1 = 2¹⁵ 2¹⁴ 2¹³ + 2¹⁵ 2¹⁴ 2¹³
AMB RESET (B) = 2¹⁵ 2¹⁴ 2¹³
TO READ COUNTER LOGIC SECTION OF EC & L MODULE TRUNNION
DISTRIBUTED TO ALL LOGIC ELEMENTS
+4V
+4V RETURN
FROM 4V POWER SUPPLY
STRUCTURE GND
SEE NOTE 1
TY NC
ERRORS (θE) ≥ 2.5-3.75 SEC EQUIV. TRUNNION ANGLE MECHANICAL
PPS-VARIABLE WIDTH
ERRORS (θE) ≥ APPROX 50 SEC TRUNNION ANGLE MECHANICAL
2015567 SHT 2
F-3

NOTES CONT:

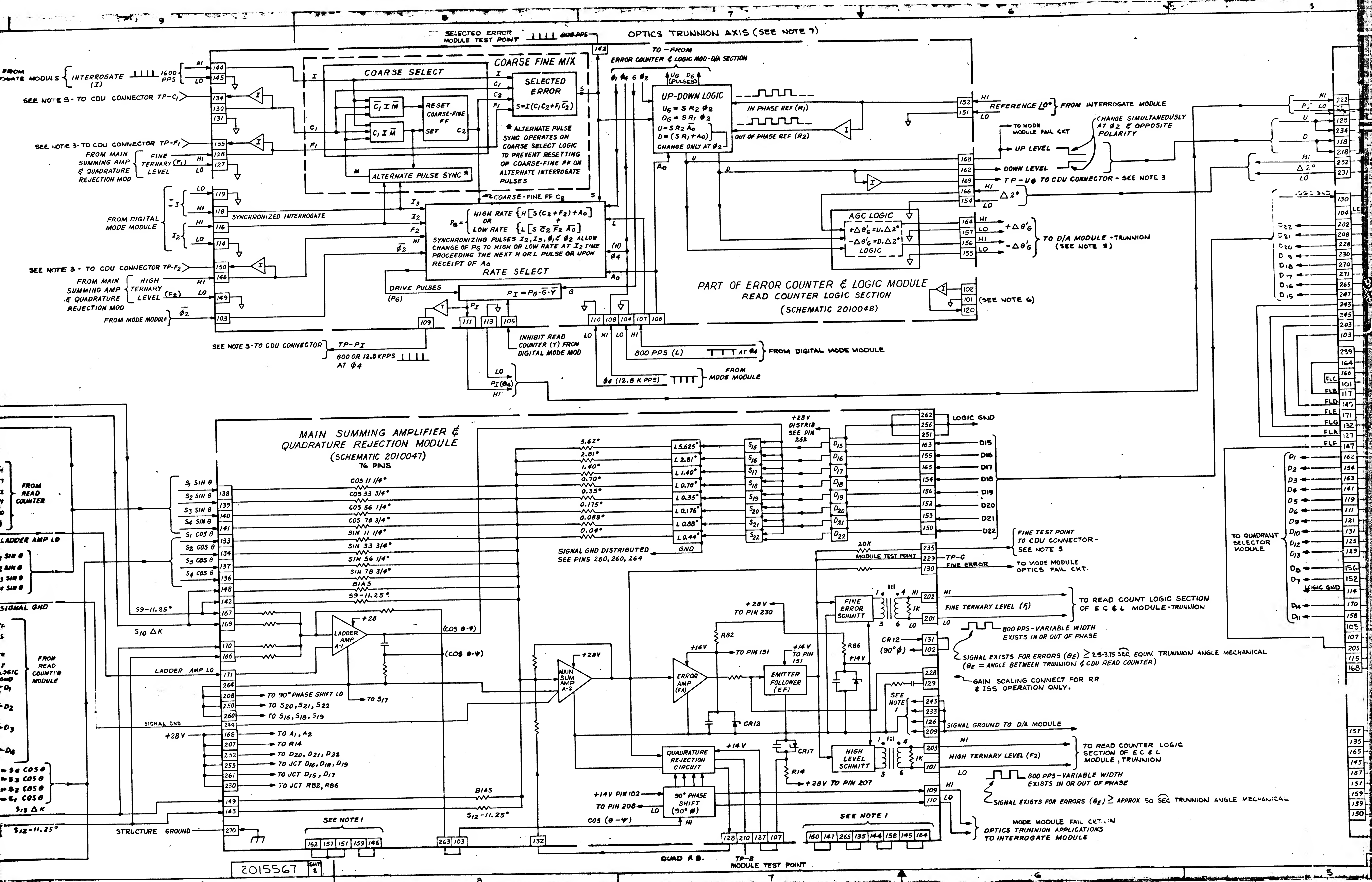
8. COMPUTER PULSE WEIGH
A) OPTICS OPERATION S
±Δθ₆ (CDU TO C
±Δθc (CGC TO CD
TRUNNION (LINE OF S
±Δθ₆ (CDU TO C
±Δθc (CGC TO C
B) TVC OPERATION : (US
PITCH SPS ENGINE
YAW SPS ENGINE

DELINEATED ON THIS DRAW
COUPLING DATA UNIT (CD
FOR OPTICS TRUNNION A
APPLICATION ONLY

NOTES :

1. JUMPER CONNECTION
INTERCONNECT INTER
FOR DETAILS REFER
MODULE SCHEMATIC
2. STRUCTURE GROUND
HEADER ASSEMBLY.
3. SEE BLOCK II HEADE
20100-3, & LEM 60
4. RESOLVER ANGELS
(ie. SIN 56¼°) SHOWN
NISA MODULES, REP.
EXPRESSED IN ELECT
5. LINE OF SIGHT ANGLE IS
MECHANICAL ANGLE.
6. AMBIGUITY LOGIC AND
TRUNNION APPLICAT
7. SHEET 1, SHOWS THE
INTERROGATE
THE ~ A FUNC
SHEET 2. SHOWS THE
MECHANICAL T
SHEET 3. SHOWS THE
MECHANICAL

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS DECIMALS ANGLES
DO NOT SCALE THIS DRAWING
MATERIAL
HEAT TREATMENT
FINAL FINISH
NEXT ASSY USED ON
APPLICATION


OPTICS TRUNNION AXIS (SEE NOTE 7)
SELECTED ERROR MODULE TEST POINT 800 PPS 142
TO - FROM ERROR COUNTER & LOGIC MOD-D/A SECTION
FROM INTERROGATE MODULE INTERROGATE (I) 1600 PPS HI LO 144 145
SEE NOTE 3 - TO CDU CONNECTOR TP-C1 134 130 131
COARSE FINE MIX
COARSE SELECT
SELECTED ERROR
S = I (C1C2 + F1C̄2)
C̄1 I M̄
C1 I M̄
RESET COARSE-FINE FF SET C2
* ALTERNATE PULSE SYNC OPERATES ON COARSE SELECT LOGIC TO PREVENT RESETTING OF COARSE-FINE FF ON ALTERNATE INTERROGATE PULSES
ALTERNATE PULSE SYNC *
SEE NOTE 3 - TO CDU CONNECTOR TP-F1 135
FROM MAIN SUMMING AMP & QUADRATURE REJECTION MOD FINE TERNARY (F1) LEVEL HI LO 128 127
FROM DIGITAL MODE MODULE I3 LO HI 119 118 I2 HI LO 116 114
SYNCHRONIZED INTERROGATE
COARSE-FINE FF C2
PG = HIGH RATE {H [S (C2 + F2) + A0] OR + LOW RATE {L [S C̄2 F̄2 Ā0]
SYNCHRONIZING PULSES I2, I3, φ1 & φ2 ALLOW CHANGE OF PG TO HIGH OR LOW RATE AT I2 TIME PROCEEDING THE NEXT H OR L PULSE OR UPON RECEIPT OF A0
RATE SELECT
SEE NOTE 3 - TO CDU CONNECTOR TP-F2 150
FROM MAIN SUMMING AMP & QUADRATURE REJECTION MOD HIGH TERNARY LEVEL (F2) HI LO 146 149
FROM MODE MODULE φ2 103
DRIVE PULSES (PG)
PI = PG · Ḡ · Ȳ
109 111 113 105
SEE NOTE 3 - TO CDU CONNECTOR TP-PI 800 OR 12.8 KPPS AT φ4
INHIBIT READ COUNTER (Y) FROM DIGITAL MODE MOD
LO PI(φ4) HI
110 108 104 107 106 LO HI LO HI
800 PPS (L) AT φ4 FROM DIGITAL MODE MODULE
φ4 (12.8 K PPS) FROM MODE MODULE
UP-DOWN LOGIC
UG = S R2 φ2
DG = S R1 φ2
U = S R2 Ā0
D = (S R1 + A0)
CHANGE ONLY AT φ2
UG DG (PULSES)
IN PHASE REF (R1)
OUT OF PHASE REF (R2)
152 151 HI LO REFERENCE /0° FROM INTERROGATE MODULE
TO MODE MODULE FAIL CKT
UP LEVEL
DOWN LEVEL
CHANGE SIMULTANEOUSLY AT φ2 & OPPOSITE POLARITY
168 162 169 166 154
TP-UG TO CDU CONNECTOR - SEE NOTE 3
Δ2°
AGC LOGIC
+Δθ'G = U·Δ2°
-Δθ'G = D·Δ2°
LOGIC
164 157 156 155 HI LO HI LO +Δθ'G -Δθ'G TO D/A MODULE - TRUNNION (SEE NOTE 8)
PART OF ERROR COUNTER & LOGIC MODULE
READ COUNTER LOGIC SECTION
(SCHEMATIC 2010048)
102 101 120 (SEE NOTE 6)
222 129 234 118 218 232 231 130 104 202 208 228 230 270 271 265 247 243 245 203 103 239 164 166 101 117 145 171 132 127 147
D22 D21 D20 D19 D18 D17 D16 D15
FLC FLB FLD FLE FLG FLA FLF
MAIN SUMMING AMPLIFIER & QUADRATURE REJECTION MODULE
(SCHEMATIC 2010047)
76 PINS
FROM READ COUNTER
S1 SIN θ S2 SIN θ S3 SIN θ S4 SIN θ S1 COS θ S2 COS θ S3 COS θ S4 COS θ
138 139 140 141 133 134 137 136 148 142 167 169 170 166 171 264 208 250 260 244 168 207 252 255 261 230 149 143 270
COS 11 1/4° COS 33 3/4° COS 56 1/4° COS 78 3/4° SIN 11 1/4° SIN 33 3/4° SIN 56 1/4° SIN 78 3/4° BIAS S9-11.25°
LADDER AMP LO
SIGNAL GND
S9-11.25°
S10 ΔK
LADDER AMP A-1 +28
(COS θ-Ψ)
TO 90° PHASE SHIFT LO
TO S17
TO S20, S21, S22
TO S16, S18, S19
TO A1, A2
TO R14
TO D20, D21, D22
TO JCT D16, D18, D19
TO JCT D15, D17
TO JCT R82, R86
+28 V
BIAS
S12-11.25°
S13 ΔK
STRUCTURE GROUND
SEE NOTE 1 162 157 151 159 146
263 103 132
5.62° 2.81° 1.40° 0.70° 0.35° 0.175° 0.088° 0.04°
L5.625° L2.81° L1.40° L0.70° L0.35° L0.176° L0.088° L0.44° GND
S15 S16 S17 S18 S19 S20 S21 S22
D15 D16 D17 D18 D19 D20 D21 D22
+28 V DISTRIB SEE PIN 252
262 256 251 163 155 165 154 156 152 153 150 LOGIC GND
D15 D16 D17 D18 D19 D20 D21 D22
SIGNAL GND DISTRIBUTED SEE PINS 250, 260, 264
235 229 130 20K MODULE TEST POINT TP-C FINE ERROR
FINE TEST POINT TO CDU CONNECTOR - SEE NOTE 3
TO MODE MODULE OPTICS FAIL CKT.
MAIN SUM AMP A-2 +28V
+28 V TO PIN 230
R82 +14V TO PIN 131
ERROR AMP (EA)
EMITTER FOLLOWER (EF)
+14 V TO PIN 131 R86 +14V
CR12 (90° φ) 131 102
CR12
FINE ERROR SCHMITT 1:1 1K 202 201 HI LO
FINE TERNARY LEVEL (F1)
TO READ COUNT LOGIC SECTION OF E C & L MODULE-TRUNNION
800 PPS - VARIABLE WIDTH EXISTS IN OR OUT OF PHASE
SIGNAL EXISTS FOR ERRORS (θE) ≥ 2.5-3.75 SEC. EQUIV. TRUNNION ANGLE MECHANICAL (θE = ANGLE BETWEEN TRUNNION & CDU READ COUNTER)
228 129 GAIN SCALING CONNECT FOR RR & ISS OPERATION ONLY.
SEE NOTE 1 243 233 126 209
SIGNAL GROUND TO D/A MODULE
QUADRATURE REJECTION CIRCUIT
+14 V CR17 R14
+28 V TO PIN 207
HIGH LEVEL SCHMITT 1:1 1K 203 101 HI LO
HIGH TERNARY LEVEL (F2)
TO READ COUNTER LOGIC SECTION OF E C & L MODULE, TRUNNION
800 PPS - VARIABLE WIDTH EXISTS IN OR OUT OF PHASE
SIGNAL EXISTS FOR ERRORS (θE) ≥ APPROX 50 SEC TRUNNION ANGLE MECHANICAL
+14 V PIN 102
TO PIN 208
90° PHASE SHIFT (90° φ) LO HI
COS (θ-Ψ)
109 110 HI LO
MODE MODULE FAIL CKT., IN OPTICS TRUNNION APPLICATIONS TO INTERROGATE MODULE
SEE NOTE 1 160 147 265 135 144 158 145 164
128 210 127 107
QUAD F.B.
TP-B MODULE TEST POINT
TO QUADRANT SELECTOR MODULE
D1 D2 D3 D4 D5 D6 D9 D10 D12 D13 D8 D7 D14 D11
162 154 163 141 119 111 121 131 125 129 156 152 114 170 158 105 107 205 115 168
LOGIC GND
157 135 165 145 167 151 159 139 150
FROM READ COUNTER LOGIC MODULE
2015567 SHT 2
9 8 7 6 5

F2

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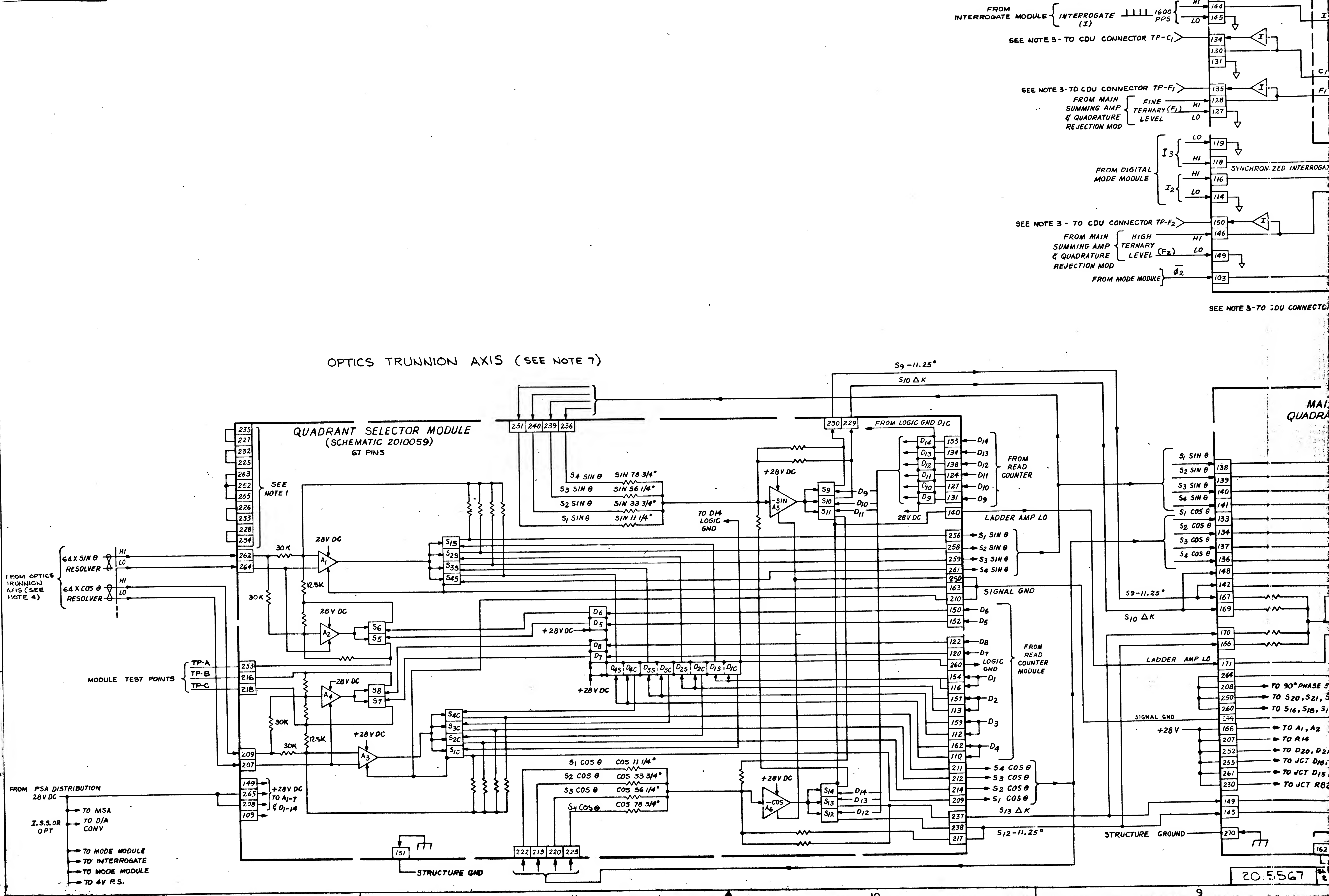
OPTICS TRUNNION AXIS (SEE NOTE 7)



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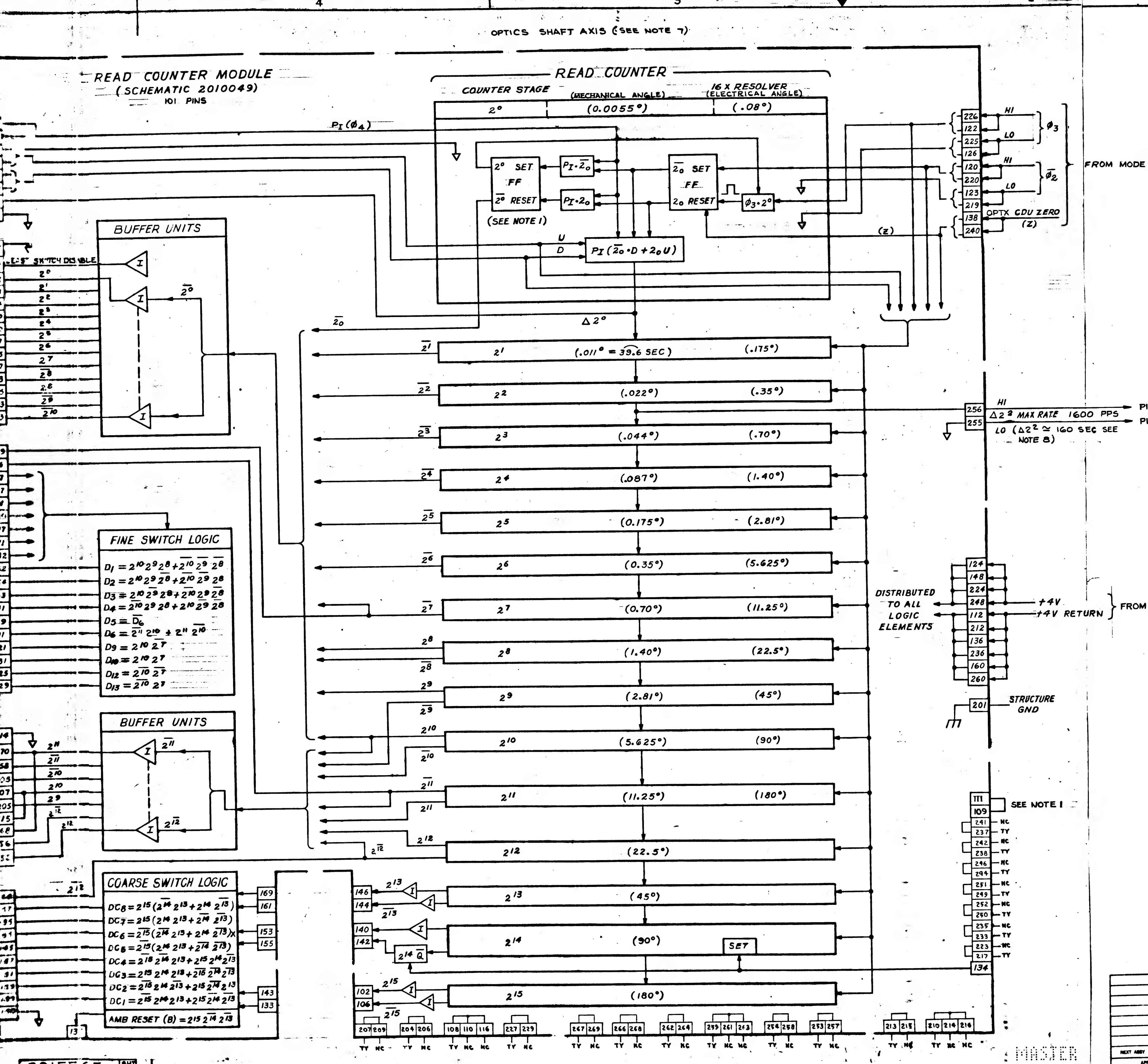

OPTICS SHAFT AXIS (SEE NOTE 7)
READ COUNTER MODULE
(SCHEMATIC 2010049)
101 PINS
READ COUNTER
COUNTER STAGE
(MECHANICAL ANGLE)
16 X RESOLVER (ELECTRICAL ANGLE)
2°
(0.0055°)
(.08°)
$P_I(\phi_4)$
2^0 SET FF $\overline{2^0}$ RESET
(SEE NOTE 1)
$P_I \cdot \overline{2_0}$
$P_I \cdot 2_0$
$\overline{2_0}$ SET FF 2_0 RESET
$\phi_3 \cdot 2^0$
U
D
$P_I(\overline{2_0} \cdot D + 2_0 U)$
(Z)
$\Delta 2^0$
$\overline{2_0}$
226
122
225
126
120
220
123
219
138
240
HI
LO
ϕ_3
$\overline{\phi_2}$
OPTX CDU ZERO (Z)
FROM MODE MODULE
BUFFER UNITS
"ZERO" SWITCH DISABLE
2^0 … 2^{10}
I
2^1 (.011° = 39.6 SEC) (.175°)
2^2 (.022°) (.35°)
2^3 (.044°) (.70°)
2^4 (.087°) (1.40°)
2^5 (0.175°) (2.81°)
2^6 (0.35°) (5.625°)
2^7 (0.70°) (11.25°)
2^8 (1.40°) (22.5°)
2^9 (2.81°) (45°)
2^{10} (5.625°) (90°)
2^{11} (11.25°) (180°)
2^{12} (22.5°)
2^{13} (45°)
2^{14} (90°)
SET
2^{14} Q
2^{15} (180°)
256
255
HI
$\Delta 2^2$ MAX RATE 1600 PPS
LO ($\Delta 2^2 \simeq$ 160 SEC SEE NOTE 8)
PIN 141
PIN 140
EC & L MODULE (SEE SHEET 1)
DISTRIBUTED TO ALL LOGIC ELEMENTS
124
148
224
248
112
212
136
236
160
260
+4V
+4V RETURN
FROM 4V POWER SUPPLY
201
STRUCTURE GND
111
109
SEE NOTE 1
241 NC
237 TY
242 NC
238 TY
246 NC
234 TY
251 NC
249 TY
252 NC
250 TY
235 NC
233 TY
223 NC
217 TY
134
FINE SWITCH LOGIC
$D_1 = 2^{10}2^9\overline{2^8} + \overline{2^{10}}\,\overline{2^9}\,2^8$
$D_2 = 2^{10}2^9\overline{2^8} + \overline{2^{10}}\,\overline{2^9}\,2^8$
$D_3 = 2^{10}\overline{2^9}\,\overline{2^8} + \overline{2^{10}}2^9 2^8$
$D_4 = \overline{2^{10}}2^9 2^8 + 2^{10}\overline{2^9}\,\overline{2^8}$
$D_5 = \overline{D_6}$
$D_6 = \overline{2^{11}}\,2^{10} + 2^{11}\,\overline{2^{10}}$
$D_9 = 2^{10}\,\overline{2^7}$
$D_{10} = 2^{10}\,2^7$
$D_{12} = \overline{2^{10}}\,\overline{2^7}$
$D_{13} = \overline{2^{10}}\,2^7$
BUFFER UNITS
2^{11} $\overline{2^{11}}$ $\overline{2^{10}}$ 2^{10} 2^9 2^{12} $\overline{2^{12}}$
COARSE SWITCH LOGIC
$DC_8 = 2^{15}(\overline{2^{14}}\,2^{13} + 2^{14}\,\overline{2^{13}})$
$DC_7 = 2^{15}(2^{14}\,2^{13} + \overline{2^{14}}\,\overline{2^{13}})$
$DC_6 = \overline{2^{15}}(\overline{2^{14}}\,2^{13} + 2^{14}\,\overline{2^{13}})$
$DC_5 = \overline{2^{15}}(2^{14}\,2^{13} + \overline{2^{14}}\,\overline{2^{13}})$
$DC_4 = \overline{2^{15}}\,\overline{2^{14}}\,2^{13} + 2^{15}\,2^{14}\,\overline{2^{13}}$
$DC_3 = \overline{2^{15}}\,2^{14}\,2^{13} + 2^{15}\,\overline{2^{14}}\,\overline{2^{13}}$
$DC_2 = \overline{2^{15}}\,2^{14}\,\overline{2^{13}} + 2^{15}\,\overline{2^{14}}\,2^{13}$
$DC_1 = \overline{2^{15}}\,\overline{2^{14}}\,\overline{2^{13}} + 2^{15}\,2^{14}\,2^{13}$
AMB RESET (B) $= 2^{15}\,\overline{2^{14}}\,\overline{2^{13}}$
169
161
153
155
143
133
13
146
144
140
142
102
106
207 209
204 206
108 110 116
227 229
267 269
266 268
262 264
259 261 263
256 258
253 257
213 215
210 214 216
TY NC

DELINEATED ON THIS DRAWING :
COUPLING DATA UNIT (CDU) 2 WIRE MECH APPLICABLE FOR
OPTICS TRUNNION & SHAFT AXIS CSM APPLICATION ONLY

NOTES :

1. JUMPER CONNECTIONS MADE IN CDU HEADER TO INTERCONNECT INTERNAL MODULE CIRCUITRY. FOR DETAILS REFER TO CORRESPONDING MODULE SCHEMATIC.
2. STRUCTURE GROUND - TIE POINT TO WIRE WRAP HEADER ASSEMBLY.
3. SEE BLOCK II HEADER CONNECTOR DWG CSM 2010073, & LEM 6010001 FOR TEST POINT USAGE.
4. RESOLVER ANGLES θ AND SCALING DESIGNATIONS (ie, SIN 56¼°) SHOWN IN QUADRANT SELECT AND MSA MODULES, REPRESENT 16X & 64X RESOLVER OUTPUTS EXPRESSED IN ELECTRICAL DEGREES.
5. LINE OF SIGHT ANGLE IS EQUAL TO TWO TIMES THE MECHANICAL ANGLE.
6. AMBIGUITY LOGIC AND DETECTION NOT USED IN OPTICS TRUNNION APPLICATION.
7. SHEET 1 , SHOWS THE OPTICS SHAFT & TRUNNION MODING, INTERROGATE FUNCTIONS, ETC. & THE D/A FUNCTION. THE D/A FUNCTION IS IDENTICAL. EXCEPT FOR SEALING AS NOTED.
   SHEET 2 , SHOWS THE OPTICS TRUNNION A/D FUNCTION 2.5 SEC MECHANICAL TRUNNION ANGLE LEAST SIGNIFICANT BIT.
   SHEET 3 , SHOWS THE OPTICS SHAFT A/D FUNCTION 20 SEC MECHANICAL SHAFT ANGLE LEAST SIGNIFICANT BIT.
8. COMPUTER PULSE WEIGHT OPTICS CDU-CGC.
   A) OPTICS OPERATION SHAFT (MECHANICAL):
   $\pm\Delta\theta_G$ (CDU TO CGC) $\simeq$ 40 SEC.
   $\pm\Delta\theta_C$ (CGC TO CDU) $\simeq$ 160 SEC.
   TRUNNION (LINE OF SIGHT):
   $\pm\Delta\theta_G$ (CDU TO CGC) $\simeq$ 10 SEC.
   $\pm\Delta\theta_C$ (CGC TO CDU) $\simeq$ 40 SEC.
   B) TVC OPERATION : (USING D/A DC ERROR SIGNALS)
   PITCH SPS ENGINE GIMBLE (SHAFT D/A) : $\pm\Delta\theta_C$ (CGC TO CDU) $\simeq$ 160 SEC
   YAW SPS ENGINE GIMBLE (TRUNNION D/A): $\pm\Delta\theta_C$ (CGC TO CDU) $\simeq$ 160 SEC

NEXT ASSY	USED ON	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS ± DECIMALS ± ANGLES ± DO NOT SCALE THIS DRAWING	MIT INSTRUMENTATION LAB CAMBRIDGE, MASS DWG. NO. CONTRACT
APPLICATION		MATERIAL —	DRAWN H. FERGUSON DATE 3-3-65 CHECKED J. Schmer 3-12-65 APPROVAL J. Schmer 3-19-65 APPROVAL 3-19-65
		HEAT TREATMENT —	NASA APPROVAL 3-23-65
		FINAL FINISH —	MIT APPROVAL 23 May 65

MANNED SPACECRAFT CENTER
HOUSTON, TEXAS

OPTICS TRUNNION & SHAFT
CDU BLOCK DIAGRAM
(2 LINE MECH)

CODE IDENT NO.	SIZE	NASA DRAWING NO.
	J	2015567
SCALE —	WT	SHEET 3 OF 3

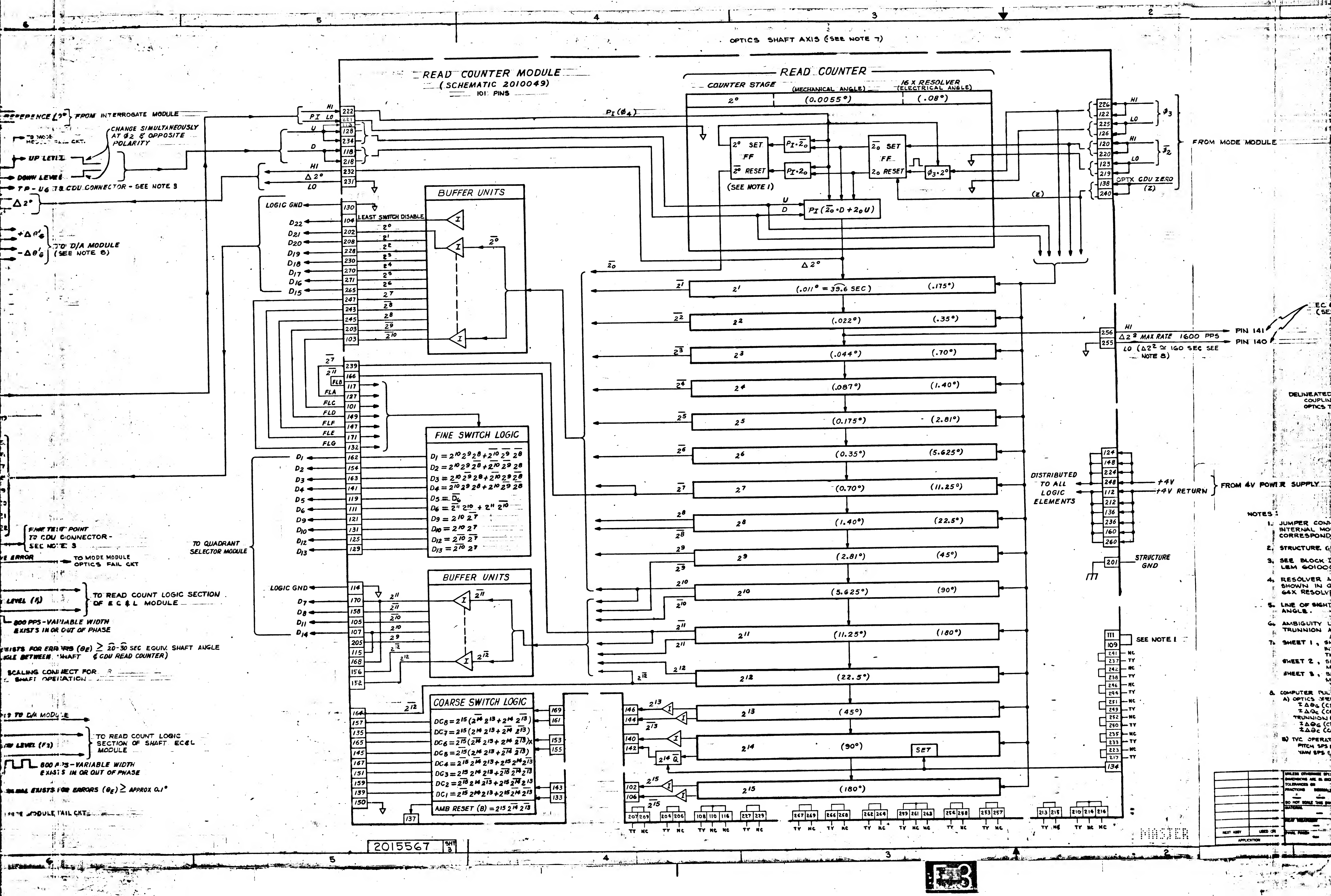
REVISIONS

2015567

2015567 SHT 3

MASTER

F-4



NOTES:

1. JUMPER CONN
INTERNAL MO
CORRESPOND

2. STRUCTURE G

3. SEE BLOCK
LEM 60100

4. RESOLVER A
SHOWN IN
64X RESOLVE

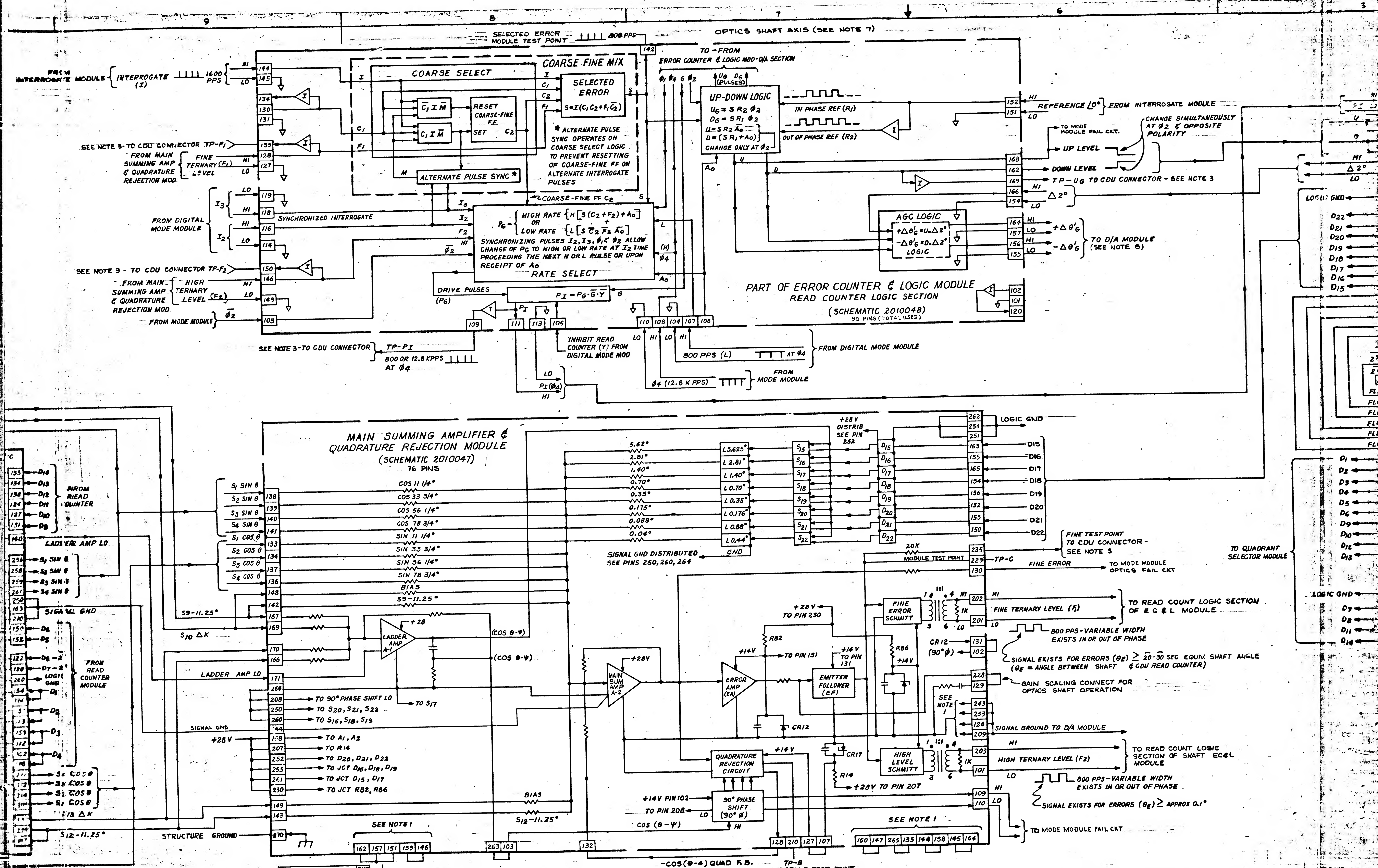
5. LINE OF SIGHT
ANGLE.

6. AMBIGUITY
TRUNNION A

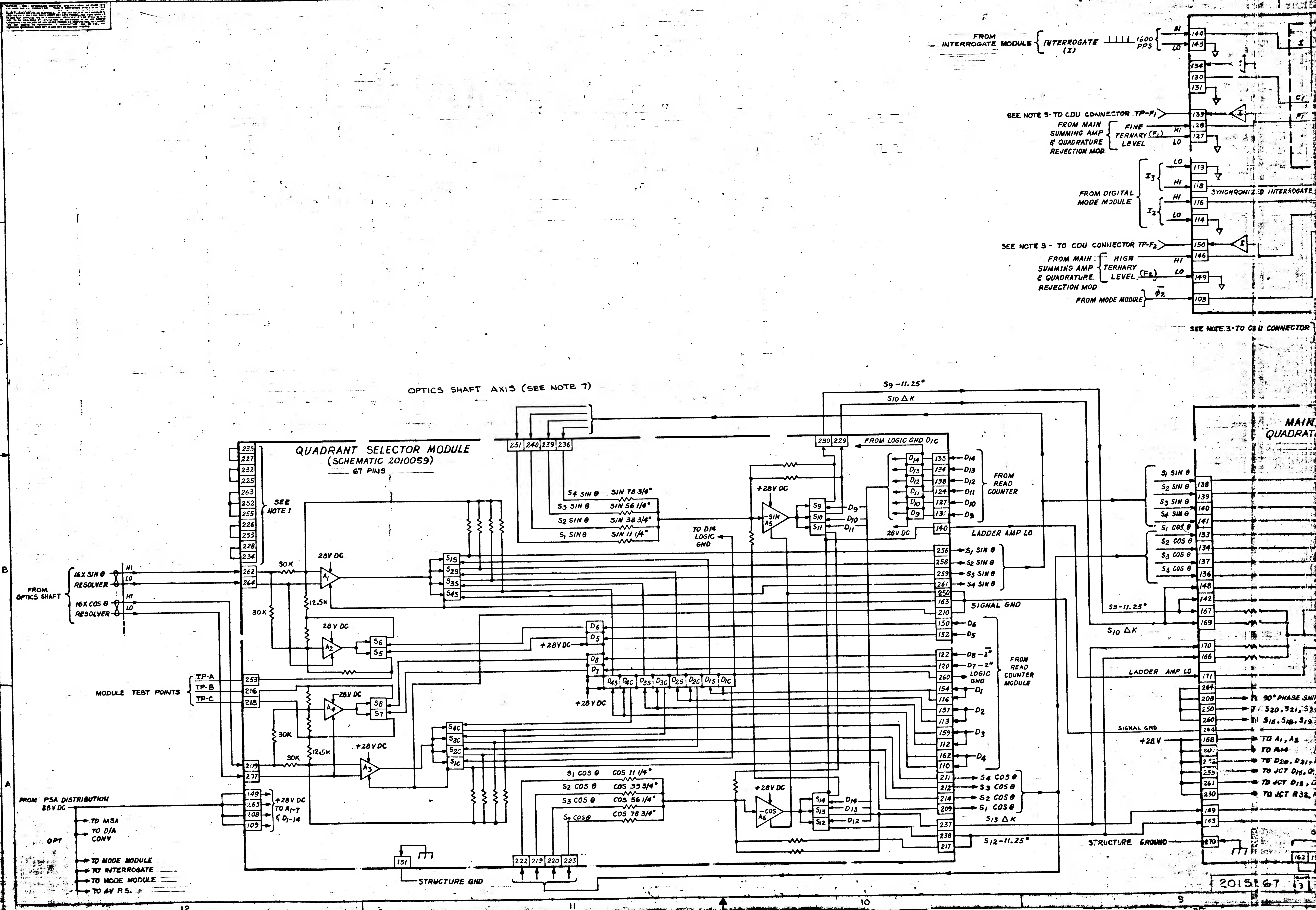
7. SHEET 1, S
SHEET 2, S
SHEET 3, S

8. COMPUTER PUL
A) OPTICS OPE
±ΔθG (C
±ΔθC (C
TRUNNION
±ΔθG (C
±ΔθC (C
B) TVC OPERAT
PITCH SPS
YAW SPS E

UNLESS OTHERWISE SPE
DIMENSIONS ARE IN INC
TOLERANCES ON
FRACTIONS DECIMALS
DO NOT SCALE THIS DR
MATERIAL
NEXT ASSY USED ON
APPLICATION


OPTICS SHAFT AXIS (SEE NOTE 7)
SELECTED ERROR MODULE TEST POINT 800 PPS
TO-FROM ERROR COUNTER & LOGIC MOD-D/A SECTION
COARSE FINE MIX
COARSE SELECT
SELECTED ERROR
S=I(C1C2+F1C2)
RESET COARSE-FINE FF
SET
* ALTERNATE PULSE SYNC OPERATES ON COARSE SELECT LOGIC TO PREVENT RESETTING OF COARSE-FINE FF ON ALTERNATE INTERROGATE PULSES
ALTERNATE PULSE SYNC *
FROM INTERROGATE MODULE { INTERROGATE (I) 1600 PPS
SEE NOTE 3-TO CDU CONNECTOR TP-F1
FROM MAIN SUMMING AMP & QUADRATURE REJECTION MOD FINE TERNARY (F1) LEVEL
FROM DIGITAL MODE MODULE
SYNCHRONIZED INTERROGATE
SEE NOTE 3 - TO CDU CONNECTOR TP-F2
FROM MAIN SUMMING AMP & QUADRATURE REJECTION MOD HIGH TERNARY LEVEL (F2)
FROM MODE MODULE
COARSE-FINE FF C2
HIGH RATE {H[S(C2+F2)+A0]} OR LOW RATE {L[S C2 F2 A0]}
SYNCHRONIZING PULSES I2, I3, φ1 & φ2 ALLOW CHANGE OF PG TO HIGH OR LOW RATE AT I2 TIME PROCEEDING THE NEXT H OR L PULSE OR UPON RECEIPT OF A0
RATE SELECT
DRIVE PULSES (PG)
PI=PG·G·Y
SEE NOTE 3-TO CDU CONNECTOR TP-PI 800 OR 12.8 KPPS AT φ4
INHIBIT READ COUNTER (Y) FROM DIGITAL MODE MOD
800 PPS (L) AT φ4
FROM DIGITAL MODE MODULE
φ4 (12.8 K PPS)
FROM MODE MODULE
UP-DOWN LOGIC
UG = S R2 φ2
DG = S R1 φ2
U = S R2 A0
D = (S R1 + A0)
CHANGE ONLY AT φ2
IN PHASE REF (R1)
OUT OF PHASE REF (R2)
REFERENCE 0° FROM INTERROGATE MODULE
TO MODE MODULE FAIL CKT.
UP LEVEL
DOWN LEVEL
CHANGE SIMULTANEOUSLY AT φ2 & OPPOSITE POLARITY
TP-UG TO CDU CONNECTOR - SEE NOTE 3
Δ2°
AGC LOGIC
+Δθ'G = UGΔ2°
-Δθ'G = DGΔ2°
LOGIC
TO D/A MODULE (SEE NOTE 8)
PART OF ERROR COUNTER & LOGIC MODULE
READ COUNTER LOGIC SECTION
(SCHEMATIC 2010048)
90 PINS (TOTAL USED)
MAIN SUMMING AMPLIFIER & QUADRATURE REJECTION MODULE
(SCHEMATIC 2010047)
76 PINS
LOGIC GND
+28 V DISTRIB SEE PIN 252
FROM READ COUNTER
LADDER AMP LO
SIGNAL GND
FROM READ COUNTER MODULE
COS 11 1/4°
COS 33 3/4°
COS 56 1/4°
COS 78 3/4°
SIN 11 1/4°
SIN 33 3/4°
SIN 56 1/4°
SIN 78 3/4°
BIAS
S9-11.25°
S10 ΔK
LADDER AMP A-1
(COS θ-ψ)
MAIN SUM AMP A-2
ERROR AMP (EA)
EMITTER FOLLOWER (EF)
QUADRATURE REJECTION CIRCUIT
90° PHASE SHIFT (90° φ)
FINE ERROR SCHMITT
HIGH LEVEL SCHMITT
TO 90° PHASE SHIFT LO
TO S20, S21, S22
TO S16, S18, S19
TO A1, A2
TO R14
TO D20, D21, D22
TO JCT D16, D18, D19
TO JCT D15, D17
TO JCT R82, R86
STRUCTURE GROUND
SIGNAL GND DISTRIBUTED SEE PINS 250, 260, 264
5.62° 2.81° 1.40° 0.70° 0.35° 0.175° 0.088° 0.04°
FINE TEST POINT TO CDU CONNECTOR - SEE NOTE 3
20K MODULE TEST POINT
TP-C
FINE ERROR
TO MODE MODULE OPTICS FAIL CKT
TO QUADRANT SELECTOR MODULE
FINE TERNARY LEVEL (F1)
TO READ COUNT LOGIC SECTION OF E C & L MODULE
800 PPS-VARIABLE WIDTH EXISTS IN OR OUT OF PHASE
SIGNAL EXISTS FOR ERRORS (θE) ≥ 20-30 SEC EQUIV. SHAFT ANGLE (θE = ANGLE BETWEEN SHAFT & CDU READ COUNTER)
GAIN SCALING CONNECT FOR OPTICS SHAFT OPERATION
SEE NOTE 1
SIGNAL GROUND TO D/A MODULE
HIGH TERNARY LEVEL (F2)
TO READ COUNT LOGIC SECTION OF SHAFT EC&L MODULE
800 PPS-VARIABLE WIDTH EXISTS IN OR OUT OF PHASE
SIGNAL EXISTS FOR ERRORS (θE) ≥ APPROX 0.1°
TO MODE MODULE FAIL CKT
+28V TO PIN 230
TO PIN 131
+14V PIN 102
TO PIN 208
+28V TO PIN 207
CR12 (90° φ)
COS (θ-ψ)
-COS(θ-ψ) QUAD F.B.
TP-B MODULE TEST POINT
SEE NOTE 1
9 8 7 6

2015567 SHT 3


FROM INTERROGATE MODULE
INTERROGATE (I)
1600 PPS
HI
LO
SEE NOTE 3 - TO CDU CONNECTOR TP-F1
FROM MAIN SUMMING AMP & QUADRATURE REJECTION MOD
FINE TERNARY (F1) LEVEL
FROM DIGITAL MODE MODULE
I3
I2
SYNCHRONIZED INTERROGATE
SEE NOTE 3 - TO CDU CONNECTOR TP-F2
HIGH TERNARY (F2) LEVEL
FROM MODE MODULE
φ2
SEE NOTE 3 - TO CDU CONNECTOR
OPTICS SHAFT AXIS (SEE NOTE 7)
QUADRANT SELECTOR MODULE
(SCHEMATIC 2010059)
67 PINS
SEE NOTE 1
S9 -11.25°
S10 ΔK
FROM LOGIC GND D1C
FROM READ COUNTER
S4 SIN θ — SIN 78 3/4°
S3 SIN θ — SIN 56 1/4°
S2 SIN θ — SIN 33 3/4°
S1 SIN θ — SIN 11 1/4°
TO D14 LOGIC GND
+28V DC
-SIN A5
28V DC
LADDER AMP LO
SIGNAL GND
FROM OPTICS SHAFT
16X SIN θ RESOLVER
16X COS θ RESOLVER
30K
12.5K
A1
A2
A3
A4
28V DC
+28V DC
MODULE TEST POINTS
TP-A
TP-B
TP-C
FROM READ COUNTER MODULE
D8 -2⁸
D7 -2⁸
LOGIC GND
S1 COS θ — COS 11 1/4°
S2 COS θ — COS 33 3/4°
S3 COS θ — COS 56 1/4°
S4 COS θ — COS 78 3/4°
-COS A6
S4 COS θ
S3 COS θ
S2 COS θ
S1 COS θ
S13 ΔK
S12 -11.25°
STRUCTURE GND
FROM PSA DISTRIBUTION 28V DC
+28V DC TO A1-7 & D1-14
TO MSA
TO D/A CONV
OPT
TO MODE MODULE
TO INTERROGATE
TO MODE MODULE
TO 4V P.S.
MAIN QUADRAT
S1 SIN θ
S2 SIN θ
S3 SIN θ
S4 SIN θ
S1 COS θ
S2 COS θ
S3 COS θ
S4 COS θ
S9 -11.25°
S10 ΔK
LADDER AMP LO
90° PHASE SHI
S20, S21, S2
S16, S18, S19
SIGNAL GND
+28V
TO A1, A2
TO R14
TO D20, D21
TO JCT D15, D
TO JCT D15, D
TO JCT R32
STRUCTURE GROUND
2015567
41+

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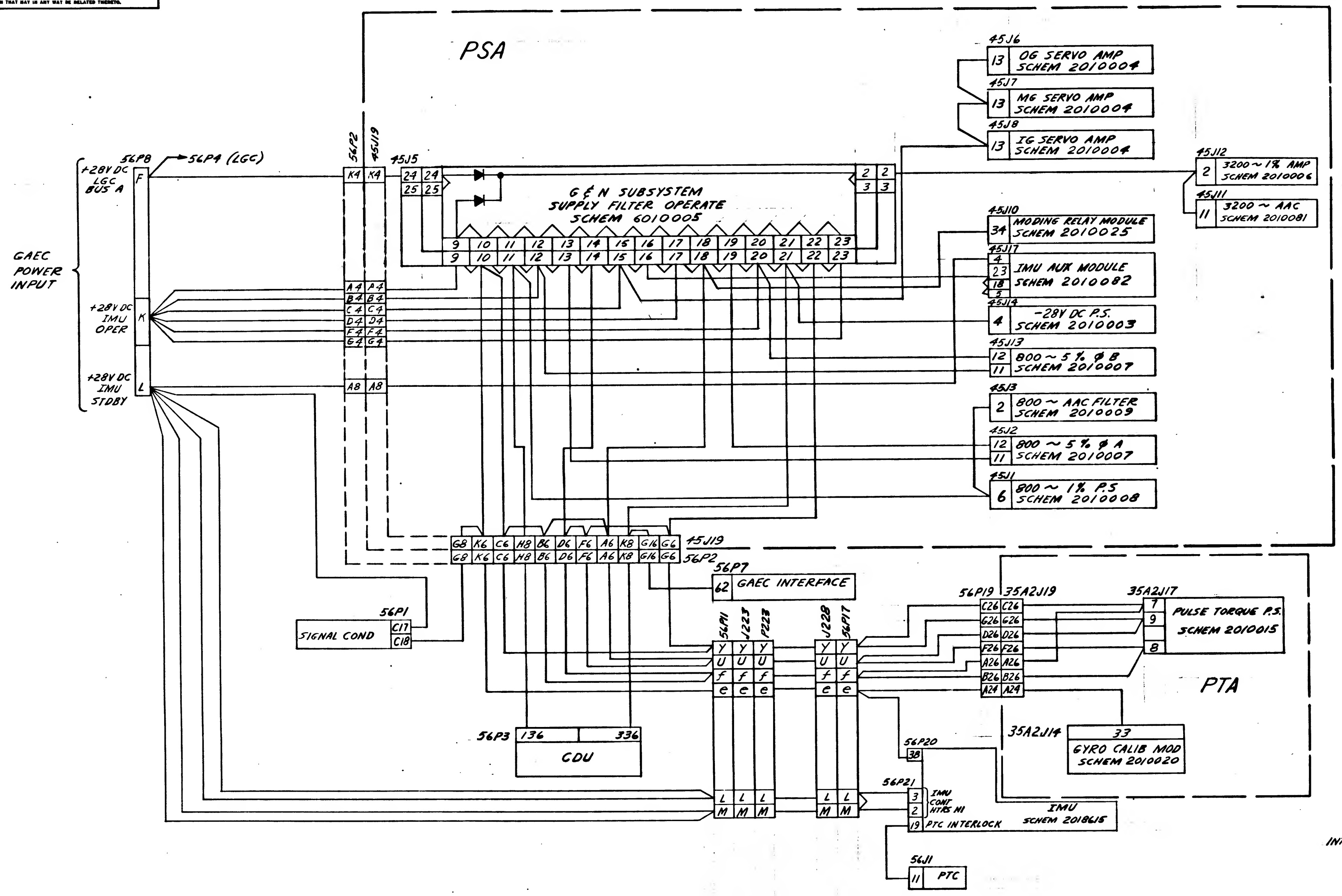
SYM	ZONE	DESCRIPTION	DR	CHK	DATE	APPROVED


PSA
GAEC POWER INPUT
+28V DC LGC BUS A
+28V DC IMU OPER
+28V DC IMU STDBY
56P8
F
K
L
56P4 (LGC)
56P2
45J19
K4
A4
B4
C4
D4
F4
G4
A8
45J5
24
25
G & N SUBSYSTEM SUPPLY FILTER OPERATE SCHEM 6010005
9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
2
3
45J6
13 OG SERVO AMP SCHEM 2010004
45J7
13 MG SERVO AMP SCHEM 2010004
45J8
13 IG SERVO AMP SCHEM 2010004
45J12
2 3200 ~ 1% AMP SCHEM 2010006
45J11
11 3200 ~ AAC SCHEM 2010081
45J10
34 MODING RELAY MODULE SCHEM 2010025
45J17
4
23
18
5
IMU AUX MODULE SCHEM 2010082
45J14
4 -28V DC P.S. SCHEM 2010003
45J13
12
11
800 ~ 5% ϕ B SCHEM 2010007
45J3
2 800 ~ AAC FILTER SCHEM 2010009
45J2
12
11
800 ~ 5% ϕ A SCHEM 2010007
45J1
6 800 ~ 1% P.S SCHEM 2010008
G8 K6 C6 H8 B6 D6 F6 A6 K8 G16 G6
45J19
56P2
56P7
62 GAEC INTERFACE
56P1
SIGNAL COND
C17
C18
56P3
136
336
CDU
56P11
J223
P223
J228
56P17
Y
U
f
e
L
M
56P19
35A2J19
C26
G26
D26
F26
A26
B26
A24
35A2J17
7
9
8
PULSE TORQUE P.S. SCHEM 2010015
PTA
35A2J14
33
GYRO CALIB MOD SCHEM 2010020
56P20
38
56P21
3
2
19
IMU CONT HTRS HI
PTC INTERLOCK
IMU SCHEM 2018615
56J1
11 PTC

INTERPRET DRAWING IN ACCORDANCE WITH MIL-D-70327

QTY REQD	PART OR IDENTIFYING NO.	MATERIAL OR NOTES	NOMENCLATURE OR DESCRIPTION	FIND NO.

LIST OF MATERIALS

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
CAPACITOR VALUES ARE IN μf
RESISTOR VALUES ARE IN OHMS
TOLERANCES ON
FRACTIONS ± DECIMALS ± ANGLES ±
DO NOT SCALE THIS DRAWING

MATERIAL

MIT
INSTRUMENTATION LAB
CAMBRIDGE, MASS.

MANNED SPACECRAFT CENTER
HOUSTON, TEXAS

DRAWN THENO 8-5-65
CHECKED D. Brown 8-10-65
APPROVED 11/1/65
APPROVED
APPROVED MIT 27
APPROVED MSC A. C. METZGER
DATE

LEM +28V DC
POWER DISTRIBUTION

CODE IDENT NO.
SIZE D
DRAWING NO. 6015570
SCALE
SHEET 1 OF 1

6015570

MASTER

ZONE	LTR	DESCRIPTION	DR	CHK	DATE	APPROVED
	A	REVISED PER TDRR 30381				
	B	REVISED PER TDRR 30665				

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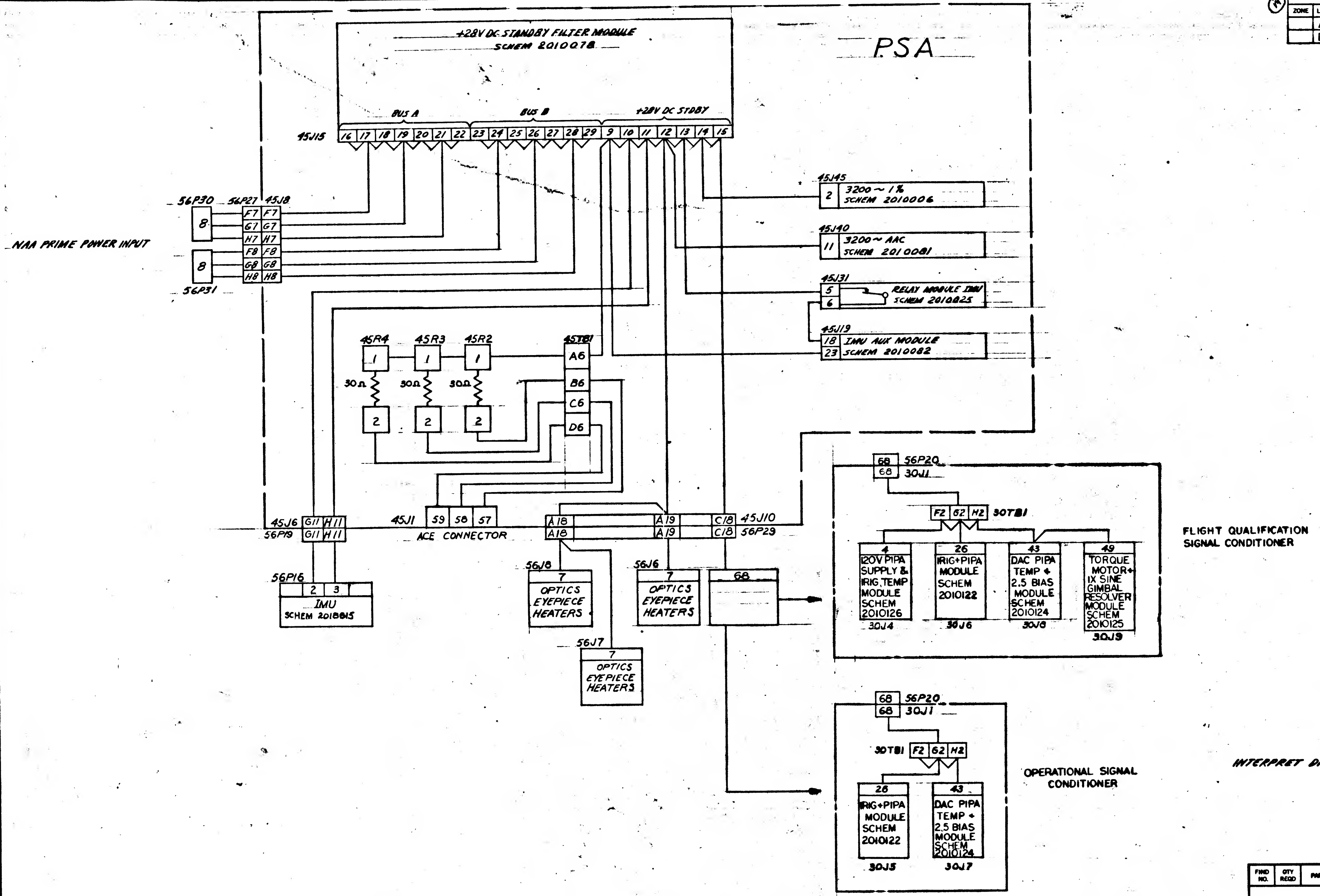

INTERPRET DRAWING IN ACCORDANCE WITH MIL-D-70327

MASTER

FIND NO.	QTY REQD	PART OR IDENT. NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR SPECIFICATION

LIST OF MATERIALS

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
CAPACITOR VALUES ARE IN μf
RESISTOR VALUES ARE IN OHMS
ELECTRICAL TOLERANCES = ±5%

DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS DECIMALS ANGLES
± ± ±
DO NOT SCALE THIS DRAWING

MATERIAL

DRAWN THENO 10-4-65
CHECKED 10-5-65
APPROVED
APPROVED

MIT APPROVED DATE 7 Dec 65
A. C. METZGER

INSTRUMENTATION LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
CAMBRIDGE, MASS.

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BLOCK II C/M

SIZE D
CODE IDENT NO.
DRAWING NO. 2015571
SCALE
SHEET 2 OF 2

2015571 B

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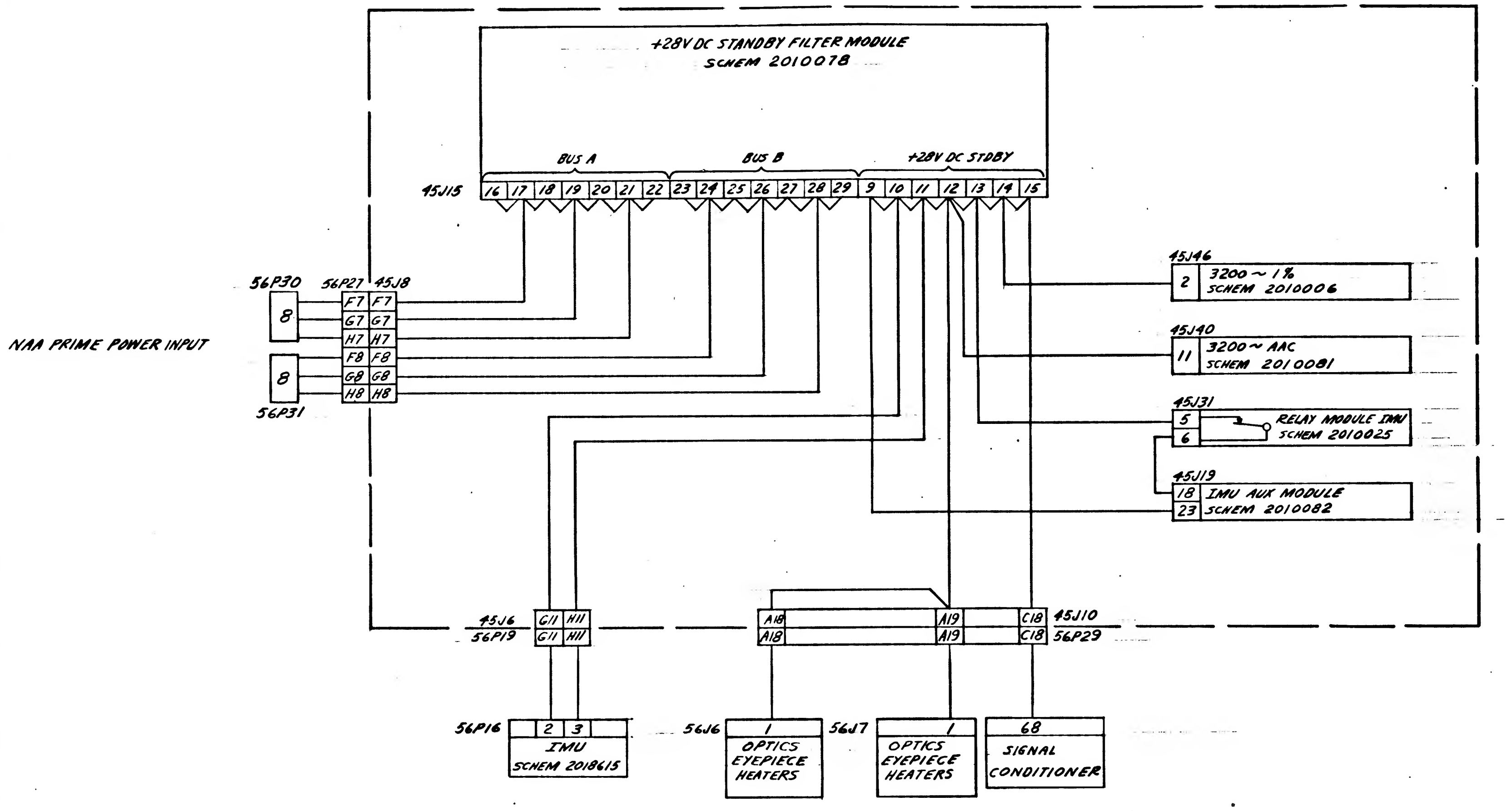

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2015571

MASTER

FIND NO.	QTY REQD	PART OR IDENT. NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR SPECIFICATION

LIST OF MATERIALS

NEXT ASSY	USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED
CAPACITOR VALUES ARE IN μf
RESISTOR VALUES ARE IN OHMS
ELECTRICAL TOLERANCES = ±5%

DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS DECIMALS ANGLES
± ± ±
DO NOT SCALE THIS DRAWING

MATERIAL

DRAWN THENO 10-4-65
CHECKED D. Brown 10-5-65
APPROVED
APPROVED

MIT APPROVED DATE 7 Dec 65
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BLOCK II G/M

SIZE D
CODE IDENT NO.
DRAWING NO. 2015571
SCALE
SHEET

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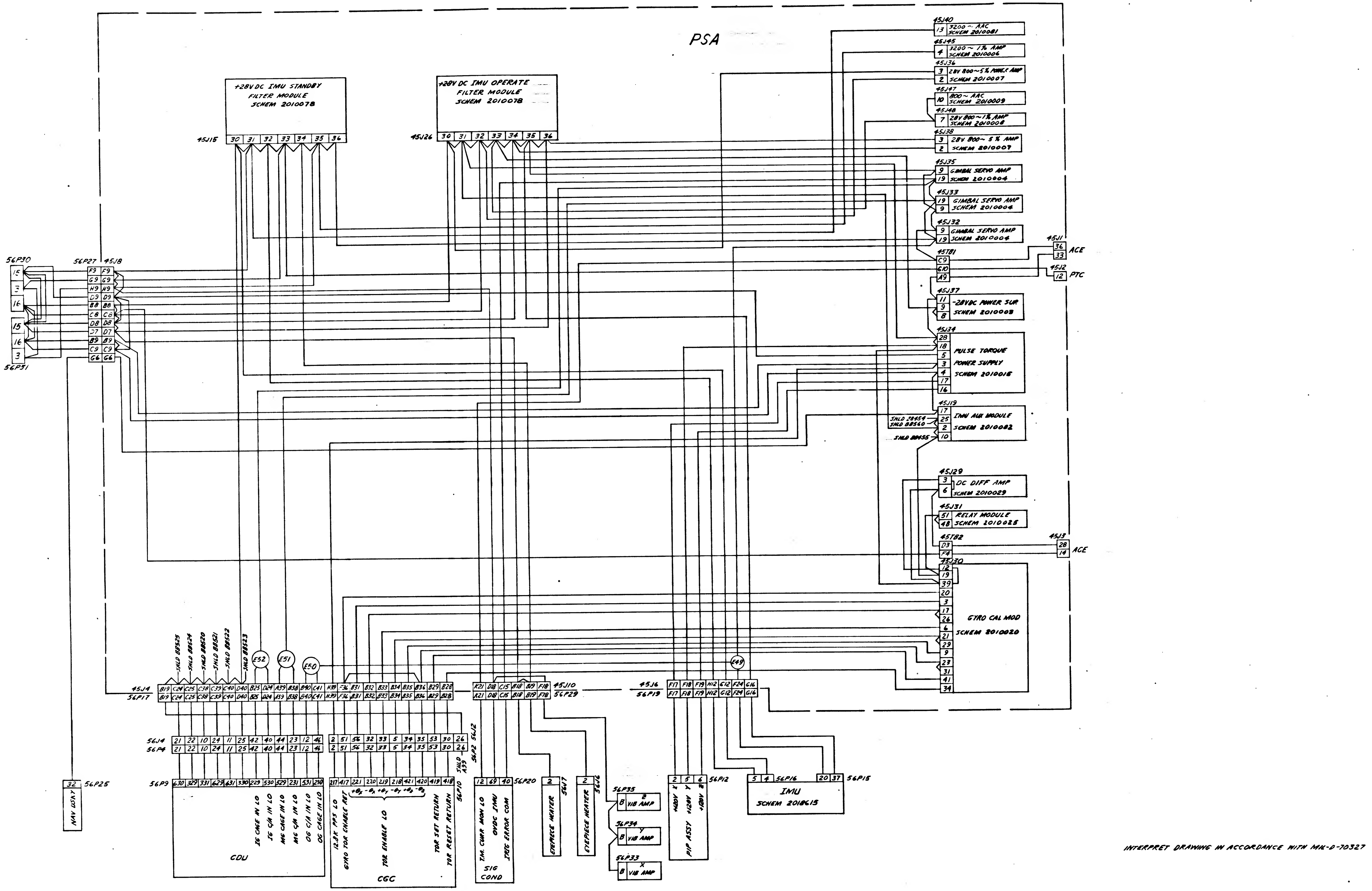
ZONE	LTR	DESCRIPTION	DR	CHK	DATE	APPROVED



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FIND NO.	QTY REQD	PART OR IDENT NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR SPECIFICATION

LIST OF MATERIALS

UNLESS OTHERWISE SPECIFIED
CAPACITOR VALUES ARE IN μf
RESISTOR VALUES ARE IN OHMS
ELECTRICAL TOLERANCES = ±5%

DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS DECIMALS ANGLES
± ± ±
DO NOT SCALE THIS DRAWING

MATERIAL

NEXT ASSY | USED ON
APPLICATION

DRAWN THENO 11-16-65
CHECKED 11-16-65
APPROVED
APPROVED

MIT APPROVED DATE 7 Dec 65
A. C. METZGER

INSTRUMENTATION LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
CAMBRIDGE, MASS.

OVDC IMU
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SIZE E | CODE IDENT NO. | DRAWING NO. 2015572
SCALE | SHEET

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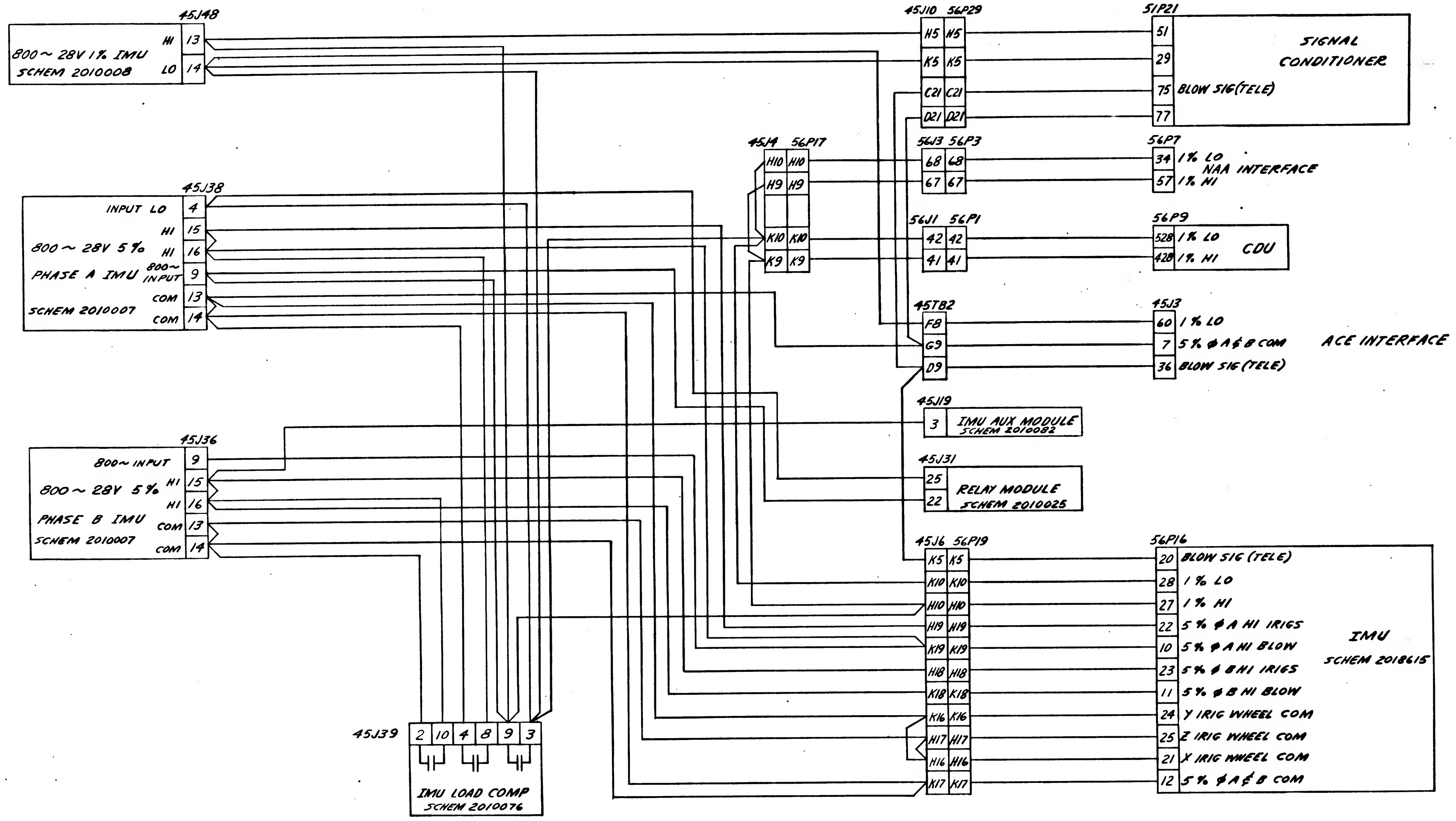
REVISIONS 24544

SYM	DESCRIPTION	DATE	APPROVAL



INTERPRET DRAWING IN ACCORDANCE WITH MIL-D-70327

MASTER

QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	FIND NO.

LIST OF MATERIALS

NEXT ASSY	USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS ± DECIMALS ± ANGLES ±
DO NOT SCALE THIS DRAWING
MATERIAL
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MIT
INSTRUMENTATION LAB
CAMBRIDGE, MASS.
DWG. NO. CONTRACT
DRAWN THENO DATE 10-25-65
CHECKED 11-1-65
APPROVAL 12/1/65
APPROVAL
NASA APPROVAL A. C. METZGER
MIT APPROVAL

MANNED SPACECRAFT CENTER
HOUSTON, TEXAS

800 ~ 1% & 5% IMU
POWER DISTRIBUTION
BLOCK II CSM

CODE IDENT NO.
SIZE D
NASA DRAWING NO. 2015573
SCALE
WT
SHEET 1 OF 1

2015573

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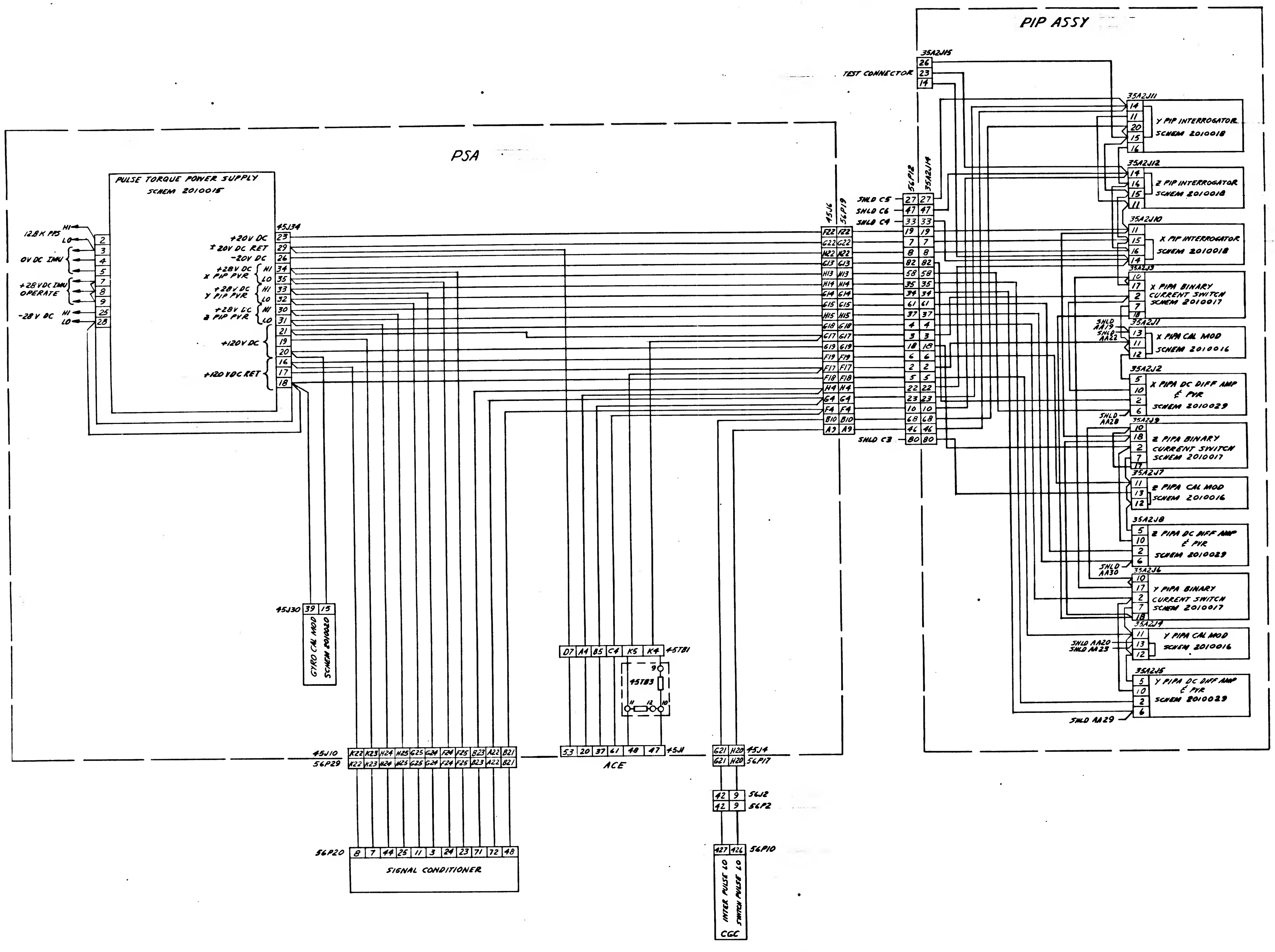
REVISIONS 24564

ZONE	LTR	DESCRIPTION	DR	CHK	DATE	APPROVED



INTERPRET DRAWING IN ACCORDANCE WITH MIL-D-70327

FIND NO.	QTY REQD	PART OR IDENT NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR SPECIFICATION

LIST OF MATERIALS

NEXT ASSY	USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED
CAPACITOR VALUES ARE IN µf
RESISTOR VALUES ARE IN OHMS
ELECTRICAL TOLERANCES = ±5%

DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS DECIMALS ANGLES
± ± ±
DO NOT SCALE THIS DRAWING

MATERIAL

DRAWN THENO -9-65
CHECKED J. Brown
APPROVED
APPROVED

MIT APPROVED W. Kupfer DATE 7 Dec 65
A. C. METZGER

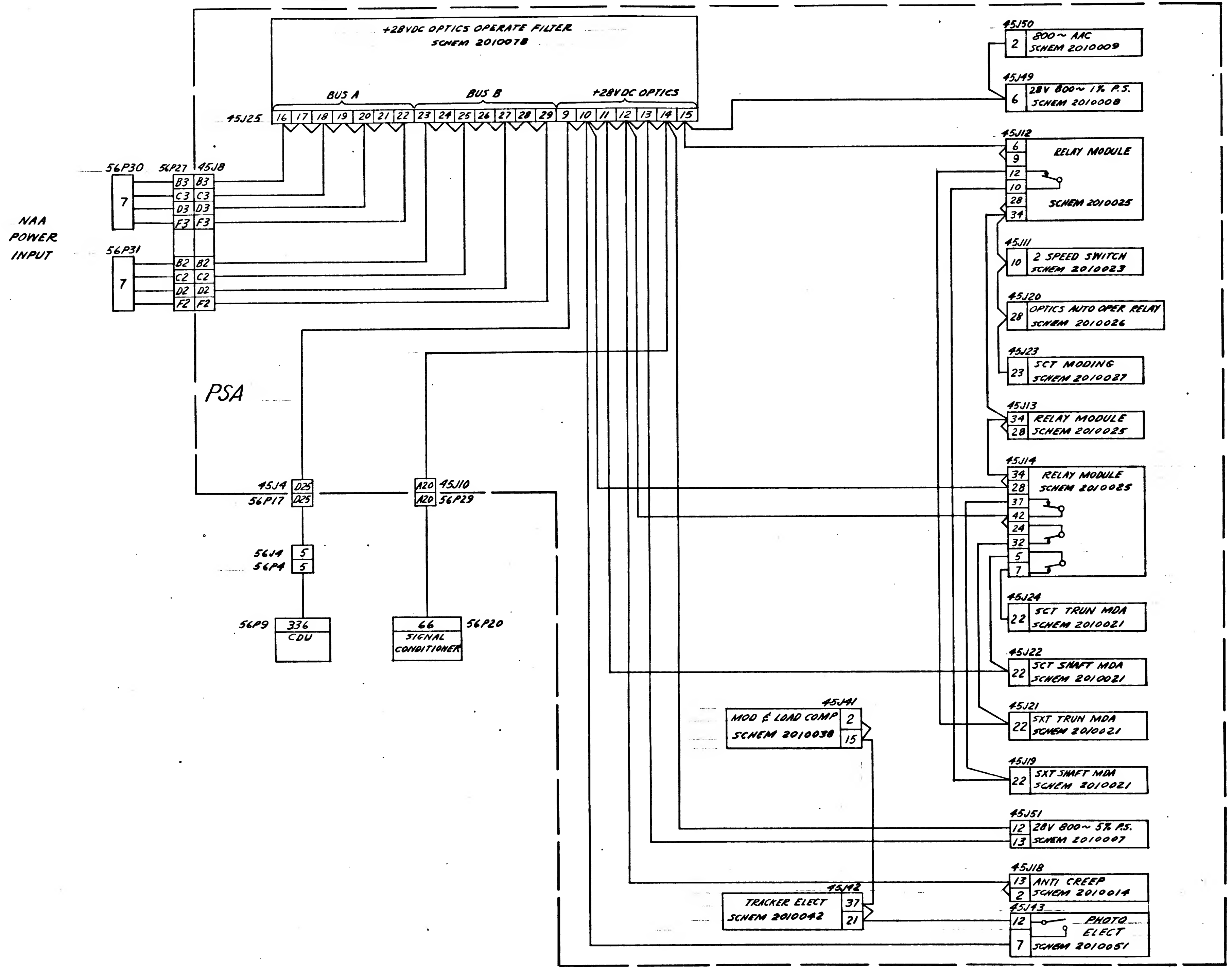
INSTRUMENTATION LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
CAMBRIDGE, MASS.

PULSE TORQUE POWER SUPPLY
OUTPUT DISTRIBUTION
BLOCK II G/M

SIZE E
CODE IDENT NO.
DRAWING NO. 2015574
SCALE
SHEET 1 OF 1

MASTER

REVISIONS 24544						
ZONE	LTR	DESCRIPTION	DR	CHK	DATE	APPROVED



INTERPRET DRAWING IN ACCORDANCE WITH MIL-D-70327

2015576

MASTER

FIND NO.	QTY REQD	PART OR IDENT. NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR SPECIFICATION

LIST OF MATERIALS

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
CAPACITOR VALUES ARE IN µf
RESISTOR VALUES ARE IN OHMS
ELECTRICAL TOLERANCES = ±5%

DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS DECIMALS ANGLES
± ± ±
DO NOT SCALE THIS DRAWING

MATERIAL

DRAWN THENO 10-3-65
CHECKED 10-4-65
APPROVED 11/1/65
APPROVED

MIT APPROVED DATE
W Kupfer 7 Dec 65
A. C. METZGER

INSTRUMENTATION LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
CAMBRIDGE, MASS.

+28V DC OPTICS OPERATE
DISTRIBUTION
BLOCK II G/M

SIZE D
CODE IDENT NO.
DRAWING NO. 2015576
SCALE
SHEET

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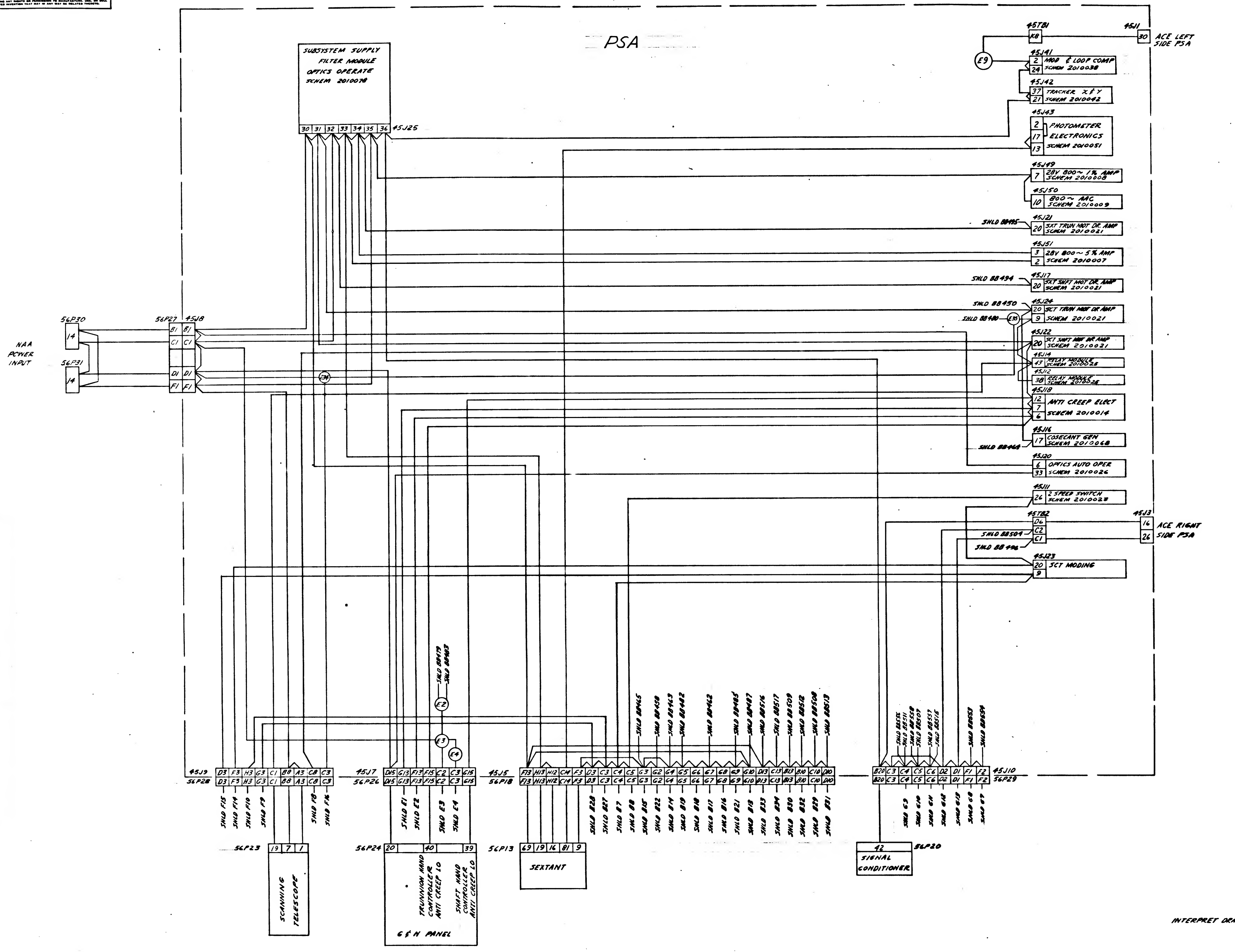
REVISIONS						
ZONE	LTR	DESCRIPTION	BY	CHK	DATE	APPROVED


PSA
SUBSYSTEM SUPPLY FILTER MODULE OPTICS OPERATE SCHEM 2010078
30 31 32 33 34 35 36 45J25
45TB1 K8
45J1 30 ACE LEFT SIDE PSA
E9
45J41 2 24 MOD & LOOP COMP SCHEM 2010038
45J42 37 21 TRACKER X & Y SCHEM 2010042
45J43 2 17 13 PHOTOMETER ELECTRONICS SCHEM 2010051
45J49 7 28V 800~ 1% AMP SCHEM 2010008
45J50 10 800~ AAC SCHEM 2010009
SHLD BB495
45J21 20 SXT TRUN MOT DR. AMP SCHEM 2010021
45J51 3 2 28V 800~ 5% AMP SCHEM 2010007
SHLD BB494
45J17 20 SXT SHFT MOT DR AMP SCHEM 2010021
SHLD BB450
SHLD BB480
E35
45J24 20 9 SCT TRUN MOT DR AMP SCHEM 2010021
45J22 20 SCT SHFT MOT DR AMP SCHEM 2010021
45J14 43 RELAY MODULE SCHEM 2010025
45J12 38 RELAY MODULE SCHEM 2010025
45J18 12 7 6 ANTI CREEP ELECT SCHEM 2010014
45J16 17 COSECANT GEN SCHEM 2010068
SHLD BB464
45J20 6 33 OPTICS AUTO OPER SCHEM 2010026
45J11 26 2 SPEED SWITCH SCHEM 2010023
45TB2 D6 C2 C1
SHLD BB509
SHLD BB496
45J3 16 26 ACE RIGHT SIDE PSA
45J23 20 9 SCT MODING
56P30 14
NAA POWER INPUT
56P31 14
56P27 45J8 B1 C1 D1 F1
E36
SHLD BB479
SHLD BB483
E2
E3
E4
45J9 56P28 D3 F3 H3 G3 C1 B8 A3 C8 C3
SHLD F15 SHLD F14 SHLD F10 SHLD F9 SHLD F8 SHLD F16
56P23 19 7 1
SCANNING TELESCOPE
45J7 56P26 D15 G13 F13 F15 C2 C3 G15
SHLD E1 SHLD E2 SHLD E3 SHLD E4
56P24 20 40 39
TRUNNION HAND CONTROLLER ANTI CREEP LO
SHAFT HAND CONTROLLER ANTI CREEP LO
G & N PANEL
45J5 56P18 F13 H13 H12 C14 F3 D3 C3 C4 C5 G3 G2 G4 G5 G6 G7 G8 G9 G10 D13 C13 B13 B10 C10 D10
SHLD BB465 SHLD BB458 SHLD BB463 SHLD BB482 SHLD BB462 SHLD BB485 SHLD BB487 SHLD BB516 SHLD BB517 SHLD BB509 SHLD BB512 SHLD BB508 SHLD BB513
SHLD B28 SHLD B27 SHLD B7 SHLD B8 SHLD B15 SHLD B22 SHLD B14 SHLD B19 SHLD B18 SHLD B17 SHLD B16 SHLD B21 SHLD B13 SHLD B33 SHLD B34 SHLD B30 SHLD B32 SHLD B29 SHLD B31
56P13 69 19 16 81 9
SEXTANT
SHLD BB556 SHLD BB511 SHLD BB558 SHLD BB507 SHLD BB557 SHLD BB516 SHLD BB653 SHLD BB654
45J10 56P29 B20 C3 C4 C5 C6 D2 D1 F1 F2
SHLD G9 SHLD G10 SHLD G11 SHLD G12 SHLD G13 SHLD G8 SHLD G7
42 56P20
SIGNAL CONDITIONER

INTERPRET DRAWING IN ACCORDANCE WITH MIL-D-70327

FIND NO.	QTY REQD	PART OR IDENT NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR SPECIFICATION

LIST OF MATERIALS

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
CAPACITOR VALUES ARE IN µf
RESISTOR VALUES ARE IN OHMS
ELECTRICAL TOLERANCES = ±5%

DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS DECIMALS ANGLES
± ± ±
DO NOT SCALE THIS DRAWING

MATERIAL

DRAWN THENO 11-18-65
CHECKED 11-22-65
APPROVED 12/1/65
APPROVED

MIT APPROVED DATE 7 Dec 65
A. C. METZGER

INSTRUMENTATION LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
CAMBRIDGE, MASS.

OVOC OPTICS
DISTRIBUTION
BLOCK II C/M

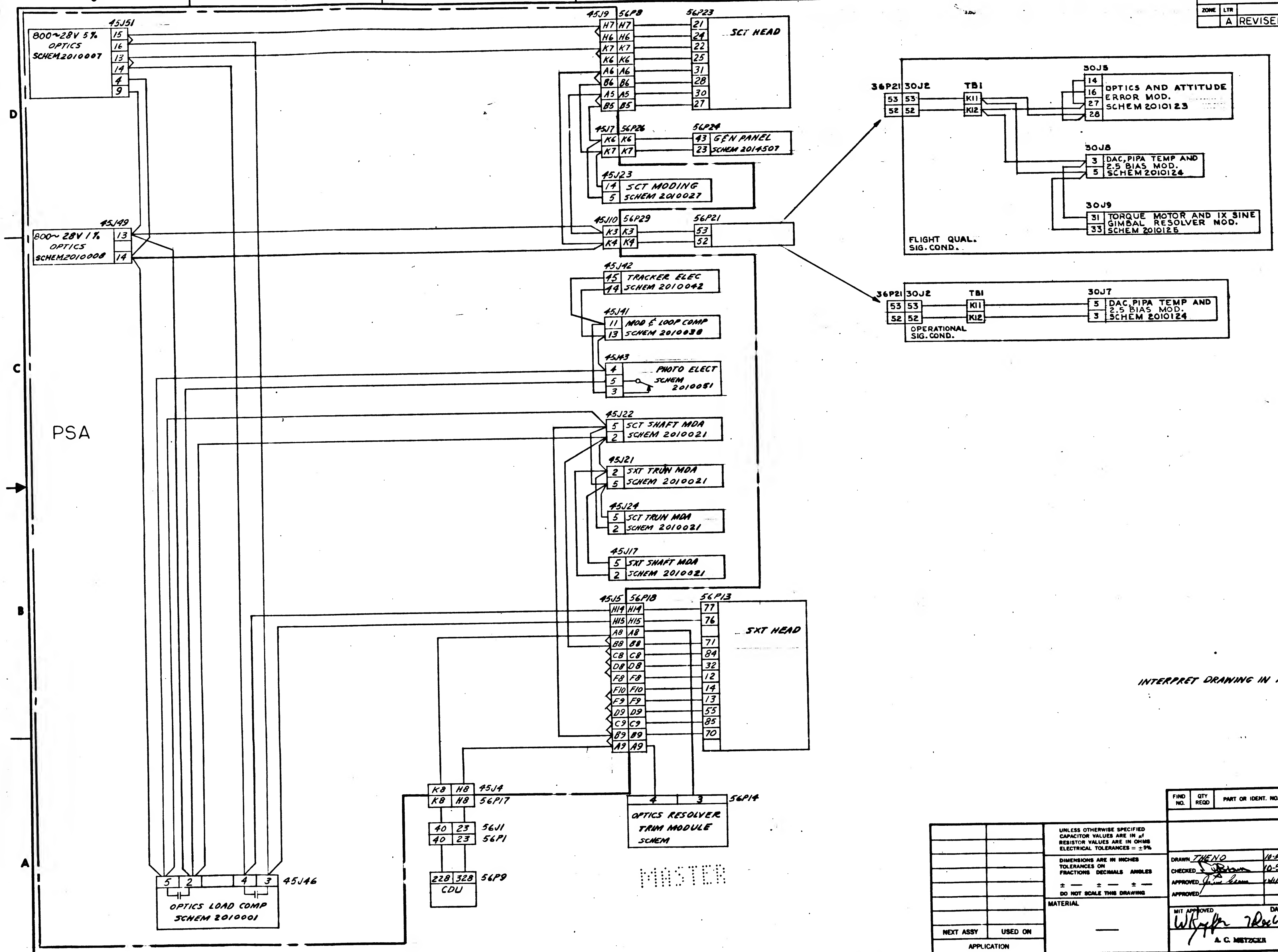
SIZE E
CODE IDENT NO.
DRAWING NO. 2015577
SCALE
SHEET 1

MASTER

2015577

REVISIONS 24544

ZONE	LTR	DESCRIPTION	DR	CHK	DATE	APPROVED
	A	REVISED PER TDRR 30387	EJM		8-1-66	



MASTER

INTERPRET DRAWING IN ACCORDANCE WITH MIL-D-70327

FIND NO.	QTY REQD	PART OR IDENT. NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR SPECIFICATION

LIST OF MATERIALS

NEXT ASSY	USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED
CAPACITOR VALUES ARE IN µf
RESISTOR VALUES ARE IN OHMS
ELECTRICAL TOLERANCES = ±5%

DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS DECIMALS ANGLES
± — ± — ± —
DO NOT SCALE THIS DRAWING

MATERIAL
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DRAWN THENO 10-5-65
CHECKED 10-5-65
APPROVED
APPROVED

MIT APPROVED DATE 7 Dec 65
A. C. METZGER

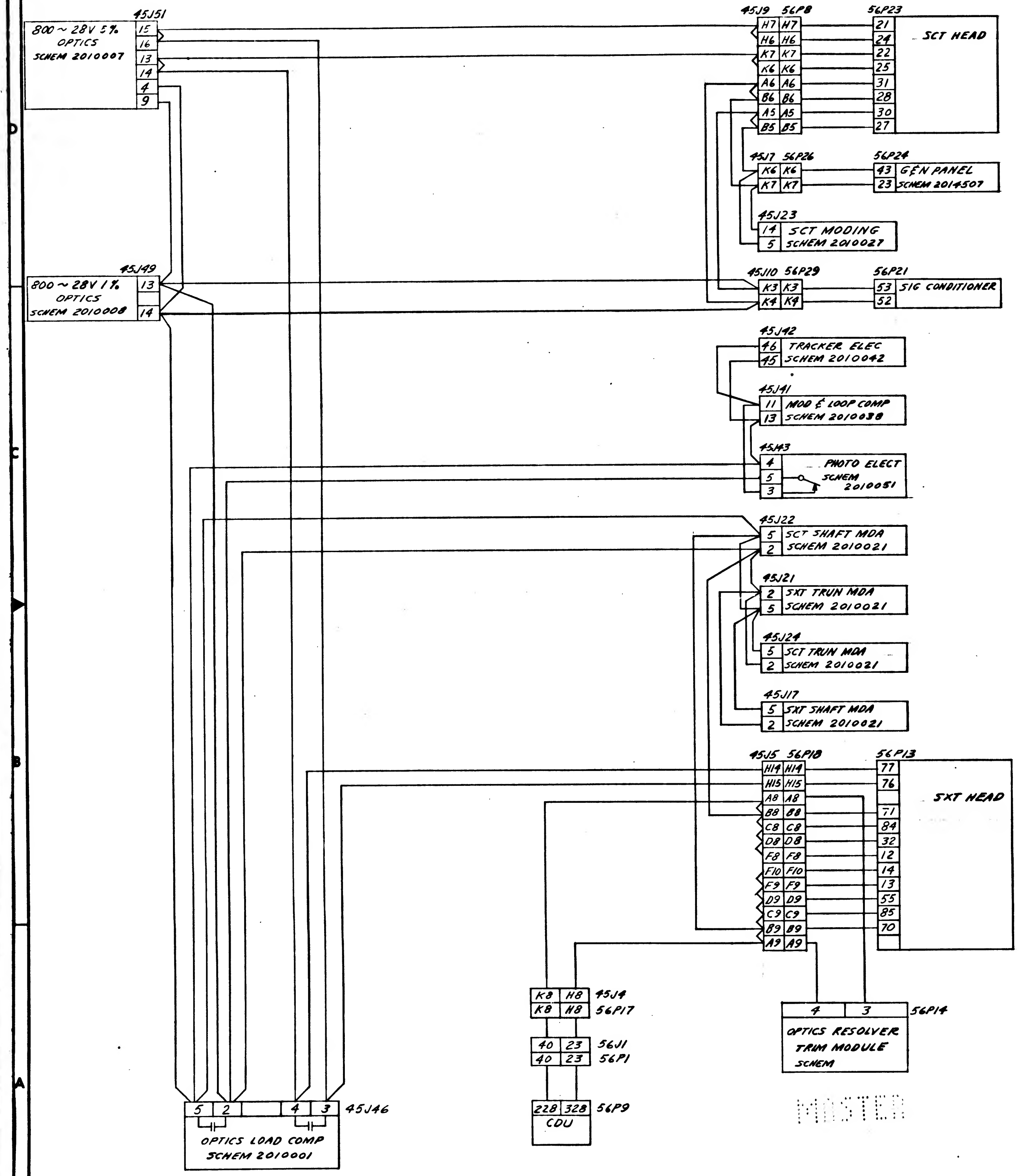
INSTRUMENTATION LABORATORY
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
CAMBRIDGE, MASS.

+28V 800~ 1% & 5%
OPTICS POWER DISTRIBUTION
BLOCK II G/M

SIZE D
CODE IDENT NO.
DRAWING NO. 2015578
SCALE —
SHEET OF 1

2015578 A

ZONE	LTR	DESCRIPTION	DR	CHK	DATE	APPROVED
		REVISIONS 24544				



MASTER

INTERPRET DRAWING IN ACCORDANCE WITH MIL-D-70327

2015578

FIND NO.	QTY REQD	PART OR IDENT. NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR SPECIFICATION

LIST OF MATERIALS

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
CAPACITOR VALUES ARE IN µf
RESISTOR VALUES ARE IN OHMS
ELECTRICAL TOLERANCES = ±5%

DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS DECIMALS ANGLES
± ± ±
DO NOT SCALE THIS DRAWING

MATERIAL

DRAWN THENO 10-5-65
CHECKED 10-5-65
APPROVED 12/1/65
APPROVED

MIT APPROVED DATE 7Dec65
A. C. METZGER

INSTRUMENTATION LABORATORY
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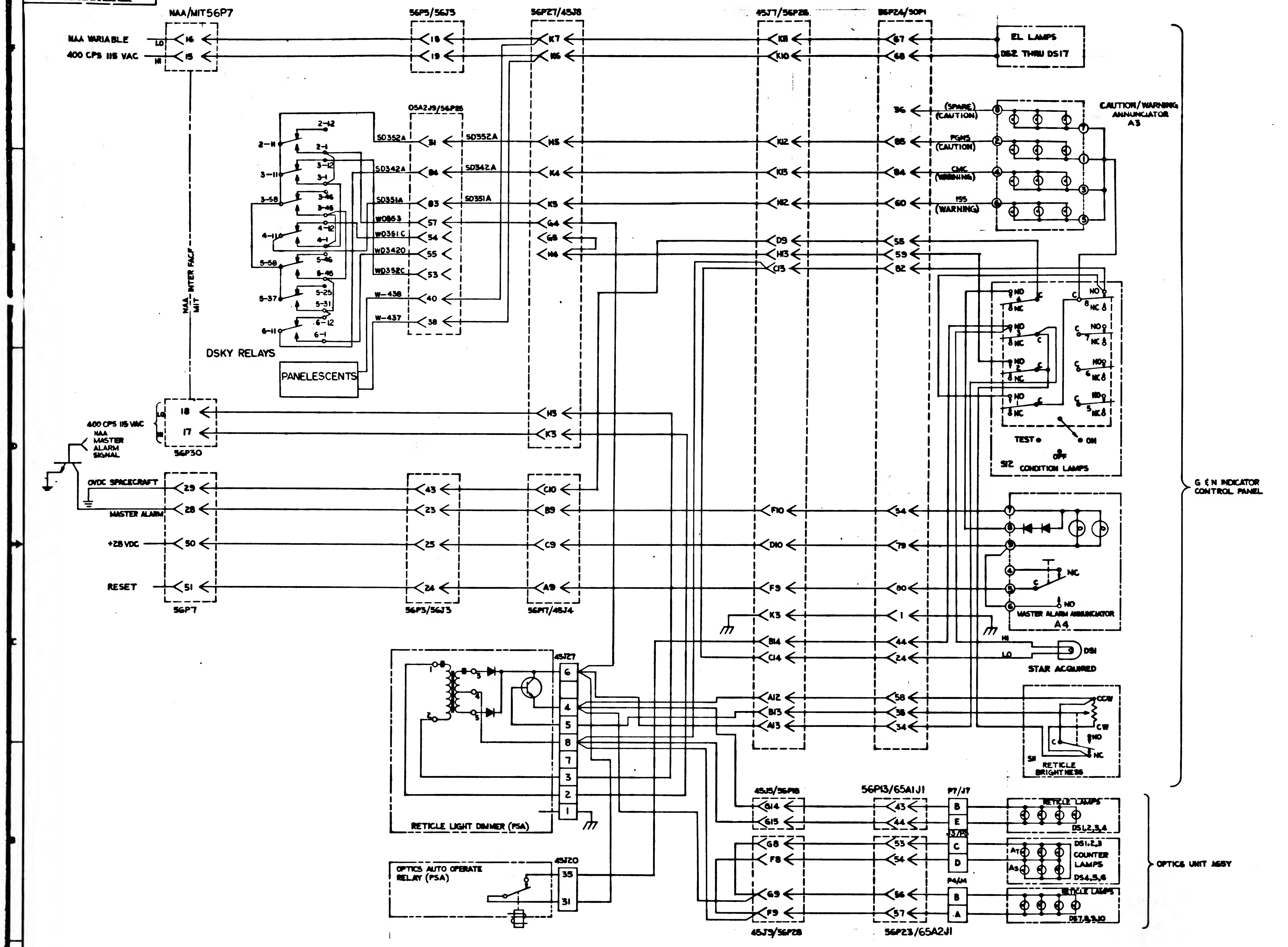
CAMBRIDGE, MASS.

+28V 800~ 1% & 5%
OPTICS POWER DISTRIBUTION
BLOCK II G/M

SIZE D
CODE IDENT NO.
DRAWING NO. 2015578
SCALE
SHEET

REVISIONS TDRR-3630

SYM	ZONE	DESCRIPTION	DR	CHK	DATE	APPROVED



QTY REQD	PART OR IDENTIFYING NO.	MATERIAL OR NOTES	NOMENCLATURE OR DESCRIPTION	FIND NO.

LIST OF MATERIALS

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
CAPACITOR VALUES ARE IN µf
RESISTOR VALUES ARE IN OHMS
TOLERANCES ON
FRACTIONS DECIMALS ANGLES
± —— ± —— ± ——
DO NOT SCALE THIS DRAWING

MATERIAL

NEXT ASSY	USED ON
APPLICATION	

MIT
INSTRUMENTATION LAB
CAMBRIDGE, MASS.

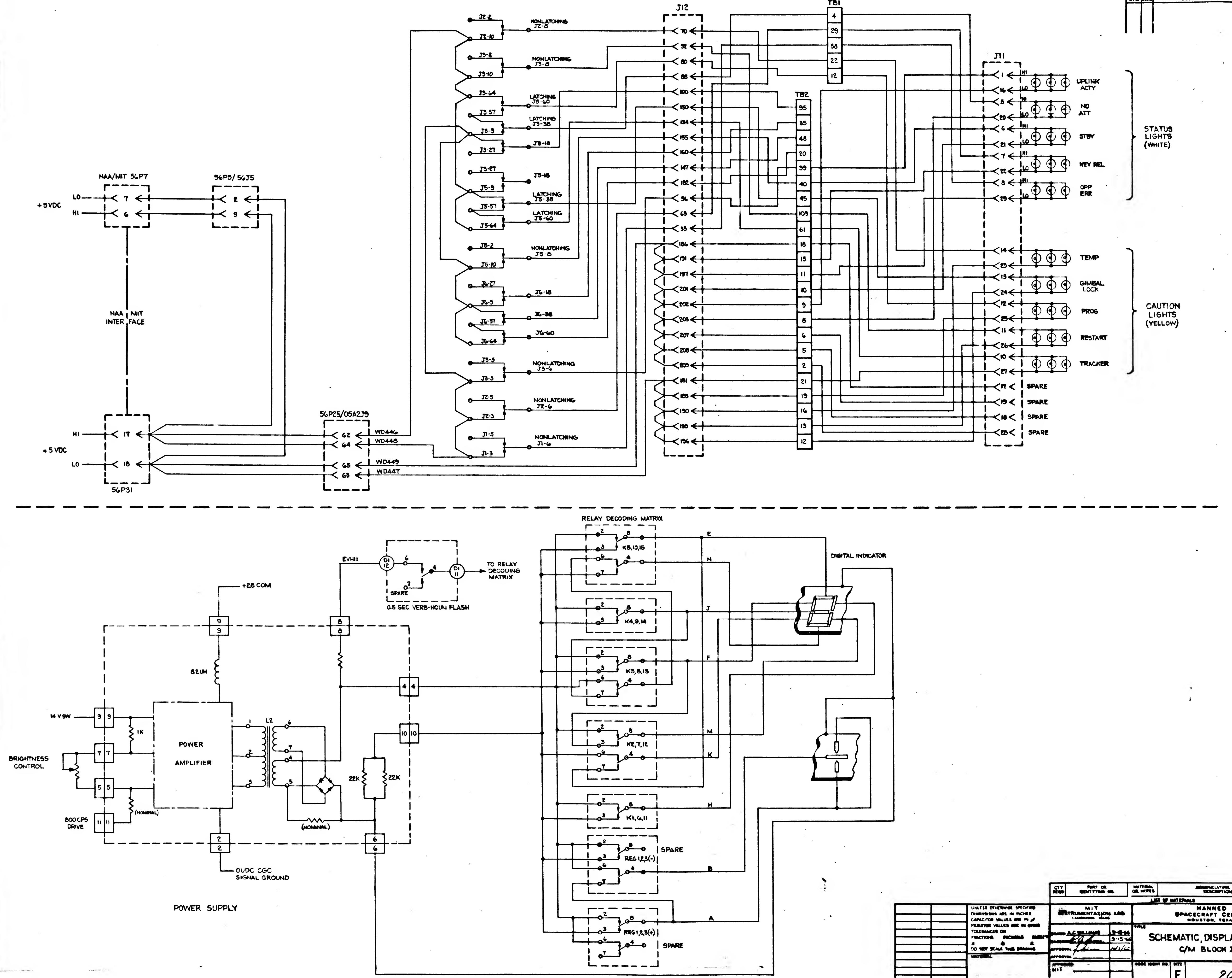
MANNED SPACECRAFT CENTER
HOUSTON, TEXAS

DRAWN J. Friedrich 2/7/66
CHECKED
APPROVED J. Brown 1-17-66
APPROVED
APPROVED MIT
APPROVED MSC

SCHEMATIC, DISPLAY CIRCUIT
C/M BLOCK II

CODE IDENT NO.
SIZE E
DRAWING NO. 2015579
SCALE NONE
SHEET OF 2
DATE

REVISIONS IDRR 31630				
SYM	ZONE	DESCRIPTION	DATE	APPROVAL



QTY REQD	PART OR IDENTIFYING NO.	MATERIAL OR NOTES	NOMENCLATURE OR DESCRIPTION	FIND NO.

LIST OF MATERIALS

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
CAPACITOR VALUES ARE IN µf
RESISTOR VALUES ARE IN OHMS
TOLERANCES ON
FRACTIONS DECIMALS ANGLES
± ± ±
DO NOT SCALE THIS DRAWING
MATERIAL

MIT
INSTRUMENTATION LAB
CAMBRIDGE MASS

DRAWN A.C. WILLIAMS 9-13-66
CHECKED 9-15-66
APPROVAL
APPROVAL
APPROVED MIT
APPROVED MSC
DATE

MANNED
SPACECRAFT CENTER
HOUSTON, TEXAS

TITLE
SCHEMATIC, DISPLAY CIRCUIT
C/M BLOCK II

CODE IDENT NO.
SIZE E
2015579
SCALE NONE
WEIGHT
CALC ACTUAL
SHEET 2 OF 2

2015579

APOLLO G&N Specification
PS 2016000 Rev. -
Original Issue Date: 23 NOV 65
Release Authority: TDRR 24230
Class A Release

PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

PROGRAM ANALYZER CONSOLE

~~DWG. NO. 189951~~

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA

This specification consists of pages 1 to 22 inclusive.

APPROVALS	C. METZGER NASA/MSC	EC Hall 11/23/65 W Kupfer 23 Nov 65 MIT/IL	11-22-65 K. 11/22/65 11/22/65 RAY 11/22/65

3.1 **Performance.** The Program Analyzer Console (PAC) is a double-rack console consisting of twenty-seven major units or sub assemblies. The units form an integrated group capable of simulating all or part of the AGC (APOLLO Guidance Computer) fixed memory, actively controlling the AGC, and actively and passively monitoring the AGC.

3.1.1 **Input Power.** The assembly shall perform as specified herein when supplied with 220 ± 10 VRMS, 3 phase, 54 to 66 CPS at a maximum of 30.0 amperes.

3.1.2 **Power Supply.** The power supply shall consist of four DC power supplies to provide unloaded sources of 3.0 ± 0.5 VDC, 10.0 ± 1.0 VDC and two 13.0 ± 1.3 VDC.

3.1.2.1 **Logic Power.** 3.0 ± 0.2 VDC shall be supplied to the logic through the Power ON/Ready and DC Distribution switches located on the Power Control panel.

3.1.2.2 **Indicator Power.** 10.0 ± 0.8 VDC shall be supplied to the indicators through the Power ON/Ready and DC Distribution switches located on the Power Control panel.

3.1.2.3 **Memory A and Memory B Power.** 13.0 + 0.7 VDC shall be supplied to the nine Memories from two separate supplies, through the Power ON/Ready and DC Distribution switches located on the Power Control panel.

3.1.3 **Blower Operation.** The Ventilating Blower, a commercial unit, shall be used in conjunction with a central plenum chamber to air cool the PAC interior. The blower shall have maximum power consumption characteristics as follows: single phase, 60 CPS, 3.0 amperes at 115 VRMS.

3.1.4 **Tape Reader and Spooler.** The Tape Reader shall contain the mechanism to read punched tape and shall operate in a 522 mode. The Tape Spooler is bi-directional and shall operate in conjunction with the Tape Reader. Both units shall have a tape capacity of one inch tape containing eight standard code channels and each unit shall utilize single phase, 60 CPS, 115 VAC power through a three wire system.

3.1.5 **Clock Signal.** The 2 megacycle clock signal shall be adjusted to have the following characteristics when measured at the output of the Oscillator Alarm and Clock Gating Circuits. Figure 3-1 defines the signal characteristics measurement area.

a	Amplitude (A1)	NMT 0.350 V
b	Amplitude (A2)	1.2 ± 0.3 V
c	Risetime (tr)	NMT 100 usec
d	Fall time (tf)	NMT 80 usec
e	Pulse Width (PW)	0.25 ± 0.012 usec
f	Period Time (T)	0.5 ± 0.025 usec

APOLLO G&N Specification
PS 2016004 Rev. A 5-6
Original Issue Date:
Release Authority: TDRR 28613
Class A Release

PROCUREMENT SPECIFICATION
PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS
AGC/GSE INTERCONNECTION SET
G&N TEST
DRAWING NO. 2014255

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA
Ⓜ 8/11/66	A	30564	1 & 3	FM	FM

This specification consists of pages 1 to 4 inclusive.

APPROVALS	A. C. METZGER NASA/MSC	MIT/IL	4/26/66 4/26/66 RAY 4/26/66

1. SCOPE

This specification establishes the detail requirements for complete identification and acceptance of the AGC/GSE Interconnection Set, G&N Test, Part No. 2014255-021 and 2014255-031.

2. APPLICABLE DOCUMENTS. Same as PS 2014255.

3. REQUIREMENTS. Same as PS 2014255 with the following exceptions.

3.1.4.6 The resistance between J1-F and each of the following pins shall be 3.3K ± 5% ohms.

J4-T
J4-U
J4-n
J4-$\overline{W}$
J4-GG
J4-t
J4-$\overline{d}$
J4-$\overline{c}$
J4-$\overline{v}$
J4-$\overline{u}$
J4-$\overline{L}$
J4-P
J4-E
J4-i
J4-$\overline{J}$
J4-$\overline{X}$
J6-JJ
J6-BB
J6-NN

J6-AA
J6-m
J6-$\overline{k}$
J6-$\overline{Z}$
J6-D
J6-X
J6-u
J6-$\overline{v}$
J6-$\overline{e}$
J6-$\overline{d}$
J6-$\overline{W}$
J6-t
J6-$\overline{GG}$
J6-HH
J6-w
J6-$\overline{V}$
J6-S
J6-FF
J5-z
J5-$\overline{T}$

J5-$\underline{g}$
J5-$\underline{p}$
J5-$\overline{BB}$
J5-CC
J5-m
J5-$\overline{k}$
J5-$\overline{V}$
J5-$\underline{c}$
J5-$\overline{w}$
J5-$\overline{AA}$
J5-HH
J5-s
J5-$\overline{FF}$
J5-NN
J5-JJ
J5-$\underline{e}$
J5-$\overline{x}$
J5-$\overline{r}$
J5-$\overline{EE}$
J5-U

J5-F
J5-C
J5-GG
J5-d
J5-$\overline{W}$
J5-v
J5-$\overline{X}$
J5-$\underline{t}$
J5-$\overline{u}$
J5-$\overline{LL}$
J5-DD
J5-$\underline{q}$
J5-$\overline{f}$
J5-$\overline{y}$
J5-$\overline{KK}$
J5-PP
J5-MM
J5-P
J5-R
J5-M

3.1.4.7 The resistance between J1-$\underline{h}$ and each of the following pins shall be 3.3K ± 5% ohms.

J6-$\underline{x}$
J6-$\overline{e}$
J6-$\overline{r}$
J6-$\overline{EE}$
J6-MM
J6-CC

J6-FF
J6-KK
J6-$\underline{y}$
J6-$\overline{f}$
J6-$\overline{q}$

J6-DD
J6-LL
J6-$\underline{z}$
J6-$\overline{g}$
J6-$\underline{p}$

APOLLO G&N Specification
PS 2016004 Rev. -
Original Issue Date: 5-6
Release Authority: TDRR 28613
Class A Release

PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

AGC/GSE INTERCONNECTION SET

G&N TEST

DRAWING NO. 2014255

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA

This specification consists of pages 1 to 4 inclusive.

APPROVALS	A. C. METZGER NASA/MSC	5/6/66 5/10/66 MIT/IL	4/26/66 4/26/66 RAY

1. SCOPE

This specification establishes the detail requirements for complete identification and acceptance of the AGC/GSE Interconnection Set, G&N Test, Part No. 2014255-021.

2. APPLICABLE DOCUMENTS. Same as PS 2014255.

3. REQUIREMENTS. Same as PS 2014255 with the following exceptions.

3.1.4.6 The resistance between J1-F and each of the following pins shall be 3.3K ± 5% ohms.

J4-T
J4-U
J4-n
J4-W
J4-GG
J4-t
J4-d
J4-c
J4-v
J4-u
J4-L
J4-P
J4-E
J4-i
J4-J
J4-X
J6-JJ
J6-BB
J6-NN

J6-AA
J6-m
J6-k
J6-E
J6-D
J6-X
J6-u
J6-v
J6-c
J6-d
J6-W
J6-t
J6-GG
J6-HH
J6-w
J6-V
J6-S
J6-FF
J5-z
J5-T

J5-g
J5-p
J5-BB
J5-CC
J5-m
J5-k
J5-V
J5-e
J5-w
J5-AA
J5-HH
J5-s
J5-FF
J5-NN
J5-JJ
J5-e
J5-x
J5-r
J5-EE
J5-U

J5-F
J5-C
J5-GG
J5-d
J5-W
J5-v
J5-X
J5-t
J5-u
J5-LL
J5-DD
J5-q
J5-f
J5-y
J5-KK
J5-PP
J5-MM
J5-P
J5-R
J5-M

3.1.4.7 The resistance between J1-h and each of the following pins shall be 3.3K ± 5% ohms.

J6-x
J6-e
J6-r
J6-EE
J6-MM
J6-CC

J6-PP
J6-KK
J6-y
J6-f
J6-q

J6-DD
J6-LL
J6-z
J6-g
J6-p

APOLLO G&N Specification
PS 2016006 Rev. A
Original Issue Date: 6/3/66
Release Authority: TDRR 29267
Class A Release

PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

COMPUTER TEST SET ASSEMBLY

DRAWING NO. 2014042

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA
7/21/66	A	30169	1 and 3		

This specification consists of pages 1 to 7 inclusive.

APPROVALS
NASA/MSC
MIT/IL
E.A. Olsen
14 May 1966
RAY
5-19-66
5/19/66
5/19/66

1. SCOPE

This specification establishes the detail requirements for complete identification and acceptance of the Computer Test Set Assembly, Part Number 2014042-031 or -041, hereinafter called CTS.

2. APPLICABLE DOCUMENTS. Same as PS 2014042.

3. REQUIREMENTS

3.1 PERFORMANCE. Same as PS 2014042.

3.1.1 Input Power. Same as PS 2014042.

3.1.2 Auxiliary Outlets. Same as PS 2014042.

3.1.3 Test Time Indicator. Same as PS 2014042.

3.1.4 AGC Stops. Same as PS 2014042.

3.1.5 AGC Read. Same as PS 2014042.

3.1.6 AGC Load. Same as PS 2014042.

3.1.7 Transfer Control. Same as PS 2014042.

3.1.8 Channel. Same as PS 2014042.

3.1.9 Monitor. Same as PS 2014042.

3.1.10 Record. Same as PS 2014042.

3.1.11 Tape Operations. Same as PS 2014042.

3.1.12 AGC Counter. Same as PS 2014042.

3.1.13 Inhibit-Bank Restore. Same as PS 2014042.

3.1.14 Scaler. Same as PS 2014042.

3.1.15 Fresh Start. Same as PS 2014042.

3.1.16 Inhibits. Same as PS 2014042.

3.1.17 System-Subsystem Test. Same as PS 2014042.

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PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

COMPUTER TEST SET ASSEMBLY

DRAWING NO. 2014042

Record of Revisions

	Date	Revision Letter	TDRR No.	Pages Revised	Approvals MIT	Approvals NASA
Ⓜ	7/21/66	A	30169	1 and 3		
Ⓜ	9/22/66	B	31284	1 and 3		

This specification consists of pages 1 to 7 inclusive.

APPROVALS	NASA/MSC	E.A. Olsson 19 May 1966 MIT/IL	5-19-66 5/19/66 5/19/66 RAY

1. SCOPE

This specification establishes the detail requirements for complete identification and acceptance of the Computer Test Set Assembly, Part Numbers 2014042-031, or -041 or -051 hereinafter called CTS.

2. APPLICABLE DOCUMENTS. Same as PS 2014042.

3. REQUIREMENTS

3.1 PERFORMANCE. Same as PS 2014042.

3.1.1 Input Power. Same as PS 2014042.

3.1.2 Auxiliary Outlets. Same as PS 2014042.

3.1.3 Test Time Indicator. Same as PS 2014042.

3.1.4 AGC Stops. Same as PS 2014042.

3.1.5 AGC Read. Same as PS 2014042.

3.1.6 AGC Load. Same as PS 2014042.

3.1.7 Transfer Control. Same as PS 2014042.

3.1.8 Channel. Same as PS 2014042.

3.1.9 Monitor. Same as PS 2014042.

3.1.10 Record. Same as PS 2014042.

3.1.11 Tape Operations. Same as PS 2014042.

3.1.12 AGC Counter. Same as PS 2014042.

3.1.13 Inhibit-Bank Restore. Same as PS 2014042.

3.1.14 Scaler. Same as PS 2014042.

3.1.15 Fresh Start. Same as PS 2014042.

3.1.16 Inhibits. Same as PS 2014042.

3.1.17 System-Subsystem Test. Same as PS 2014042.

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PROCUREMENT SPECIFICATION
PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS
APOLLO GUIDANCE COMPUTER SUBSYSTEM
DRAWING NO. 2003991

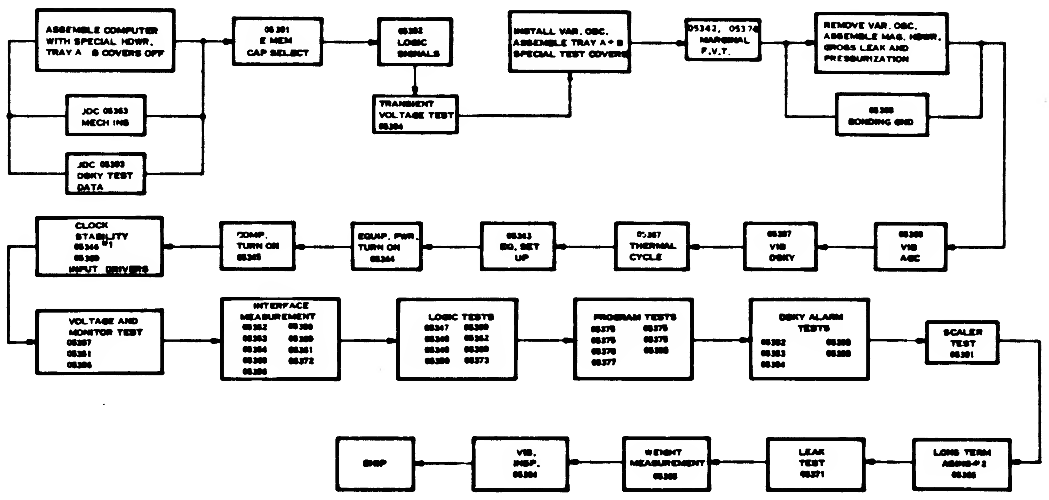
Record of Revisions

Ⓜ Ⓜ

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA
3-2-67	A	33144	1, 89	EMS	EMS

This specification consists of pages 1 to 114 inclusive.

APPROVALS	NASA/MSC	EC Hall 12/13 WStameris 14 Dec 66 MIT/IL	RAY



NOTES

# 1. THIS JDC IS PERFORMED CONTINUALLY

# 2. THIS JDC IS PERFORMED IN PARALLEL WITH OTHER OPERATING JDC'S.

3. IF MORE THAN ONE JDC IS LISTED IN A BOX THE PERFORMANCE SEQUENCE IS NOT CRITICAL, THEREFORE, THEY MAY BE PERFORMED IN ANY CONVENIENT ORDER.

ASSEMBLY TEST PLAN

APOLLO G&N Specification
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PROCUREMENT SPECIFICATION
PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS
APOLLO GUIDANCE COMPUTER SUBSYSTEM
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Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA
3-2-67	A	33144	1, 89		
4-13-67	B	33607	1,2,81,82,88,89	FM	FM

This specification consists of pages 1 to 115 inclusive.

APPROVALS	NASA/MSC	EC Hall W Stameris 14 Dec 66 MIT/IL	RAY

1.0 SCOPE

This specification establishes the detail requirements for complete identification and acceptance of all units of the Apollo Guidance Computer, Part Numbers 2003200-011,-021,-031 and 2003993-021, hereinafter called AGC and the Display and Keyboard Assy, Part Number 2003994-011, hereinafter called DSKY.

2.0 APPLICABLE DOCUMENTS

2.1 EFFECTIVE ISSUES. The following documents form a part of this specification to the extent specified herein. Unless otherwise specified, Military Standards and Specifications shall be the issue in effect on the date of request for proposal or invitation to bid.

SPECIFICATIONS

APOLLO G&N

ND 1002214	General Specification for Preservation, Packaging, Packing and Container Marking of APOLLO Guidance and Navigation Major Assemblies, Assemblies, Subassemblies, Parts and Associated Ground Support Equipment.

DRAWINGS

APOLLO G&N

2003991	APOLLO Guidance Computer Subsystem

(Copies of specifications, standards, drawings, bulletins, and publications required by suppliers in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer).

2.2 CONFLICTING REQUIREMENTS. In event of a conflict between requirements, the following order of precedence shall apply. The contractor shall also notify MIT/IL APOLLO Management of the conflict.

a. The contract
b. This specification
c. Documents listed in this section

3.1.7 **Leak Rate.** With the computer pressurized to 30.0 ± 1.0 psia with dry nitrogen at 25°C ± 2C°, the leak rate shall not exceed 1.0 psia for a period of 24.0 ± 0.5 hours. With the DSKY pressurized to 2 psig at 25°C ± 2°C using a mixture of 90% nitrogen and 10% helium the leak rate shall not exceed 1 x 10^{-3} cc/sec/atm.

3.1.8 **Aging.** The AGC Subsystem shall have accumulated not less than two hundred hours operating time prior to completion of test.

3.1.9 **Miscellaneous Signals.**

3.1.9.1 Signal W-910 (CNTRL 1) (2000-ohm short to ground) shall force the output of the +4 VDC power supply to 3.40 ± 0.01 VDC and 4.50 ± 0.01 VDC.

3.1.9.2 Signal W-911 (CNTRL 2) (2000-ohm short to ground) shall force the output of the +14 VDC power supply to 12.10 ± 0.01 VDC and 16.40 ± 0.01 VDC.

3.1.9.3 Signal D-912 (NHVFAL) shall inhibit RESTART due to voltage fail condition.

3.1.10 **Spare and Not Connected Terminals.** The following AGC connector A51 and DSKY connector J9 pins are provided as spare and NC terminals.

Connector A51 Pin Numbers	Connector J9 Pin Numbers	Signal	Designation
115	75	W-210	SPARE
-	74	W-213	SPARE
116	73	W-241	SPARE
-	13	W-246	SPARE
-	34 (N)	SD326	SPARE
-	37 (N)	SD328	SPARE
-	56 (M)	SD444	SPARE
-	34 (M)	SD445	SPARE
141	-	A-859	NC
140	-	A-860	NC
-	-	RD875	4/7/68
-	-	--908	-
413	-	CB028	NC

3.1.11 Bonding Continuity. The resistance measured between the items listed in Table 3-16 shall not exceed the value specified in Table 3-16.

TABLE 3-16

From	To	Resistance
Tray B Cover (Magnesium Surface) -	Tray A Cover (Magnesium Surface) -	20 milliohms
Tray A - (Brass to Magnesium Surface)	Mid Spacer (Magnesium Surface)	20 milliohms
Tray B Cover - (Magnesium Surface)	Baby Tray - (Screw to helicoil to Magnesium Surface)	30 milliohms

3.1.12 Transient Susceptibility. With the computer exercised by a rope program and with transient voltage spikes, as specified below, applied to the positive and negative 28 volt input power lines of the computer; there shall be no evidence of transient susceptibility.

Transient Voltage Spikes
(Output of Test Circuitry Prior to Application to 28 Volt lines)

Amplitude	50 ± 2 volts
Pulse Width	10.0 ± 4.0 usec at the 5 volt level
Pulse Rate	10 pps
Rise Time	1 usec max (10% to 90%)
Polarity	Positive

3.2 PRODUCT CONFIGURATION

3.2.1 Drawings. The configuration of the assembly shall be in accordance with Apollo G&N Drawings 2003200-011,-021,-031, 2003993-011 and 2003993-021 and all drawings and engineering data referenced thereon.

3.2.2 Weight. The weight of the computer and DSKY shall be measured and recorded.

4. QUALITY ASSURANCE PROVISIONS

4.1 GENERAL. The contractor responsible for the manufacture of the assembly shall be responsible for the accomplishment of each test required herein. See Table 4-1, Product Performance and Configuration Requirements/Quality Verification Cross Reference Index.

4.1.1 Test Conditions

4.1.1.1 Environmental. The assembly shall be tested under the following ambient conditions:

a. Temperature: 25° ± 10°C

b. Relative Humidity: 90% max

c. Barometric Pressure: 28 to 32 inches of Hg

4.1.2 Nonconforming Units. Failure of the unit to pass any examination or test of this specification shall automatically classify the unit as nonconforming. Each nonconforming unit corrected by the contractor shall be reinspected. Reinspection may be limited to the test or examination which defined the nonconformance, or, when directed by the cognizant inspector, a complete retest and re-examination may be required. Nonconforming units which have not been corrected will be considered for acceptance only upon formal application by the contractor to the cognizant NASA representative. Any module replaced during testing shall have operated in the system under test for not less than fifty hours, shall be thermal cycled, and vibrated and the assembly shall be leak tested prior to final acceptance.

4.2 TESTS/VERIFICATIONS

4.2.1 Drawing Compliance. The assembly shall be visually examined for compliance to the requirements of APOLLO G&N Drawing 2003991. Particular attention shall be given to inspection for damage to surfaces, structure, and equipment, including contaminants, pin misalignment, and legibility and appearance of marking.

4.2.2 Acceptance Tests. All tests shall be performed using the JDC's listed herein in the order specified in the Assembly Test Plan.

4.2.2 (Continued)

a. The Acceptance Tests must be performed with one (1) Computer and two (2) Dsky's. If any of the units are missing, Hangar Queen units shall be used during the tests. (*)
The Hangar Queen units shall not be subjected to mechanical inspection, vibration, thermal cycling, weight measurement, leak test or to the requirements of long term aging or Test Data JDC. A failure isolated to a Hangar Queen shall not be cause for rejection of the unit undergoing acceptance tests.

b. To perform the tests specified herein, Fixed Memory Modules containing Newspeak Program are required in the B1 and B2 positions and Warning Test Rope Assemblies are required in the B3, B4, B5 and B6 positions. These modules must meet the requirements for factory test equipment.

(*) Definition of Hangar Queen

A Hangar Queen Unit shall be defined as a Computer or Dsky which is capable of passing the following JDC's:

1.	05394	Transient Voltage Test
2.	05343	Equipment Setup
3.	05344	Equipment Power Turn On
4.	05345	Computer Power Turn On
5.	05351	Marginal Voltage Test
6.	05376	Automatic Newspeak Test
7.	05379	Dsky Test (Indicators & Keyboard)
8.	05382	Standby - E Memory Test
9.	05384	Priority of Interrupts
10.	05385	Dsky Spacecraft Signals
11.	05388	CTS Control of Newspeak

The equipment shall be tested in accordance with the above requirements during preliminary testing of the unit (s) which will be sold.

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PROCUREMENT SPECIFICATION
PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS
APOLLO GUIDANCE COMPUTER SUBSYSTEM
DRAWING NO. 2003991

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Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA
3-2-67	A	33144	1, 89	DMS	DMS
4-13-67	B	33607	1,2,51,52,[illegible],89	DMS FH	DMS FH
4-27-67	C	33673	1, 71	DMS FH	DMS FH

This specification consists of pages 1 to 115 inclusive.

APPROVALS				
		EC Hall 12/13	W Stameris 14 Dec 66	[illegible]	[illegible]
	NASA/MSC	MIT/IL		RAY	

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PROCUREMENT SPECIFICATION
PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS
APOLLO GUIDANCE COMPUTER SUBSYSTEM
DRAWING NO. 2003991

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA
3-2-67	A	33144	1, 89	DMS	DMS
4-13-67	B	33607	1,2,51,52,[illegible],89	DMS FA	DMS FA
4-27-67	C	33673	1, 71	DMS FA	DMS FA
6-8-67	D	33934	1, 80, 81, & 90-115	DMS FA	DMS FA

This specification consists of pages 1 to 115 inclusive.

APPROVALS	NASA/MSC	EC Hall 12/13	14 Dec 66 MIT/IL	RAY

3.1.6.1 (Continued)

Vibration in each of three mutually perpendicular axis shall be for 2 minutes as follows: 3DB/octave Rollup 10 HZ to $0.04g^2$/HZ at 70 HZ, $0.04g^2$/HZ to 420 HZ, 3DB/octave Rolloff from 420 HZ to 2000 HZ.

Tolerance limits between 10 HZ shall be ± 3DB;
*Tolerance limits between 50 HZ and 1000 HZ shall be ± 1.5DB;
Tolerance limits between 1000 HZ and 2000 HZ shall be ± 3DB

*In the event the ± 1.5DB from 50 to 1000 HZ cannot be met with existing facilities, the tolerance may be broadened to ± 3DB providing the overall g rms level is held to ± 10 percent.

3.1.7 Leak Rate. With the computer pressurized to 30.0 ± 1.0 psia with dry nitrogen at 25°C ± 2C°, the leak rate shall not exceed 1.0 psia for a period of 24.0 ± 0.5 hours. With the DSKY pressurized to 2 psig at 25°C ± 2°C using a mixture of 90% nitrogen and 10% helium the leak rate shall not exceed 1×10^{-3} cc/sec/atm.

3.1.8 Aging. The AGC Subsystem shall have accumulated not less than two hundred hours operating time prior to completion of test.

3.1.9 Miscellaneous Signals.

3.1.9.1 Signal W-910 (CNTRL 1) (2000-ohm short to ground) shall force the output of the +4 VDC power supply to 3.40 ± 0.01 VDC and 4.50 ± 0.01 VDC.

3.1.9.2 Signal W-911 (CNTRL 2) (2000-ohm short to ground) shall force the output of the +14 VDC power supply to 12.10 ± 0.01 VDC and 16.40 ± 0.01 VDC.

3.1.9.3 Signal D-912 (NHVFAL) shall inhibit RESTART due to voltage fail condition.

3.1.10 Spare and Not Connected Terminals. The following AGC connector A51 and DSKY connector J9 pins are provided as spare and NC terminals.

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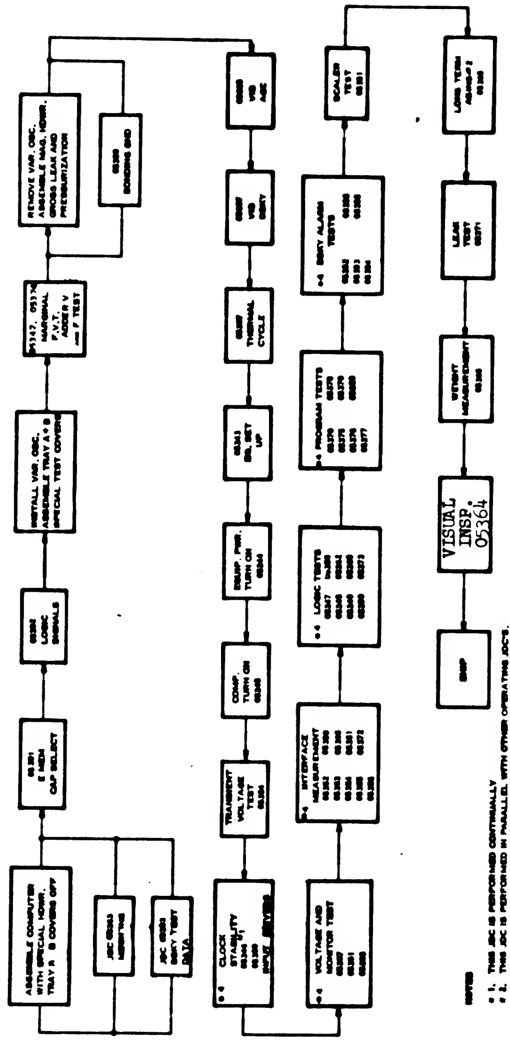
116	73	W-241	SPARE
-	13	W-246	SPARE
-	34 (N)	SD326	SPARE
-	37 (N)	SD328	SPARE
-	56 (M)	SD444	SPARE
-	34 (M)	SD445	SPARE
141	-	A-859	NC
140	-	A-860	NC
-	-	RD875	4/7/68
-	-	--908	-
413	-	CB028	NC


REMOVE VAR. OSC. ASSEMBLE MAG. HDWR. GROSS LEAK AND PRESSURIZATION
BONDING GND
05347, 05378 MARGINAL P.V.T. ADDER V — F TEST
INSTALL VAR. OSC. ASSEMBLE TRAY A + B SPECIAL TEST COVERS
LOGIC SIGNALS
E MEM CAP SELECT
ASSEMBLE COMPUTER WITH SPECIAL HDWR. TRAY A B COVERS OFF
DSKY TEST DATA
THERMAL CYCLE
EQUIP. PWR. TURN ON
COMP. TURN ON
TRANSIENT VOLTAGE TEST
*4 CLOCK STABILITY *1 INPUT DRIVERS
*4 VOLTAGE AND MONITOR TEST
*4 INTERFACE MEASUREMENT
*4 LOGIC TESTS
*4 PROGRAM TESTS
*4 DSKY ALARM TESTS
SCALER TEST
LONG TERM
LEAK TEST
WEIGHT MEASUREMENT
VISUAL INSP. 05364
SHIP

NOTES

- *1. THIS JDC IS PERFORMED CONTINUALLY
- *2. THIS JDC IS PERFORMED IN PARALLEL WITH OTHER OPERATING JDC'S.
- *3. IF MORE THAN ONE JDC IS LISTED IN A BOX THE PERFORMANCE SEQUENCE IS NOT CRITICAL, THEREFORE, THEY MAY BE PERFORMED IN ANY CONVENIENT ORDER.
- *4. THE PERFORMANCE SEQUENCE OF THESE JDC'S IS NOT CRITICAL, THEREFORE THEY MAY BE PERFORMED IN ANY CONVENIENT ORDER.

ASSEMBLY TEST PLAN

05342	Adder Voltage and Frequency Test
05343	Equipment Set-Up
05344	Equipment Power Turn-On
05345	Computer Power Turn-On
05346	AGC Clock Stability
05347	Central Registers Test
05348	Bank Registers Test
05349	Interrupt Registers Test
05350	Peripheral Channel-Instruction Test
05351	Marginal Voltage Test
05352	Radar Signal Measurements
05353	Downlink Signal Measurements
05354	Continuous Signal Characteristics
05355	Programmed Signal Characteristics Test
05356	C and RD Signals Test
05357	AGC Power Fail
05358	Scaler Double Frequency and Oscillator Alarm Test
05359	Hand Controller Test
05360	Input Counters Marginal Test
05361	Channel Inbits Marginal Test
05362	GoJam Initialization Test
05363	AGC Mechanical Inspection
05364	AGC Subsystem Visual Inspection
05365	Weight Measurement
05366	Long Term Aging
05367	Thermal Cycling Test
05368	Vibration Test-AGC (Random)
05369	PIPA Fail Test
05370	Voltage Variation Program Fail Test
05371	Leak Test
05372	Inlink Margin Test
05373	Increments Priority/Basic Instruction Test
05374	Marginal Frequency-Voltage and Thermal Test
05375	Worst Case Noise Erasable Memory Test
05376	Automatic Newspeak Test
05377	Timing Test
05378	Channel 30, 31, and 32 Test
05379	DSKY Test (Indicators and Keyboard)
05380	Alarms Test
05381	Scaler Test (24 hours)
05382	Standby - E Memory Test
05383	Warning Filter Alarm Test
05384	Priority of Interrupts
05385	DSKY Spacecraft Signals
05386	Monitor Signals Test
05387	Vibration Test-DSKY
05388	CTS Control of Newspeak
05389	AGC Input Drivers Signal Measurements
05390	Bonding Continuity Measurements
05391	Erasable Memory Capacitor Selection
05392	Logic Signal Measurements
05393	DSKY Test Data
05394	Transient Voltage Test

4.2.3 PROGRAM NEWSPEAK. The following information is supplied as a further explanation of the Program Newspeak JDC's 05375 thru 05386, and 05388.

4.2.3.1 Erasable Memory Checks (Ref. Paragraph 3.1.1.3).

4.2.3.1.1 Registers A, L, and Q are tested using both positive and negative numbers. Multiplication is used to check that the low order product in L is generated correctly. The Q register is checked by addition and subtraction as well as by checking for correct return addresses when the TC instructions are utilized.

4.2.3.1.2 Test ARUPT and BRUPT registers for proper loading.

4.2.3.1.3 Registers CYL and CYR are tested by loading with ± 0 and cycling 16 times to assure that no bits are either dropped or picked up. These registers are then loaded with negative full scale (40000) and cycled 17 times to assure proper cycling and end around carry.

The SR register is checked for propagation of the sign bit and for shifting of a one in the MSB to LSB. This register is also checked with ± 0.

The EDOP register is first checked with negative zero and then with a loop that loads a moving one starting with negative full scale down a plus one.

4.2.3.1.4 Test Erasable Banks 0, 1 and 2 by Register and Absolute Address.

This test checks that the same locations in erasable banks 0, 1 and 2 can be addressed by either specifying the actual address or by erasable bank register and an S-register value above 1400 octal.

4.2.3.1.5 Test Erasable Bank 0

To permit testing of bank 0 the contents must be placed in erasable bank 1. A checksum of bank 0 is taken before the contents are transferred to bank 1 and again when it is restored to its previous state.

The following tests performed on erasable banks 1 through 7 are done separately on erasable bank 0 after the contents of bank 0 are placed in bank 1. The starting address of bank 0 is 0060.

a. All locations are loaded with all ones and all zeroes and checked.

b. All locations are loaded with a moving one and moving zero pattern and checked.

c. Four checkerboards are loaded and checked -- 52525 and 25252 and opposite also 63146 and 14631 and opposite.

d. Each location is loaded with its own bank number and S-register address and checked.

4.2.3.2 Transfer Control Tests (Ref. Paragraph 3.1.1.5)

The TC instruction is checked for proper operation from fixed memory, from A and Q registers and also from erasable memory. This instruction is also checked for proper loading of Q register. The TCF instruction is checked for proper transfer in fixed memory and also for non-disturb of the Q register.

4.2.3.3 CA, TS and AD Test (Ref. Paragraph 3.1.1.5)

This test checks CA from both fixed and erasable memories for ± 0 and ± numbers. It also checks that CA does not disturb the E memory location used. This test also checks TS for ± 0 and ± numbers and checks that no skip occurs for non overflow in these cases. AD is checked for ± 0 and ± numbers from erasable memory.

4.2.3.4 CA and CCS Test (Ref. Paragraph 3.1.1.5)

This test checks the CCS instruction for proper transfer using ± 0 and ± numbers including +1. It also checks that the proper diminished absolute value is generated in these cases.

4.2.3.5 TS test with Overflow (Ref. Paragraph 3.1.1.5)

This test checks that OVSK (TS A) results in a TC +2 if the number in A contains overflow. It also checks that the accumulator contains the proper result after the OVSK. This test also checks AD from fixed memory for ± 0 and ± numbers.

4.2.3.6 Check of CCS for Decrementing (Ref. Paragraph 3.1.1.5)

This test uses the CCS instruction to decrement a number from negative full scale to positive zero simultaneously incrementing an erasable memory location. When the CCS results in +0 the erasable counter is checked for positive full scale.

4.2.3.7 Check AD using moving one loop (Ref. Paragraph 3.1.1.5)

The AD instruction is checked using a loop that generates a moving one from the LSB to the MSB.

4.2.3.8 Check AD using propagate one loop (Ref. Paragraph 3.1.1.5)

The AD instruction is checked using a loop that propagates a one from the LSB to the MSB.

4.2.3.9 LXCH Test (Ref. Paragraph 3.1.1.5)

LXCH is checked for positive and negative numbers both from erasable memory and from the Special and Central (S & C) registers.

4.2.3.10 XCH Test (Ref. Paragraph 3.1.1.5)

The XCH instruction is checked using positive and negative numbers in both erasable and special and central registers.

4.2.3.11 MASK Test (Ref. Paragraph 3.1.1.5)

The MASK instruction is checked for proper operation from fixed and erasable memories and from Special and Central registers. The MASK instruction is also checked for no edit from the editing registers.

4.2.3.12 CS Test (Ref. Paragraph 3.1.1.5)

The CS instruction is checked from fixed and erasable memory using ± 0 and ± full scale. This instruction is also checked using special and central registers.

4.2.3.13 INDEX Test (Ref. Paragraph 3.1.1.5)

This instruction is checked for erasable memory and for special and central registers. This instruction is checked further in the index generation of instructions.

4.2.3.14 INCR Test (Ref. Paragraph 3.1.1.5)

The INCR instruction is checked by a loop that increments a memory location from negative full scale to positive full scale and keeping the same count in A. When an overflow occurs in A the incremented location is checked for positive full scale. The instruction is also checked for producing overflow in A.

4.2.3.15 DXCH Test (Ref. Paragraph 3.1.1.5)

DXCH is checked using both positive and negative numbers in special and erasable locations. The following table reflects the signs of each of six combinations of numbers utilized in the test.

A	L	Erasable Hi	Erasable Low
pos	neg	neg	pos
pos	pos	+0	pos
pos	pos	pos	pos
neg	neg	neg	neg
neg	pos	neg	pos
neg	neg	pos	neg

4.2.3.16 DAS and AS Test (Ref. Paragraph 3.1.1.5)

The DAS test uses both positive and negative numbers in special and erasable locations to produce overflow and underflow in both high and low order sums.

The following table reflects the signs of the arguments, the high and low order sums and the overflow or underflow produced.

A	L	Erasable Hi	Erasable Low	Hi ans	Low ans
pos	neg	neg	pos	77777	77777
pos	pos	pos	pos	00000 - OFLO	00000 - OFLO
pos	pos	pos	pos	25252	25252
neg	neg	neg	neg	65252 - UFLO	65300 - UFLO
neg	pos	neg	pos	77776	37776 - OFLO
neg	neg	pos	neg	12345	54321

The Add to Storage test ranges from positive full scale to negative full scale to check for both overflow and underflow conditions. In addition the L-register is also checked for duplication of the A-register in the overflow condition.

4.2.3.17 BZF Test (Ref. Paragraph 3.1.1.5)

Check that a branch is made on ±0 numbers. Also check that no branch occurs on ± numbers with and without overflow. Check that no branch occurs on a moving bit going from the LSB to the MSB, including a check on the negative of each number.

4.2.3.18 BZMF Test (Ref. Paragraph 3.1.1.5)

Check that a branch is made on ±0 and -numbers with and without overflow. Check that no branch occurs on positive numbers with overflow.

4.2.3.19 DCA Tests (Ref. Paragraph 3.1.1.5)

Check that instruction will put correct values in to A and L when accessing fixed, erasable, and special and central memory, including a DCA L. Numbers used are combinations of ±,± including zero cases and overflow in A when doing a DCA L. When accessing erasable memory, a check is made to insure that the locations used did not change values.

4.2.3.20 DCS Test (Ref. Paragraph 3.1.1.5)

Check that instruction will put correct values in to A and L when accessing fixed, erasable, and special and central memory, including a DCS L. Numbers used are combinations of ± ± including zero cases and overflow in A when doing a DCS L. When accessing erasable memory, a check is made to insure that the locations used did not change values.

4.2.3.21 MSU Test (Ref. Paragraph 3.1.1.5)

Check all four combinations of modular subtraction using ± numbers on both special and central and erasable memory. Also check the case where the answer is an overflow uncorrected number.

4.2.3.17 BZF Test (Ref. paragraph 3.1.1.5) Check that a branch is made on ±0 numbers. Also check that no branch occurs on ± numbers with and without overflow. Check that no branch occurs on a moving bit going from the LSB to the MSB, including a check on the negative of each number.

4.2.3.18 BZMF Test (Ref. paragraph 3.1.1.5) Check that a branch is made on ±0 and -numbers with and without overflow. Check that no branch occurs on positive numbers with overflow.

4.2.3.19 DCA Tests (Ref. paragraph 3.1.1.5) Check that instruction will put correct values in to A and L when accessing fixed, erasable, and special and central memory, including a DCA L. Numbers used are combinations of +, ± including zero cases and overflow in Q when doing a DCA L. When accessing erasable memory, a check is made to insure that the locations used did not change values.

4.2.3.20 DCS Tests (Ref. paragraph 3.1.1.5) Check that instruction will put correct values in to A and L when accessing fixed, erasable, and special and central memory, including a DCS L. Numbers used are combinations of I, I including zero cases and overflow in Q when doing a DCS L. When accessing erasable memory, a check is made to insure that the locations used did not change values.

4.2.3.21 MSU Test (Ref. paragraph 3.1.1.5) Check all four combinations of modular subtraction using + numbers on both special and central and erasable memory. Also check the case where the answer is an overflow uncorrected number.

4.2.3.22 QXCH Test (Ref. paragraph 3.1.1.5) Check this instruction by using +) and ± numbers, with and without overflow when doing QXCH A and QXCH L.

4.2.3.23 SU Test (Ref. paragraph 3.1.1.5) A check is made for correct subtraction by propagating a one from the LSB to the MSB.

4.2.3.24 AUG Test (Ref. paragraph 3.1.1.5) Check that AUG works properly on ± and ±0 numbers in both erasable and special and central memory, including generation of overflow in the A-register.

4.2.3.25 DIM Test (Ref. paragraph 3.1.1.5) Check that DIM works properly on ± and ±0 numbers in both erasable and special and central memory.

4.2.3.26 INDEX Test (Ref. paragraph 3.1.1.5) Check that the extra code index does not reset the extra code switch, that more than one index may be performed before the extra code switch is reset, use ± and ±0 numbers, check that the instruction can use fixed, erasable, and special and central memory, and also check that erasable and special and central memory location used are not changed by the index instruction.

4.2.3.27 MP Test (Ref. paragraph 3.1.1.5) Multiply combinations of ± and +0 numbers from fixed, erasable, and special and central memory, checking that the final results are coreedt and the erasable memory multipliers are not lost during the multiply.

4.2.3.28 DIVIDE Test (Ref. paragraph 3.1.1.5) Divide combinations of ±, ± 0 and ±, ±0 double precision numbers by ± numbers checking for the correct results. Division is made from erasable and special and central checking that the divisor is not changed during the division.

4.2.3.29 READ Test (Ref. paragraph 3.1.1.5) Load L and Q with ± 0 and ± overflow numbers and check that proper results are read out while not destroying contents of L and Q.

4.2.3.30 WRITE Test (REf. paragraph 3.1.1.5) Write ± 0 and ± overflow numbers into L and Q. Check that write did not change A and that proper contents were stored in L and Q.

4.2.3.31 RAND Test (Ref. Paragraph 3.1.1.5) Load L and Q with alternating bit pattern and check RAND instruction when A has reverse alternating bit pattern and NZ. Also load L and Q with ± overflow numbers and check RAND instruction when A has NZ. L and Q are checked after each RAND to insure they have not been destroyed.

4.2.3.32 WAND Test (Ref. paragraph 3.1.1.5) WAND instruction checked by writing 52525, 25252, ± 0, ± overflow numbers into L and Q and checking for correct contents of A after the instruction.

4.2.3.33 ROR Test (Ref. paragraph 3.1.1.5) Check ROR instruction by loading L and Q with alternating bit patterns and ± overflow numbers and checking the contents of A, L and Q after the ROR instruction has been performed.

4.2.3.34 WOR Test (Ref. paragraph 3.1.1.5) Check WOR instruction by loading L and Q with ± 0 and write alternate bit patterns PFS and ± overflow numbers checking A, L and Q after each write.

4.2.3.35 RXOR Test (REf. paragraph 3.1.1.5) Check RXOR instruction by loading L and Q with NZ and ± overflow numbers and after each read checking contents of A, L and Q.

4.2.3.36 Checksum (Ref. paragraph 3.1.1.4) This routine takes a double precision checksum of any or all of the six modules as specified by the user and checks the sum against pre-stored values on the module level.

4.2.3.37 Check that Time 3 overflow causes an interrupt, by presetting only time 4 to overflow in a short period of time. (Ref. paragraph 3.1.1.9)

4.2.3.38 Check that Time 4 overflow causes an interrupt, by presetting only time 4 to overflow in a short period of time. (Ref. paragraph 3.1.1.9)

4.2.3.39 EDRUPTN (Ref. paragraph 3.1.1.5) Check that EDRUPT will transfer control to the A-register if no interrupt has been requested.

4.2.3.40 NORUPTN (Ref. paragraph 3.1.1.6) Check that no interrupts occurring will cause a gojam within a 140-300 ms period.

4.2.3.41 RUPTLOCN (Ref. paragraph 3.1.1.6) Check that inhibiting interrupts for too long will cause an interrupt during a 140-300 ms period.

4.2.3.42 RELINT3N (Ref. paragraph 3.1.1.6) Check that INHINT and RELINT work by causing an interrupt while inhinting and then relinting.

4.2.3.43 PRIORN (Ref. paragraph 3.1.1.9) Basic check of priority circuit by causing a Time 3 and Time 4 interrupt while inhibiting interrupts, and check the order of execution after a RELINT has been performed.

4.2.3. 44 XPARN (Ref. paragraph 3.1.1.6) Check that 13 words of bad parity will each case a gojam.

4.2.3.45 ALLPARN (Ref. paragraph 3.1.1.7) Write all bit combinations into one location and check that no bad parity occurs.

4.2.3.46 INRUPTN (Ref. paragraph 3.1.1.6) Do not resume from a Time 6 interrupt and check that a gojam occurs within a 140-300 ms period.

4.2.3.47 TCA Trap Test (Ref. paragraph 3.1.1.6) Check that executing a TC or TCF loop will cause a gojam within a 5-15 ms period.

4.2.3.48 NTWTCHMAN (Ref. paragraph 3.1.1.6) Check that not accessing location 0067 within a .64-1.92 sec. period will cause a gojam.

4.2.3.49 SELF Test (Ref. paragraph 3.1.1.5)

4.2.3.50 I/O STARTP (Ref. paragraph 3.1.1.8) This test is designed to check the decoding circuitry of downlink channels 34 and 35. Before describing the actual test performed to insure that this is doen properly, a brief discription of the circuitry involved will be given.

In essence the downlink circuitry consists of 2 channels, 34 and 35, which contain the information to be transmitted. A five-stage counter, whose outputs are decoded to gate out one bit of information at a time. A signal, DKBSNC, enables the output data to be transmitted and causes the 5-stage counter to be "incremented." Another signal, DKSTRT, resets the five-stage counter.

Bit 7 of channel 13 may best be described by saying that it functions as a "flag bit" for the downlink data and is gated out by signal DKBSNC when the five-stage counter is in the zero state, that is, reset.

4.2.3.50 cont.

The outputs from the five-stage counter are decoded and function as follows:

Stages 4 and 5 divide channel 34 and 35 into four 8 bit sections. Stages 1, 2, and 3 are decoded and enable a single bit from an 8 bit section to be transmitted.

For clarity it will be stated that bit 16 is the first bit transmitted from a channel while the parity bit is the last bit transmitted. Channel 34 is transmitted before channel 35.

Following is a list of interface connections used to generate the required downlink signals:

GYRRST causes DKSTRT which resets the 5-stage counter
GYRSET causes DKBSNC which steps the counter
DKDATA causes XLINK1 which allows the downlink output bits to be stored in counter 45.

GYRRST and GYRSET are controlled by bit 10 of channel 14 and the contents of out counter 47. The number of times signal GYRSET is generated is determined by the contents of counter 47. Signal GYRRST is generated whenever GYRSET is not. Both occur at a frequency of 3200 cps.

Following is a list of checks performed within this test to insure proper decoding:

C(34)	C(35)	#BITSYNC'S Generated	C(45)
00177	77777	9	00000

The above test proves that only one of the four 8 bit sections is active and that it is the proper one.

37600	77777	2	00000
17600	77777	3	00000
07600	77777	4	00000

These three tests plus the first test of the next group are sufficient to prove that multiple decoding is not present within the eight bit section.

40000	77777	5	00001
37600	77777	3	00001
17600	77777	4	00001
07600	77777	5	00001
03600	77777	6	00001
01600	77777	7	00001
00600	77777	8	00001
00200	77777	9	00001

The above eight tests prove that the lower 3 stages of the 5 stages are getting decoded properly and that each of eight states is capable of gating a data bit out of channel 34.

4.2.3.50 cont.

*10000	77777	17	00000
10100	*10177	25	00000
10100	*10000	33	00000

The above three tests prove that the remaining three states of stages 4 and 5 are getting decoded properly and activate the proper 8 bit section.

*40177	10000	17	00377 (eight puls
*40000	77600	25	00377
40000	*40177	33	00377

These three tests show that each of the bits within an 8 bit section is capable of being transmitted.

*The input to counter 45 is inhibited until the position being interrogated is beyond this point.

The last check performed in this section is set channel 34 and 35 to zero, set bit 7 of channel 13 to a one and generate two BITSYNC pulses. Counter 45 is checked for 1 pulse, if this test is successful bit 7 of channel 13 is functioning properly.

4.2.3.51 I/O STPIP (Ref. paragraph 3.1.1.8) The purpose of this test is to check the GYRO signals controlled by channel 14, bits 7 through 10, and the associated circuitry of PIPA counters 37, 40 and 41.

The following interface connections are made in order to accomplish this test:

Load CH. 14				Generate Signal	Causes Counter Request
10	9	8	7		
1	0	0	0	None	None
1	0	0	1	GYXP	PINC 37
1	0	1	0	GYXP	PINC 40
1	0	1	1	GYZP	PINC 41
1	1	0	0	None	None
1	1	0	1	GYXM	MINC 37
1	1	1	0	GYXM	MINC 40
1	1	1	1	GYZM	MINC 41

Ordinarily this signal pairing would not function properly, since the BYRO signals occur at a 102.4 KC rate and are gated by computer timing signal SB1. The PIPA counter increments are generated during SBZ time. It was therefore necessary to invert the counter increment requests being generated by the GYRO signals. This was accomplished by wiring the high side of GYRO output transformer to the low side of the PIPA input transformer. Computer signal PIPSAM then converted the 102.4 KC GYRO signals to 3200 KC counter increment requests for the three PIPA counters.

Associated with the PIPA counter increment requests is a circuit which rejects the first three consecutive pulses of one type, i.e., the first three PINC requests or three MINC requests.

4.2.3.51 cont.

In order to check that all of the above circuitry is functioning properly the following tests are made for each code which is entered into channel 14.

Enter a code into channel 14 which will pre-condition the PIPA circuits so that the first three counter increment requests generated by the test code will be rejected. Enter the code to be tested into channel 14. When bit 10 of channel 14 gets reset, go check the counter which was to be incremented for the proper number of pulses. Then check that the other two counters contain positive zero, that is, they did not receive any pulses.

The number of pulses gated out for each test is octal 103. The counter being tested is checked for octal 100.

In the case of the two illegal codes, all three counters are checked for positive zero.

The term pre-condition implies that when the code to be tested will cause PINCS on a counter, the code which MINCS the same counter is used to set the PIPA rejection circuit to a known state. Therefore the first three positive increment requests will be rejected. The reverse is also true when the MINC codes for each counter are tested.

4.2.3.52 I/O Test 1V (Ref. paragraph 3.1.1.8) This test checks that out counters 50 through 54 are diminished by instruction DINC when the proper bit is written into channel 14. This is accomplished by wiring the resultant interface signals which are generated during instruction DINC into circuits which request counter increments.

Load Ch. 14 Bit	DINC OUTCTR	If Contents of OUTCTR is	Generate Interface Signal	This is Wired Into	Causes Counter Request
16/15	50	Positive	CDUXDP	CDUXP	PCDU 32
	50	Negative	CDUXDM	CDUXM	MCDU 32
14	51	Positive	CDUYDP	CDUYP	PCDU 33
	51	Negative	CDUYDM	CDUYM	MCDU 33
13	52	Positive	CDUZDP	CDUZP	PCDU 34
	52	Negative	CDUZDM	CDUZM	MCDU 34
12	53	Positive	TRNDP	TRNP	PCDU 35
	53	Negative	TRNDM	TRNM	MCDU 35
11	54	Positive	SHFTDP	SHAFTP	PCDU 36
	54	Negative	SHFTDM	SHAFTM	MCDU 36

PCDU causes a counter to be incremented in two's complement arithmetic.

The CDU-DP or M signals are generated until the contents of the out counter are diminished to minus zero. At this time the channel bit which was requesting the DINC instruction is reset and checked.

In this routine each counter pair, 32+x, 50+x (x = 0 to X = 4) is tested separately. Four tests are performed on each pair. Initially 32+x is set to -30. The following numbers are placed in 50+x.

4.2.3.52 cont.

Trial 1. $+30_{10}$
" 2. $+30_{10}$
" 3. -30_{10} (1's complement)
" 4. -30_{10} (1's complement)

The corresponding 32+x values should become -
results of trial 1. +0
" " " 2. $+30_{10}$
" " " 3. +0
" " " 4. -30 (2's complement)

When performing a trial, after one of the above numbers is placed on 50+x and its corresponding drive bit set, the program waits until the drive bit resets and then checks 32+x for the expected result. Inorder to avoid an endless loop in the case of the drive bit not resetting, a time limiting loop has been incorporated. If the drive bit does not reset within the given time (aproximately 10 msec.) the test fails.

4.2.3.53 I/O Test 2V (Ref. paragraph 3.1.1.8) This test checks that the radar control codes which are associated with bits 1 through 4 of channel 13 are functioning properly. This is accomplished by using the decoded radar signals to generate increment requests for BMAG counters 42, 43, and 44. Bit 8 of channel 13 also gets tested since the counter requests which are generated at the interface module must pass through circuitry which is enables by this bit.

Below is a sequence of events which occur when a code is entered into the lower 4 bits of channel 13.

Ch. 13 Code				Radar Biganl Generated	Counter Request Generated	Type of Increment Requested	On CTR #
4	3	2	1				
1	0	0	0	None	None	None	None
1	0	0	1	RR RANG	BMGXP	PINC	42
1	0	1	0	RR RARA	BMGXM	MINC	42
1	0	1	1	None	None	None	None
1	1	0	0	LRSVEL	BMGYP	PINC	43
1	1	0	1	LRYVEL	BMGYM	MINC	43
1	1	1	0	LRZVEL	BMGZP	PINC	44
1	1	1	1	LR RANG	BMGZM	MINC	44

The radar signals are generated at a 3200 cycle/second rate for a period of 90 ms. This results in the generation of 256 pulses each time a code is entered into channel 13.

4.2.3.53 cont.

Initially, in this test, counters 42-44 are set to +0 and three tests are performed with each radar code and bit 8 of channel 13 set.

In the case of codes 11, 14, and 16 the proper counter is initialized at -400_8. The first request should PINC the counter to -0. The second request of the same code should MINC it to -377_8. It is then set to 40400_8. After the next request of the same code it should read 40000_8.

A test is performed with each radar code and bit 8 of channel 13 reset to ascertain that the counter accessed will not change in value.

The program periodically checks that no counter has changed form +0 other than the one to which a request is sent.

Each counter request should produce a RADARUPT. The program checks to see that this has occurred.

When bit 4 in channel 13 is reset, the program knows that the proper counter should contain the expected value and that the RADARUPT should have occurred. A timing loop has been incorporated to prevent an endless loop from occurring in the event bit 4 of channel 13 was not reset.

The no signal codes (10 and 13) are used to check that no signals are generated to any counter.

4.2.3.54 I/O Test 3V (Ref. paragraph 3.1.1.8) This test checks that bit 1 of channel 14 controls the OUTLINK circuitry and that this circuitry is functioning in the prescribed manner. Bit 1 of channel 14 causes the computer to generate a FLAG bit for the OUTLINK data and then shifts the 15 bits of OUTLINK data out of counter 57. Each of these 16 bits generate either a OTLNK1 or OTLNKO signal in the interface module depending on whether or not the data bit was a "1" or a "0" respectively. These signals are then used to generate SHINC and SHANC instructions for the UPLINK counter.

OTLNK1 causes UPLINK1 which requests a SHANC on counter 45.
OTLNKO causes UPLINKO which reqhests SHINC on counter 45.

This causes the data of counter 57 to be duplicated in counter 45.

Bits 5 and 6 of channel 13 are also incorporated in this test since they control the inhibit or enable status of the UPLINK counter.

4.2.3.54 cont.

Four checks are performed here. They are -

I.
1. Set Channel 13 bits 5 and 6 to 00.
2. Set counter 57 to 25252_8 counter 45 = 0, and Channel 14 bit 1 = 1.
3. Wait a maximum of 10 ms for Channel 14 bit 1 to reset. If it has not reset within this time, test fails.
4. Delay 5 more ms.
5. Check that an UPRUPT occurred. If not, Fail. UPRUPT should have been caused when the flag bit was detected in bit 16 of CTR 45.
6. Check that counter 45 now contains 25252_8. If not, Fail.

II.
1. Set Channel 13 bits 6 and 5 to 10 (INHIBIT UPLINK).
2. Set counter 57 to 25252, counter 45 = 0 and channel 14 bit 1 = 1.
3. Wait a maximum of 10 ms for channel 41 bit 1 to reset. If it has not reset within this time, test fails.
4. Delay 5 more ms.
5. Check that no UPRUPT occurred. If it did, Fail.
6. Check that counter 45 still contains 0. If not, Fail.

III. Same as I above except set CTR 57 to 52525 in step 2 and expect 52525 in CTR 45 in step 6.

IV. Same as II above except set CTR 57 to 52525 in step 2.

4.2.3.55 I/O Test 4V (ref. paragraph 3.1.1.8) This test checks that bits 2 and 3 of channel 14 control the altitude meter circuitry and that this circuitry is functioning in the prescribed manner. Bit 3 of channel 14 causes the computer to generate a flag bit for the altitude meter data and then shift the 15 data bits out of counter 60. Bit 2 selects one of the two paths by which the data may be transmitted.

Bit 2	Data Bit	Transmit Via
0	0	ALTO
	1	ALT1
1	0	ALRTO
	1	ALRT1

The wiring at the interface is such that -

ALTO causes RRINO,
ALT1 causes RRIN1,

ALRTO causes LRINO,
ALRT1 causes LRIN1,

These RR and LR signals will be converted to counter requests for

4.2.3.55 cont.

SHINC and SHANC on counter 46 when a radar code is loaded into channel 13.

The following is a list of the tests which are done to insure proper operation of the combined circuitry.

Load Ch. 14 Bits	Load Ch. 13 Bits	Data Expected in Computer
3 2	4 3 2 1	
1 0	1 0 0 0	None
	1 0 0 1	Duplicate of counter 60
	1 0 1 0	Duplicate of counter 60
1 1	1 0 0 0	None
	1 1 0 0	Duplicate of counter 60
	1 1 0 1	Duplicate of counter 60
	1 1 1 0	Duplicate of counter 60
	1 1 1 1	Duplicate of counter 60

There are two checks made for each code listed for channel 13. In the first check counter 60 is loaded with an odd bit configuration, in the second check counter 60 is loaded with an even bit configuration. The two results are then added and the answer checked for minus zero. Where no data is expected the answer is checked for positive zero.

There is one other test performed, and that is one the generation of the flag bit from the altitude meter circuitry. Unlike counter 45 there are no interrupts generated when the flag bit is sensed in position 16 of the counter and therefore this bit is not self checking.

This check consists of loading counter 60 with a plus one and waiting until this bit has been shifted one place to the left. At this time, counter 46 is checked to see that it contains the same information.

Radar code 1011 is not implemented and should not be tested.

4.2.3.56 I/O Test 5V (Ref. paragraph 3.1.1.8) This test checks that out counters 55 and 56 are diminished by instruction DINC when the proper bit is written into channel 14. This accomplished by wiring the resultant interface signals which are generated during instruction DINC into circuits which request counter increments.

4.2.3.56 cont.

Load Ch. 14 Bit	DINC OUTCTR	If Contents of OUTCTR is	Generate Interface Signal	This is Wired Into	Causes CTR Request
4	55	Positive	+THRST	BMGXP	PINC 42
	55	Negative	-THRST	BMGXM	MINC 42
5	56	Positive	+EMS	BMGYP	PINC 43
	56	Negative	-EMS	BMGYM	MINC 43

Bit 8 of channel 13 is also used since it enables the counter requests to be gated into the counter cells.

Following is a list of tests actually performed.

I.
1. Write 1 into channel 13 bit 8.
2. 0 CTR 42 (BMAGX), 0 CTR 43 (BMAGY).
3. 377_8 CTR 55.
4. Set channel 14 bits 5, 4 = 01.
5. Wait until channel 14 bit resets (100 ms is allowed).
6. Does CTR 42 = 377_8? If not, error.

II. Same as I except 77400_8 CTR 55 (step 2) and 77400_8

III.
1. Write 1 into channel 13 bit 8.
2. 0 CTR 42 0 CTR 43.
3. 377_8 CTR 56.
4. Set channel 14 bits 5, 4 - 10.
5. Wait until channel 14 bit resets (100 ms is allowed).
6. Does CTR 43 - 377_8? If not, error.

IV. Same as III except 77400 CTR 56 (step 2) and 77400_8 expected on CTR 43 (step 6).

4.2.3.57 I/O Test 6V (Ref. paragraph 3.1.1.8) This test is performed in order to check the decoding circuitry controlled by bits 5 and 6 of channel 13. These two bits are decoded such that information may be gated into the UPLINK counter, via of counter priority cells, from two different sources. That is, interface signal UPLINK or XLINK. It also checks that the circuit used for detecting excessive rates of information flow from these two sources is operative, and does control the INLINK TOO FAST bit of channel 33 when an excessive rate is detected. This is accomplished by using bit 6 of channel 14 to generate signal GYENAB and making the interface connection such that GYENAB causes XLINKO. The frequency of GYENAB is approximately 102 KC.

The following is a list of the eight tests which are performed -

4.2.3.57 cont.

Set Ch. 13		Set Ch. 14	In Ch. 33 Bit 11 Look for a
Bits 6	5	Bit 6	
0	0	1	1
1	0	1	1
1	1	1	1
0	1	1	0

The four are then repeated with bit 6 of channel 14 set to zero. For these four tests bit 11 of channel 33 should remain a one. The bits of channel 33 are inverted. Therefore bit 11 will be a one until the INLINK TOO FAST signal is present.

In checks one and two, bit 5 inhibits information from entering the counter priority cells via XLINK, therefore the excessive rate of XLINKO is not detected. In check three, bit 6 inhibits reception of INLINK data from either source, again the excessive rate should not be detected.

In check number four the combination of bits 5 and 6 allows information to be gated into the INLINK cirucitry via XLINK and at this time the excessive rate of XLINKO is detected and signal INLINK TOO FAST is generated, channel 33 bit 11 set to zero.

4.2.3.58 Special Rope Test (Ref. Paragraph 3.1.1.4). Individual, time dependent checksums will be performed on each of the abbreviated rope modules. The checksum used will accomplish more than an ordinary checksum. The program will be written to detect interchanged strand wiring and interchanged inhibit wiring. The program will also check proper resetting of the cores.

4.2.3.59 Register 20-23 & NDX Generation (Ref. Paragraph 3.1.1.5). Check the proper operation of all instructions on registers 20-23. Check worst case add by adding all possible numbers to NZ. Check that INCR and AUG instructions will cause interrupts when overflow results are obtained in Time 5, and executing the RUPT by using the EDRUPT instruction. Check the proper operation of INCR on Time 1 and Time 2. Generate all instructions by using INDEX instructions. Check that gojam will reset channels 5, 6, 10, 11, 12, 13, 14, 34, and 35.

4.2.3.60 DSKY Display (Ref. Paragraph 3.1.1.14). Turn OFF all lights on the DSKY's. Turn ON all alarms, 9's +sign, and V/N flash, turn ON all 8's and -sign. Turn ON all 7's-0's consecutively without sign. Blank the DSKY.

TIMECHKS consist of 16 tests described below --

(Tests #'s 1, 2, & 3 Ref. Paragraph 3.1.1.10)
(Test #4, Ref. Paragraph 3.1.1.11)
(Tests #5 thru #16, Ref. Paragraph 3.1.1.10)

All time counters and channels 3 and 4 are checked from proper frequency of incrementing. T1 through T6 are checked for proper phasing to each other. The external clock indicates amount of time actually taken. DSKY displays the amount that should have been taken.

Test #1 - Allow channel 4 to count from 0 to 0. Should take 5120 ms.

Test #2 - Allows channel 4 to pulse 32 times. Should take 10 ms.

Test #3 - Waits for channel 3 to pulse once. Should take 5120 ms.

4.2.3.60 (Cont'd)

Test #4 - Loads and checksums erasable memory, stores CH3 and 4 time and goes into Standby. Upon returning from Standby it computes the number of increments which Ch3 and 4 should have received and displays them -- the operator can then compute whether the external clock reading is accurate. It also does a checksum on E memory to see that it remained undisturbed by the Standby mode.

Test #5 thru Test #9 - Allows each time counter (Time 1-5) to count from 1 to 0. Each should take 163,830 ms.

Test #10 - Allows time 6 to count from 37777_8 to -0. Should take 10.23938 secs.

Test #11 - Allows time 6 to count from 40000_8 to -0. Should take 10.23938.

Test #12 - Checks amount of time that elapses between incrementing of time 3 and 4. Should be 7.5 ms.

Test #13 - Checks amount of time that elapses between incrementing of time 3 and time 5. Should be 5.0 ms.

Test #14 - Checks amount of time that elapses between incrementing of time 4 and time 1. Should be 2.5 ms.

Test #15 - Checks phasing from time 4 to time 2. Should be 2.5 ms because time 1 is set to PFS at each time 2 change.

Test #16 - Checks phasing from time 3 to time 6. Should be .3125 ms.

4.2.3.61 Worst Case Noise Erasable Memory Test (Ref. Paragraph 3.1.1.3) Banks 0 to 7 of erasable memory are loaded with the bit patterns as indicated in Table 1. Each work of bank 0 through 7 is checked in the following manner:

1. The word is read out and compared against the word that was stored.
2. One bit of the word (starting with bit 15) is complemented and together with the rest of the original word is restored into its previous location.

4.2.3.61 (Cont'd)

3. This word is then read out and checked for the proper bit configuration.

4. The original word is now restored to its proper location.

It should be noted that each bit as described in step 2 is done for all banks before the next bit in the word is complemented. This sequence of operations is repeated for all 15 bits of a word and when complete, each word that was stored originally, as indicated by Table 1, is now complemented and the process is repeated.

Upon successful completion the whole test is recycled. If an error is detected, the program will stop on a TC Trap.

Table 1

E Bank	Starting Address	Word Pattern
0	1424	0,0,1,1,0,0,1,1, etc,
1	1400	1,1,0,0,1,1,0,0, etc,
2	1400	1,1,0,0,1,1,0,0, etc,
3	1400	0,0,1,1,0,0,1,1, etc,
4	1400	0,0,1,1,0,0,1,1, etc,
5	1400	1,1,0,0,1,1,0,0, etc,
6	1400	1,1,0,0,1,1,0,0, etc,
7	1400	0,0,1,1,0,0,1,1, etc,

4.2.3.62 Warning Integrator Check Test (Ref. Paragraph 3.1.1.12). The purpose of this test is to check the warning alarm. Upon entering the test, the state of the warning alarm is examined. If on, the computer activity light is set; otherwise, it is reset. There is then a fifteen second delay during which the warning light should go OFF if it wasn't. If this does not happen, the STOP Fail routine is entered and the test terminated.

If the above check was successful, eight further checks are performed. Any of these checks which fail will not terminate the test -- just give a fifteen second indication of the failure on the DSKY and then continue to the next check.

4.2.3.62 (Cont'd)

The eight checks employ the same philosophy. Each is concerned with pulsing the test alarm bit every "Y" seconds over a period of "Z" seconds. The state of the warning bit is examined at the end of the "Z" seconds and, if it is not what is expected, there is a 15 second fail display. Otherwise, there is a 15 second success display.

Each time the test alarm bit is pulsed (i.e., every "Y" seconds during a check), the state of the warning bit is checked. When on, the computer activity light is set. When off, it is reset.

For the first four of the eight checks, the warning alarm bit is reset before the above described pulsing of the alarm bit is initiated. On the last four, the warning alarm bit is set.

During the performance of a particular check, the DSKY will display the following:

R1 = 8-"test #(1-8)"

R2 = "Y" - how often the test alarm bit is being pulsed (shown in seconds and hundredths of seconds)

R3 = "Z" - length of time over which the alarm bit is pulsed (in seconds).

At the end of the check, R2 and R3 are blanked and, if success, 8-"test #" remains in R1. Otherwise R1 becomes 9 -"test #".

The particulars for each check are as follows:

Check No.	R1 Display	R2 (Y) (1 pulse every Y.YY secs. for ZZ seconds)	R3 (Z)	Initial Warning State	End Expected Warning State
1	8-1	3.00	60	OFF	OFF
2	8-2	2.00	60	OFF	OFF or ON accepted.
3	8-3	1.00	12	OFF	ON
4	8-4	0.16	1	OFF	ON
5	8-5	0.50	60	ON	ON
6	8-6	1.00	60	ON	ON
7	8-7	2.00	60	ON	OFF or ON accepted.
8	8-8	3.00	60	ON	OFF

4.2.3.63 **Supervisor.** Displays failures for 15 seconds, forever, or returns to the next test. Displays number of successes and failures on DSKY at the end of a complete loop of tests. Failures display test number, address of failure, bank values, and number of failures to that point.

4.2.3.64 **DSKY Checks** (Ref. Paragraph 3.1.1.15). Check input of each key for proper codes. A continuous failure of the same type will terminate the test. Entries of keys within a .50 ms period will cause an alarm indication at all times.

4.2.3.65 **Priority of Interrupts** (Ref. Paragraph 3.1.1.12). Generate all interrupts and check that each occurs with correct priority.

4.2.3.66 **DSKY Vibration.** The computer is locked up and the DSKY cleared. If a keyrupt occurs while the DSKY is being vibrated, this entry is displayed in the R1 component of both DSKY's. The display represents the total number os such entries since the beginning of the test.

4.2.3.67 **BEGINP Test** (Ref. Paragraph 3.1.1.8). Briefly, channels 30, 31 and 32 received information, DC signals, which are controlled by switches on the CTS. Some of these signals, CH31, bits 1-12 and CH32, bits 1-10, may cause rupt 10 when enabled by the proper bit of channel 13. The breakdown is as follows:

CH13 Bit	Enables	If Ch32 contains any of the following bits	If CH33 contains any of the following bits
12	rupt 10	1 through 6	-
13	rupt 10	7 through 12	-
14	rupt 10	-	1 through 10

4.2.3.67 (Cont'd)

This test then checks that CH30, 31 and 32 received DC signals in the proper bit positions via the interface module. Also it checks to see that the interrupt is controlled by the proper bit position of channel 13 and occurs when requested.

Following is a description of the way in which this is handled.

Initially check to see that CH30, 31 and 32 have no bits present. Turn OFF COMP. ACT. This signals the operator that it is OK to stard checking the switches, beginning at CH30, switch position one.

When the program finds that the switch has been turned ON, it checks to see that it is the proper switch, if it is, it then checks the other two channels to insure that they do not have bits present. It both of these checks pass, the COMP ACT, is turned ON in the DSKY and the A register shows a five second flashing display of the bit just tested. After 5 seconds the COMP ACT. is turned OFF, this signals the operator to turn OFF the switch just tested and turn ON the next switch to the left. When a test is completed on an entire channel the next switch to be tested is switch number one of the next channel.

The following is a list of DSKY indications used in this test, and their interpretation.

NO ATT	Operator failed to turn ON next test vit within one minute of completion of testing of last bit.
KEY RELEASE	Two adjacent switches are ON for 30 seconds. This situation arises when the operator turns ON the switch to be tested before he turns OFF the switch which was just checked.
GIMBAL LOCK AND HOLD	RUPT10 was caused by wrong bit.
HOLD	Detection of an improper bit in CH30, 31 or 32. Display on DSKY as follows: Noun - Channel where error was detected Reg1 = Octal display of CH30 Reg2 - Octal display of CH31 Reg3 - Octal display of CH32
HOLD with Flashing Verb, Noun	Interrupt did not occur when requested. Display contents of CH30, 31 and 32 as previously described.

4.2.3.67 (Cont'd)

OPERATOR ERROR	Oper ator failed to select and option for returning from one of the three hold conditions.
FREE	The selected option has been processed.

The options for returning to the test are requested by switches 1 and 2 or 14 and 15 of channel 30.

Switch	Function
1 or 14	Test same bit over
2 or 15	Start test at next bit position
1 and 2 or 14 and 15	Start test at position one of next channel.
None of the above	Operator error.

The procedure, for using the options when a hold condition exists is as follows:

Turn ON T12
Turn OFF all channel switches
Select an option
Push fresh start
Turn OFF T12
Press Proceed - Free light comes on

Turn ON T12
Turn OFF option switches
Push fresh start
Turn OFF T12
Press Proceed - DSKY clears and switch selected for testing may be turned on.

Procedure for returning from no ATT and KEY RELEASE conditions.

Turn ON T12
Correct condition which caused ALARM
Push fresh start
Turn OFF T12
Push Proceed - Routine starts test where it left off - if the same condition exists at this time, the operator will get a hold condition which is an error.

5. PREPARATION FOR DELIVERY

5.1 GENERAL. Preparation for delivery shall be in accordance with Specification ND 1002214. The Computer Assy and DSKY's shall be pressurized for shipment at 2.0 ± 0.5 psig with dry nitrogen at ambient room temperature.

6. NOTES. None.

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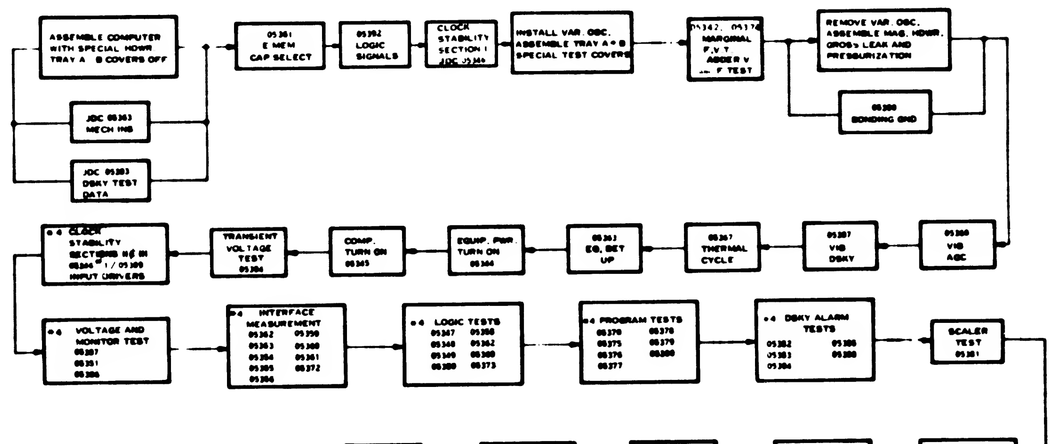
				MIT	NASA
3-2-67	A	33144	1, 89	DMS	DMS
4-13-67	B	33607	1, 2, 51, 52, 88, 89	DMS FA	DMS FA
4-27-67	C	33673	1, 71	DMS FA	DMS FA
6-8-67	D	33934	1, 80, 81, & 90-115	DMS FA	DMS FA
8-24-67	E	34451	1, 4, 90	[illegible] FA	[illegible] FA

This specification consists of pages 1 to 115 inclusive.

APPROVALS	NASA/MSC	EC Hall 1/4/3 W Stameris 14 Dec 66 MIT/IL	RAY


ASSEMBLE COMPUTER WITH SPECIAL HDWR. TRAY A B COVERS OFF
JDC 05363 MECH INS
JDC 05383 DSKY TEST DATA
05361 E MEM CAP SELECT
05392 LOGIC SIGNALS
CLOCK STABILITY SECTION I JDC 05366
INSTALL VAR. OSC. ASSEMBLE TRAY A + B SPECIAL TEST COVERS
05342, 05376 MARGINAL F.V.T. ADDER V F TEST
REMOVE VAR. OSC. ASSEMBLE MAG. HDWR. GROSS LEAK AND PRESSURIZATION
05380 BONDING GND
05388 VIB AGC
05387 VIB DSKY
05367 THERMAL CYCLE
05363 EQ. SET UP
EQUIP. PWR. TURN ON 05344
COMP. TURN ON 05345
TRANSIENT VOLTAGE TEST 05384
*4 CLOCK STABILITY SECTIONS II & III 05366 *1 / 05389 INPUT DRIVERS
*4 VOLTAGE AND MONITOR TEST 05387 05351 05386
*4 INTERFACE MEASUREMENT 05362 05363 05354 05385 05386 05350 05360 05361 05372
*4 LOGIC TESTS 05347 05348 05349 05380 05358 05362 05360 05373
*4 PROGRAM TESTS 05370 05375 05376 05377 05378 05379 05380
*4 DSKY ALARM TESTS 05382 05383 05384 05386 05380
SCALER TEST 05381
LONG TERM AGING #2 05386
LEAK TEST 05371
WEIGHT MEASUREMENT 05386
VIS. INSP. 05384
SHIP

NOTES

- *1. THIS JDC IS PERF[illegible]MED CONTINUALLY
- *2. THIS JDC IS PERFORMED IN PARALLEL WITH OTHER OPERATING JDC'S.
- 3. IF MORE THAN ONE JDC IS LISTED IN A BOX THE PERFORMANCE SEQUENCE IS NOT CRITICAL, THEREFORE, THEY MAY BE PERFORMED IN ANY CONVENIENT ORDER.
- *4. THE PERFORMANCE SEQUENCE OF THESE JDC'S IS NOT CRITICAL, THEREFORE THEY MAY BE PERFORMED IN ANY CONVENIENT ORDER.

ASSEMBLY TEST PLAN

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4-27-67	C	33673	1, 71	DMS FA	DMS FA
6-8-67	D	33934	1, 80, 81, & 90-115	DMS FG	DMS FG
8-24-67	E	34451	1, 4, 90	GB FA	GB FA
9-12-67	F	34587	1, 81	GB FA	GB FA

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3.1.6.1 (Continued)

Vibration in each of three mutually perpendicular axis shall be for 2 minutes as follows: 3DB/octave Rollup 10 HZ to $0.04g^2$/HZ at 70 HZ, $0.04g^2$/HZ to 420 HZ, 3DB/octave Rolloff from 420 HZ to 2000 HZ.

Tolerance limits between 10 HZ shall be ± 3DB;
*Tolerance limits between 50 HZ and 1000 HZ shall be ± 1.5DB;
Tolerance limits between 1000 HZ and 2000 HZ shall be ± 3DB

*In the event the ± 1.5DB from 50 to 1000 HZ cannot be met with existing facilities, the tolerance may be broadened to ± 3DB providing the overall g rms level is held to ± 10 percent.

3.1.7 **Leak Rate.** With the computer pressurized to 30.0 ± 1.0 psia with dry nitrogen at 25°C ± 2C°, the leak rate shall not exceed 1.0 psia for a period of 24.0 ± 0.5 hours. With the DSKY pressurized to 2 psig at 25°C ± 2°C using a mixture of 90% nitrogen and 10% helium the leak rate shall not exceed 1×10^{-3} cc/sec/atm.

3.1.8 **Aging.** The AGC shall have accumulated not less than two hundred hours operating time prior to completion of test.

3.1.9 **Miscellaneous Signals.**

3.1.9.1 Signal W-910 (CNTRL 1) (2000-ohm short to ground) shall force the output of the +4 VDC power supply to 3.40 ± 0.01 VDC and 4.50 ± 0.01 VDC.

3.1.9.2 Signal W-911 (CNTRL 2) (2000-ohm short to ground) shall force the output of the +14 VDC power supply to 12.10 ± 0.01 VDC and 16.40 ± 0.01 VDC.

3.1.9.3 Signal D-912 (NHVFAL) shall inhibit RESTART due to voltage fail condition.

3.1.10 **Spare and Not Connected Terminals.** The following AGC connector A51 and DSKY connector J9 pins are provided as spare and NC terminals.

Connector A51 Pin Numbers	Connector J9 Pin Numbers	Signal	Designation
115	75	W-210	SPARE
-	74	W-213	SPARE
116	73	W-241	SPARE
-	13	W-246	SPARE
-	34 (N)	SD326	SPARE
-	37 (N)	SD328	SPARE
-	56 (M)	SD444	SPARE
-	34 (M)	SD445	SPARE
141	-	A-859	NC
140	-	A-860	NC
-	-	RD875	4/7/68
-	-	--908	-
413	-	CB028	NC

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3-2-67	A	33144	1, 89		
4-13-67	B	33607	1, 2, 81, 82, 85, 89	FM	FM
4-27-67	C	33673	1, 71	FM	FM
6-8-67	D	33934	1, 80, 81, & 90-115		
8-24-67	E	34451	1, 4, 90	FM	FM
9-12-67	F	34587	1, 81	FM	FM
10-6-67	G	34813	1, 90	FB	FB

This specification consists of pages 1 to 115 inclusive.

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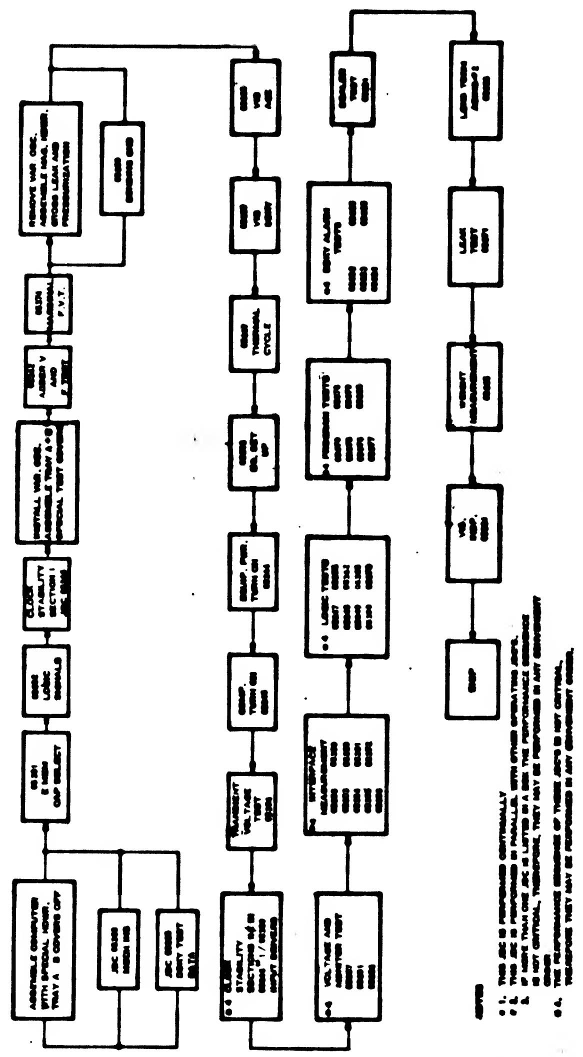
ASSEMBLE COMPUTER WITH SPECIAL HDWR. TRAY A B COVERS OFF
LOGIC SIGNALS
CLOCK STABILITY SECTION I
INSTALL VAR. OSC. ASSEMBLE TRAY A & B SPECIAL TEST COVERS
P.V.T.
REMOVE VAR OSC. ASSEMBLE MAG. HDWR. GROSS LEAK AND PRESSURIZATION
CLOCK STABILITY
VOLTAGE TEST
THERMAL CYCLE
VOLTAGE AND MONITOR TEST
INTERFACE MEASUREMENT
LOGIC TESTS
PROGRAM TESTS
DUTY ALARM TESTS
SHIP
WEIGHT MEASUREMENT
LEAK TEST

NOTES
*1. THIS JDC IS PERFORMED CONTINUALLY
*2. THIS JDC IS PERFORMED IN PARALLEL WITH OTHER OPERATING JDC'S.
*3. IF MORE THAN ONE JDC IS LISTED IN A BOX THE PERFORMANCE SEQUENCE IS NOT CRITICAL, THEREFORE, THEY MAY BE PERFORMED IN ANY CONVENIENT ORDER.
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3-2-67	A	33144	1, 89	DMS	DMS
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4-27-67	C	33673	1, 71	DMS FH	DMS FH
6-8-67	D	33934	1, 80, 81, & 90-115	DMS FS	DMS FS
8-24-67	E	34451	1, 4, 90	SB FH	JK FH
9-12-67	F	34587	1, 81	SB FH	SB FH
10-6-67	G	34813	1, 90	JK FB	JK FB
11-16-67	H	35078	1, 2	FB	FH

This specification consists of pages 1 to 115 inclusive.

APPROVALS	A Cohen NASA/MSC	EC Hall 12/13 W Stameris 14 Dec 66 MIT/IL	[illegible] RAY

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4-27-67	C	33673	1, 71		
6-8-67	D	33934	1, 80, 81, & 90-115		
8-24-67	E	34451	1, 4, 90		
9-12-67	F	34587	1, 81		
10-6-67	G	34813	1, 90		
11-16-67	H	35078	1, 2		
11-17-67	J	35079	1, 81, 88		

This specification consists of pages 1 to 115 inclusive.

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9-12-67	F	34587	1, 81	GB FH	GB FH
10-6-67	G	34813	1, 90	JK FH	JK FH
11-16-67	H	35078	1, 2	FH	FH
11-17-67	J	35079	1, 81, 88	FH	FH
12-21-67	K	35329	1,81 thru 116	GB FH	GB FH

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APPROVALS	NASA/MSC	EC Hall 12/13	W Stameris 14 Dec 66 MIT/IL	[illegible]	[illegible] RAY

3.1.6.1 (Continued)

Vibration in each of three mutually perpendicular axis shall be for 2 minutes as follows: (See Figure 3-4). 3DB/octave Rollup 10 HZ to $0.04g^2$/HZ at 70 HZ, $0.04g^2$/HZ to 420 HZ, 3DB/octave Rolloff from 420 HZ to 2000 HZ.

Tolerance limits between 10 HZ shall be ± 3DB;
*Tolerance limits between 50 HZ and 1000 HZ shall be ± 1.5DB;
Tolerance limits between 1000 HZ and 2000 HZ shall be ± 3DB

*In the event the ± 1.5DB from 50 to 1000 HZ cannot be met with existing facilities, the tolerance may be broadened to ± 3DB providing the overall g rms level is held to ± 10 percent.

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3.1.8 Aging. The AGC shall have accumulated not less than one hundred hours operating time during acceptance test.

3.1.9 Miscellaneous Signals.

3.1.9.1 Signal W-910 (CNTRL 1) (2000-Ohm short to ground) shall force the output of the +4 VDC power supply to 3.40 ± 0.01 VDC and 4.50 ± 0.01 VDC.

3.1.9.2 Signal W-911 (CNTRL 2) (2000-ohm short to ground) shall force the output of the +14 VDC power supply to 12.10 ± 0.01 VDC and 16.40 ± 0.01 VDC.

3.1.9.3 Signal D-912 (NHVFAL) shall inhibit RESTART due to voltage fail condition.

3.1.10 Spare and Not Connected Terminals. The following AGC connector A51 and DSKY connector J9 pins are provided as spare and NC terminals.

Connector A51 Pin Numbers	Connector J9 Pin Numbers	Signal	Designation
115	75	W-210	SPARE
-	74	W-213	SPARE
116	73	W-241	SPARE
-	13	W-246	SPARE
-	34 (N)	SD326	SPARE
-	37 (N)	SD328	SPARE
-	56 (M)	SD444	SPARE
-	34 (M)	SD445	SPARE
141	-	A-859	NC
140	-	A-860	NC
-	-	RD875	4/7/68
-	-	--908	-
413	-	CB028	NC

4.1

TABLE 4-1 (Cont'd)

Requirement	JDC
3.1.1.22.8	05384
3.1.1.22.9	05384
3.1.1.22.10	05384
3.1.1.23	05376 05380
3.1.1.23.1	05380
3.1.1.23.2	05380
3.1.1.23.3	05380
3.1.1.23.4	05380
3.1.1.23.5	05380
3.1.1.23.6	05369
3.1.1.23.7	05362 05357
3.1.1.23.8	05358
3.1.1.23.9	05358
3.1.1.23.9.1	05358
3.1.1.23.9.2	05358
3.1.1.24	05376 05362
3.1.1.24.1	05362 05383
3.1.1.24.2	05383
3.1.1.25	05378
3.1.1.26	05386
3.1.2.1	05344 05345
3.1.2.1.1	05345
3.1.2.1.2	05344
3.1.2.2	05379
3.1.2.3	N/A
3.1.2.4	N/A
3.1.2.5	N/A
3.1.2.6	N/A
3.1.2.7	N/A
3.1.2.8	N/A
3.1.2.9	N/A
3.1.2.10	N/A
3.1.3	05374
3.1.4	05391
3.1.4.1	05391
3.1.4.2	05391
3.1.4.3	05391
3.1.4.4	05391
3.1.5	05367
3.1.6	05368
3.1.7	05371
3.1.8	05366
3.1.9	05366
3.1.10	N/A
3.1.11	05390
3.1.12	05394
3.2.1	05363
3.2.2	05365

4.2.2 (Continued)

a. The Acceptance Tests must be performed with one (1) Computer and two (2) Dsky's. If any of the units are missing, Hangar Queen units shall be used during the tests. (*)
The Hangar Queen units shall not be subjected to mechanical inspection, vibration, thermal cycling, weight measurement, leak test or to the requirements of long term aging or Test Data JDC. A failure isolated to a Hangar Queen shall not be cause for rejection of the unit undergoing acceptance tests.

b. To perform the tests specified herein, Fixed Memory Modules containing Newspeak Program are required in the B1 and B2 positions and Warning Test Rope Assemblies are required in the B3, B4, B5 and B6 positions. These modules must meet the requirements for factory test equipment.

(*) Definition of Hangar Queen

A Hangar Queen Unit shall be defined as a Computer or Dsky which is capable of passing the following JDC's:

1.	05394	Transient Voltage Test
2.	05343	Equipment Setup
3.	05344	Equipment Power Turn On
4.	05345	Computer Power Turn On
5.	05351	Marginal Voltage Test
6.	05376	Automatic Newspeak Test
7.	05379	Dsky Test (Indicators & Keyboard)
8.	05382	Standby - E Memory Test
9.	05384	Priority of Interrupts
10.	05385	Dsky Spacecraft Signals
11.	05388	CTS Control of Newspeak

The equipment shall be tested in accordance with the above requirements during preliminary testing of the unit (s) which will be sold.

4.2.3 PROGRAM NEWSPEAK. The following information is supplied as a further explanation of the Program Newspeak JDC's 05375 thru 05386, and 05388.

4.2.3.1 Erasable Memory Checks (Ref. Paragraph 3.1.1.3).

4.2.3.1.1 Registers A, L, and Q are tested using both positive and negative numbers. Multiplication is used to check that the low order product in L is generated correctly. The Q register is checked by addition and subtraction as well as by checking for correct return addresses when the TC instructions are utilized.

4.2.3.1.2 Test ARUPT and BRUPT registers for proper loading.

4.2.3.1.3 Registers CYL and CYR are tested by loading with ± 0 and cycling 16 times to assure that no bits are either dropped or picked up. These registers are then loaded with negative full scale (40000) and cycled 17 times to assure proper cycling and end around carry.

The SR register is checked for propagation of the sign bit and for shifting of a one in the MSB to LSB. This register is also checked with ± 0.

The EDOP register is first checked with negative zero and then with a loop that loads a moving one starting with negative full scale down a plus one.

4.2.3.1.4 Test Erasable Banks 0, 1 and 2 by Register and Absolute Address.

This test checks that the same locations in erasable banks 0, 1 and 2 can be addressed by either specifying the actual address or by erasable bank register and an S-register value above 1400 octal.

4.2.3.1.5 Test Erasable Bank 0

To permit testing of bank 0 the contents must be placed in erasable bank 1. A checksum of bank 0 is taken before the contents are transferred to bank 1 and again when it is restored to its previous state.

The following tests performed on erasable banks 1 through 7 are done separately on erasable bank 0 after the contents of bank 0 are placed in bank 1. The starting address of bank 0 is 0060.

a. All locations are loaded with all ones and all zeroes and checked.

b. All locations are loaded with a moving one and moving zero pattern and checked.

c. Four checkerboards are loaded and checked -- 52525 and 25252 and opposite also 53146 and 14631 and opposite.

d. Each location is loaded with its own bank number and S-register address and checked.

1.0 SCOPE

This specification establishes the detail requirements for complete identification and acceptance of all units of the Apollo Guidance Computer, Part Number 2003993-011, hereinafter called AGC and the Display and Keyboard Assy, Part Number 2003994-011, hereinafter called DSKY.

2.0 APPLICABLE DOCUMENTS

2.1 EFFECTIVE ISSUES. The following documents form a part of this specification to the extent specified herein. Unless otherwise specified, Military Standards and Specifications shall be the issue in effect on the date of request for proposal or invitation to bid.

SPECIFICATIONS

APOLLO G&N

ND 1002214	General Specification for Preservation, Packaging, Packing and Container Marking of APOLLO Guidance and Navigation Major Assemblies, Assemblies, Subassemblies, Parts and Associated Ground Support Equipment.

DRAWINGS

APOLLO G&N

2003991	APOLLO Guidance Computer Subsystem

(Copies of specifications, standards, drawings, bulletins, and publications required by suppliers in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer).

2.2 CONFLICTING REQUIREMENTS. In event of a conflict between requirements, the following order of precedence shall apply. The contractor shall also notify MIT/IL APOLLO Management of the conflict.

a. The contract
b. This specification
c. Documents listed in this section

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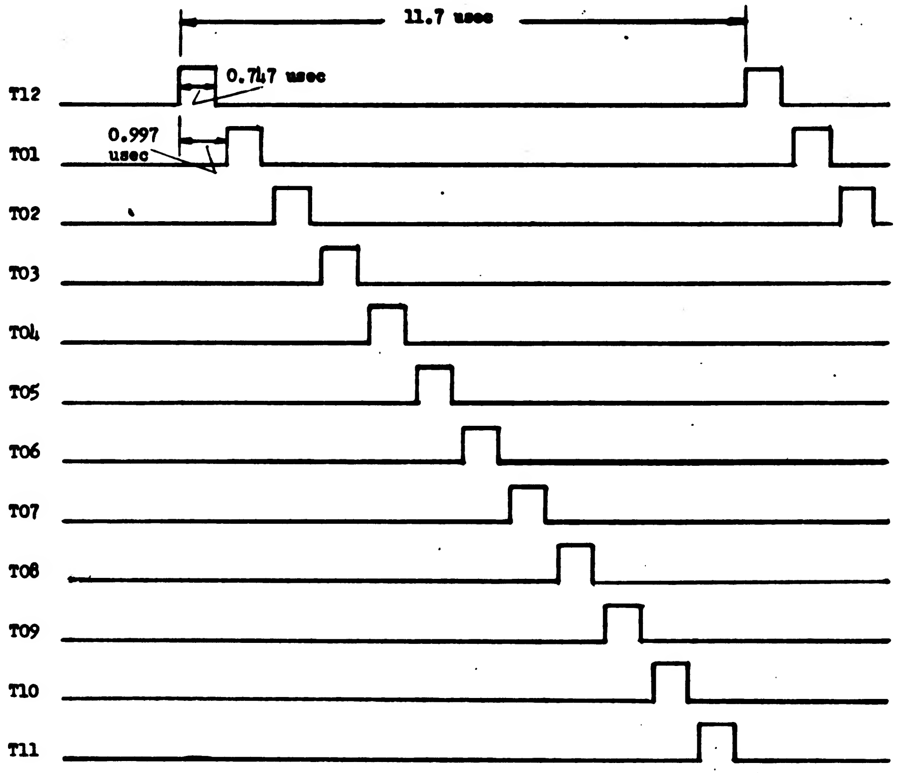


FIGURE 3-1 Memory Cycle Time

3.1.1.9 CP Register. The Write, Read and Clear Timing of the CP registers shall be as designated in Table 3-2. Write Control pulses for each register shall be gated by a WT pulse. The Write control pulses shall also be gated by a CT pulse to produce a clear pulse. Read Control pulses shall be gated by an RT pulse.

3.1.1.9.1 Register A. This register shall consist of 16-bit positions corresponding to the sixteen write lines. Information shall be written into or read out of register A in accordance with the control pulses listed in Table 3-2 as follows:

3.1.1.9.1.1 WA. Control pulse WA shall clear the A register and enter information from write lines 1 through 16 into the corresponding A register bit positions.

3.1.1.9.1.2 WSC. Control pulse WSC shall clear the A register and enter information from write lines 1 through 16 into the corresponding A register bit positions provided that the octal address specified in Table 3-2 is entered into the S register.

3.1.1.9.1.3 WALS. Control pulse WALS shall clear the A register; and enter information from write lines 3 through 16 into A register bit positions 1 through 14 respectively; shall enter information into A register bit positions 15 and 16 from G register bit 16 provided bit 1 of G register contains a ZERO; and shall enter information into A register bit positions 15 and 16 from write line 16 provided that bit 1 of G register contains a ONE.

3.1.1.9.1.4 RA. Control pulse RA shall read the contents of register A bit positions 1 through 16 into the corresponding write lines.

3.1.1.9.1.5 RSC. Control pulse RSC shall read the contents of register A bit positions 1 through 16 into the corresponding write lines provided the octal address specified in Table 3-2 is entered into the S register.

3.1.1.9.2 Register L. This register shall consist of 16-bit positions corresponding to the sixteen write lines. Information shall be written into or read out of register L in accordance with the control pulses listed in Table 3-2 as follows:

3.1.1.9.2.1 WL. Control pulse WL shall clear the L register and enter information from write lines 1 through 16 into the corresponding L register bit positions.

3.1.1.9.2.2 WSC. Control pulse WSC shall clear the L register and enter information from write lines 1 through 16 into the corresponding L register bit positions provided that the octal address specified in Table 3-2 is entered into the S register.

3.1.1.9.2.3 WALS. Control pulse WALS shall clear the L register and enter information from write lines 1 and 2 into L register bit positions 13 and 14 respectively.

3.1.1.9.2.4 RL. Control pulse RL shall read the contents of register L bit positions 1 through 14 into the corresponding write lines and bit position 16 into write lines 15 and 16.

3.1.2 DISPLAY and KEYBOARD (DSKY). The Display and Keyboard Assemblies shall have the capability to store, display, and transfer binary information as required by the computer. Each DSKY shall comply to PS 2003994 prior to shipment with the computer.

In addition, the following data for each DSKY shall be included in the Acceptance Data Package.

1. Module visual inspection data
2. Leak test data
3. Electrical test data
4. Intensity test data
5. Switch chatter data

3.1.2.1 Voltage Requirements. The DSKY assemblies shall perform as specified herein when supplied with the following input voltages.

3.1.2.1.1 DC Voltages. The following DC voltages shall be applied to the assemblies through the designated connector pins.

DSKY J9 Connector Pins

VOLTAGE	MAIN	NAV	SIGNAL - NAME
a. 14.0± 1.0 vdc	1	1	WD240 - BPLSSW
b. 27.0± 6.5 vdc	21	-	WD243 +28 COM
	-	21	WD355 +28 COM
c. 5.0± 0.1 vdc	-	64	W-347 5V Status Power
	-	65	W-348 5V Status Power Ret.
	-	62	W-349 5V Caut. Power
	-	63	W-350 5V Caut. Power Ret.
	62	-	WD446 5V Caut. Power
	63	-	WD447 5V Caut. Power Ret.
	64	-	WD448 5V Status Power
	65	-	WD449 5V Status Power Ret.
d. Ovdc (Ground)	8	8	WD239 OVDC

3.1.2.1.2 AC Voltages The AC voltage supplied to the assemblies shall be 75 VRMS at 400 + 8 cps, single phase variable up to 115 ± 5VRMS and capable of being turned off. This voltage is applied to the following DSKY connector pins as the designated signals.

NAV DSKY		MAIN DSKY	
Signal — Name	J9 Connector Pin	Signal — Name	J9 Conn. Pin
W-343 115V 400 cps	38	W-437 115V 400 cps	38
W-344 115V 400 cps RET	40	W-438 115V 400 cps RET	40

3.1.2.2 Input Sync Pulse. An 800 + 16 cps sync pulse shall be applied to the DSKY assemblies through the following connector pins.

Signal	Name	DSKY J9 Connector Pins	
		Main	NAV
CC212	ELSNCN	-	7
CC242	ELSNCM	7	-

3.1.2.3 Legend Brightness Control. The brightness of the legends (NOUN, VERB, PROGRAM, and the horizontal bars above each register) shall be variable from OFF to maximum brightness by input signals to the DSKY connectors as follows:

Signal	Name	DSKY J9 Connector Pins	
		Main	Nav
WD345	DIMMER	-	5
WD346	DIMMER RET.	-	4
RD442	DIMMER	5	-
WD443	DIMMER RET.	4	-

3.1.2.4 Keyboard. With all keys except "STBY" individually pressed, signals DE201 through DE205 from the NAV DSKY and signals DE253 through DE257 from the Main DSKY shall produce the codes specified in Table 3-11. With no keys except STBY depressed, signal D-206 from the NAV DSKY and signal D-209 from the Main DSKY shall be present. Keys RSET and STBY on each DSKY shall produce signals D-207 and D-208, respectively, when pressed.

3.1.2.5 Flashing Alarm Characters. With the flashing timing pulse, signals CB236 and CB244, applied to pins 46 and 72 of J9, respectively, the alarm indicators KEY REL and OPR ERR shall flash.

3.1.2.6 Flashing Noun Characters. With the Flasher Timing Pulse, signal CB238 applied to pin 70 of J9 and the Noun numerical characters programmed for 8's (ref. Tables 3-12 and 3-13,) the numerical characters shall flash.

3.1.2.7 Flashing Verb Characters. With the Flasher Timing Pulse, signal CB238, applied to pin 70 of J9 and the Verb numerical characters programmed for 8's (ref. Tables 3-12 and 3-13,) the numerical characters shall flash.

3.1.2.8 Numerical Electroluminescent Indicators. With the appropriate RLYWD and RLYBT combinations of logic "ones" and "zeros" applied as specified in Tables 3-12 and 3-13, the corresponding Noun, Verb, and Program legend numerical characters and the numerical characters of all registers shall be displayed.

3.1.2.9 **Isolated Relay Indicators.** When the codes specified in Table 3-14 are present, the corresponding isolated relay indicator shall be illuminated. Contact closure shall exist between pins of J9 as specified in Table 3-14.

3.1.2.10 **Status and Caution Indicators.** With the signal applied to an input pin of J9 as specified in Table 3-15 the corresponding status or caution indicator shall be illuminated. Contact closure shall exist between pins of J9 as specified in Table 3-15.

TABLE 3-11 KEY CODES

	OUTPUT PINS								
KEY	DE257	DE256	DE255	DE254	DE253	D-206	D-208	D-207	MAIN SIGNALS
	DE205	DE204	DE203	DE202	DE201	D-209	D-208	D-207	NAV SIGNALS
	79	76	77	78	51	49	48	28	
KEY REL	1	1	0	0	1	0	0	0	
VERB	1	0	0	0	1	0	0	0	
NOUN	1	1	1	1	1	0	0	0	
ENTR	1	1	1	0	0	0	0	0	
CLR	1	1	1	1	0	0	0	0	
+	1	1	0	1	0	0	0	0	
-	1	1	0	1	1	0	0	0	
0	1	0	0	0	0	0	0	0	
1	0	0	0	0	1	0	0	0	
2	0	0	0	1	0	0	0	0	
3	0	0	0	1	1	0	0	0	
4	0	0	1	0	0	0	0	0	
5	0	0	1	0	1	0	0	0	
6	0	0	1	1	0	0	0	0	
7	0	0	1	1	1	0	0	0	
8	0	1	0	0	0	0	0	0	
9	0	1	0	0	1	0	0	0	
RSET	1	0	0	1	0	0	1	0	
STBY	0	0	0	0	0	1	0	1	

3.1.5 Thermal Cycle Extremes. The subsystem shall be subjected to the thermal cycle specified below. The AGC shall be exercised using a rope program during the thermal cycle. The computer shall be pressurized at 2.0 ± 0.2 psig, and the DSKY pressurized at 2.0 ± 0.2 psig at $25^{\circ}C \pm 3^{\circ}C$.

a. Set ambient temperature to $0^{\circ}C \, {}^{+0C^{\circ}}_{-2.8C^{\circ}}$ for 8 ± 1 hours. (power OFF and computer installed on coldplate).

b. Increase the ambient temperature to $65^{\circ}C \, {}^{+2.8C^{\circ}}_{-0C^{\circ}}$ in not less than 40 minutes. This temperature shall be maintained for 3 hours.

c. Decrease the ambient temperature to $0^{\circ}C \, {}^{+0C^{\circ}}_{-2.8C^{\circ}}$ in not less than 40 minutes. This temperature shall be maintained for 1.5 hours.

d. Increase the ambient temperature to $65^{\circ}C \, {}^{+2.8C^{\circ}}_{-0C^{\circ}}$ in not less than 40 minutes. This temperature shall be maintained for 1.5 hours.

e. Decrease the ambient temperature to $0^{\circ}C \, {}^{+0C^{\circ}}_{-2.8C^{\circ}}$ in not less than 40 minutes. This temperature shall be maintained for 1.5 hours.

f. Increase the ambient temperature to $65^{\circ}C \, {}^{+2.8C^{\circ}}_{-0C^{\circ}}$ in not less than 40 minutes. This temperature shall be maintained for 1.5 hours.

g. Decrease the ambient temperature to room ambient (approx. $25^{\circ}C$) in not less than 20 minutes.

3.1.6 Vibration. The subsystem shall be exercised using a rope program while subjected to the random vibration limits specified below:

3.1.6.1 The Random vibration shall be Gaussian distributed with the exception that magnitude limiting shall occur at a peak to rms "g" ratio of 3 to 1.

Vibration in each of three mutually perpendicular axis shall be for 2 minutes as follows: 3DB/octave Rollup 10 HZ to $0.04g^2$/HZ at 70 HZ, $0.04g^2$/HZ to 420 HZ, 3DB/octave Rolloff from 420 HZ to 2000 HZ.

Tolerance limits between 10 HZ and 50 HZ shall be ± 3DB;
*Tolerance limits between 50 HZ and 1000 HZ shall be ± 1.5DB;
Tolerance limits between 1000 HZ and 2000 HZ shall be ± 3DB;

*In the event the ± 1.5 db from 50 to 1000 HZ cannot be met with existing facilities, the tolerance may be broadened to ± 3 db providing the overall g rms level is held to ± 10 percent.

3.1.7 **Leak Rate.** With the computer and each DSKY pressurised to 30.0 ± 1.0 psia with dry nitrogen at 25°C ± 2C°, the leak rate shall not exceed 1.0 psia for a period of 24.0 ± 0.5hours.

3.1.8 **Aging.** The AGC Subsystem shall have accumulated not less than two hundred hours operating time prior to completion of test.

3.1.9 **Miscellaneous Signals.**

3.1.8.1 Signal W-910 (CNTRL I)(2000-ohm short to ground) shall force the output of the +4 VDC power supply to 3.40 ± 0.01 vdc and 4.50 ± 0.01 vdc.

3.1.9.2 Signal W-911 (CNTRL 2) (2000-ohm short to ground) shall force the output of the +14 vdc power supply to 12.10 ± 0.01 vdc and 16.40 ± 0.01 vdc.

3.1.9.3 Signal D-912 (NHVFAL) shall inhibit RESTART due to voltage fail condition.

3.1.10 **Spare and Not Connected Terminals.** The following AGC connector A51 and DSKY connector J9 pins are provided as spare and NC terminals.

Connector A51 Pin Numbers	Connector J9 Pin Numbers	Signal	Designation
115	75	W-210	SPARE
-	74	W-213	SPARE
116	73	W-241	SPARE
-	13	W-246	SPARE
-	34(N)	SD326	SPARE
-	37(N)	SD328	SPARE
-	56(M)	SD444	SPARE
-	34(M)	SD445	SPARE
141	-	A-859	NC
140	-	A-860	NC
-	-	RD875	4/7/68/
-	-	--908	-
413	-	CB028	NC

3.1.11 Bonding Continuity. The resistance measured between the items listed in Table 3-16 shall not exceed the value specified in Table 3-16.

TABLE 3-16

From	To	Resistance
Tray B Cover (Magnesium Surface)	Tray A Cover (Magnesium Surface)	20 milliohms
Tray A (Brass to Magnesium Surface)	Mid Spacer (Magnesium Surface)	20 milliohms
Tray B Cover (Magnesium Surface)	Baby Tray (Screw to helicoil to Magnesium Surface)	30 milliohms

3.1.12 Transient Susceptibility. With the computer exercised by a rope program and with transient voltage spikes, as specified below, applied to the positive and negative 28 volt input power lines of the computer; there shall be no evidence of transient susceptibility.

Transient Voltage Spikes
(Output of Test Circuitry Prior to Application to 28 Volt lines)

Amplitude	50 ± 2 volts
Pulse Width	10.0 ± 4.0 usec at the 5 volt level
Pulse Rate	10 pps
Rise Time	1 usec max (10% to 90%)
Polarity	Positive

3.2 PRODUCT CONFIGURATION

3.2.1 Drawings. The configuration of the assembly shall be in accordance with Apollo G&N drawing 2003993-011 and all drawings and engineering data referenced thereon.

3.2.2 Weight. The weight of the computer and DSKY shall be measured and recorded.

4. QUALITY ASSURANCE PROVISIONS

4.1 GENERAL. The contractor responsible for the manufacture of the assembly shall be responsible for the accomplishment of each test required herein. See Table 4-1, Product Performance and Configuration Requirements/Quality Verification Cross Reference Index.

TABLE 4-1

Requirement	JDC	Requirement	JDC	Requirement	JDC
3.1	05364	3.1.1.9.1.1	05376	3.1.1.9.4.1	05376
3.1.1.1	05365 05345	3.1.1.9.1.2	05376	3.1.1.9.4.2	05376
3.1.1.1.1	05344	3.1.1.9.1.3	05376	3.1.1.9.5	05348 05376
3.1.1.1.2	05345	3.1.1.9.1.4	05376	3.1.1.9.5.1	05376
3.1.1.1.3	05345	3.1.1.9.1.5	05376	3.1.1.9.5.2	05376
3.1.1.1.4	05357	3.1.1.9.2	05347 05376	3.1.1.9.6	05347 05376
3.1.1.2	05351	3.1.1.9.2.1	05376	3.1.1.9.6.1	05376
3.1.1.3	N/A	3.1.1.9.2.2	05376	3.1.1.9.6.2	05376
3.1.1.4	05346	3.1.1.9.2.3	05376	3.1.1.9.6.3	05376
3.1.1.4.1	N/A	3.1.1.9.2.4	05376	3.1.1.9.6.4	05376
3.1.1.5	05346	3.1.1.9.2.5	05376	3.1.1.9.6.5	05376
3.1.1.6	05381	3.1.1.9.2.6	05376	3.1.1.9.6.6	05376
3.1.1.7	05382	3.1.1.9.3	05347 05376	3.1.1.9.7	05348 05376
3.1.1.7.1	05354	3.1.1.9.3.1	05376	3.1.1.9.7.1	05376
3.1.1.7.2	05356	3.1.1.9.3.2	05376	3.1.1.9.7.2	05376
3.1.1.8	05376	3.1.1.9.3.3	05376	3.1.1.9.7.3	05376
3.1.1.9	05376	3.1.1.9.3.4	05376	3.1.1.9.8	05376
3.1.1.9.1	05347 05376	3.1.1.9.4	05348 05376		

4.1

TABLE 4-1 (Cont'd)

Requirement	JDC	Requirement	JDC	Requirement	JDC
3.1.1.9.8.1	05376	3.1.1.9.13.2	05376	3.1.1.11	05349 05376
3.1.1.9.8.2	05376	3.1.1.9.13.3	05376	3.1.1.11.1	05376
3.1.1.9.8.3	05376	3.1.1.9.14	05376	3.1.1.12	05376
3.1.1.9.8.4	05376	3.1.1.9.14.1	05376	3.1.1.12.1	05376
3.1.1.9.9	05376	3.1.1.9.14.2	05376	3.1.1.13	05376
3.1.1.9.10	05376	3.1.1.9.14.3	05376	3.1.1.14	05362
3.1.1.9.10.1	05376	3.1.1.9.14.4	05376	3.1.1.14.1	05362
3.1.1.9.11	05376	3.1.1.9.15	05376	3.1.1.14.2	05362
3.1.1.9.11.1	05376	3.1.1.9.15.1	05376	3.1.1.14.3	05362
3.1.1.9.11.2	05376	3.1.1.9.15.2	05376	3.1.1.14.4	05376
3.1.1.9.11.3	05376	3.1.1.9.15.3	05376	3.1.1.14.5	05373
3.1.1.9.11.4	05376	3.1.1.9.15.4	05376	3.1.1.14.6	05384
3.1.1.9.11.5	05376	3.1.1.9.15.5	05376	3.1.1.15	05376
3.1.1.9.11.6	05376	3.1.1.9.15.6	05376	3.1.1.15.1	05376
3.1.1.9.11.7	05376	3.1.1.9.15.7	05376	3.1.1.15.2	05376
3.1.1.9.11.8	05376	3.1.1.9.16	05376	3.1.1.15.3	05376
3.1.1.9.11.9	05376	3.1.1.9.16.1	05376	3.1.1.15.4	05376
3.1.1.9.11.10	05376	3.1.1.9.16.2	05376	3.1.1.15.5	05376
3.1.1.9.12	05376	3.1.1.9.16.3	05376	3.1.1.15.6	05376
3.1.1.9.12.1	05376	3.1.1.9.16.4	05376	3.1.1.15.7	05350 05376
3.1.1.9.12.2	05376	3.1.1.9.16.5	05376	3.1.1.15.8	05376
3.1.1.9.13	05376	3.1.1.10	05349 05376	3.1.1.15.9	05376
3.1.1.9.13.1	05376	3.1.1.10.1	05375 05376	3.1.1.15.10	05376

TABLE 4-1 (Cont'd)

4.1

Requirement	JDC	Requirement	JDC	Requirement	JDC
3.1.1.15.11	05376	3.1.1.17	05356 05376	3.1.1.20.3.2	05376
3.1.1.15.12	05376	3.1.18	05361 05376 05378	3.1.1.20.3.3	05376
3.1.1.15.13	05376	3.1.1.19	05354	3.1.1.20.4	05376
3.1.1.15.14	05376	3.1.1.20	05377	3.1.1.20.4.1	05376
3.1.1.15.15	05361 05378	3.1.1.20.1	05377	3.1.1.20.4.1.2	05376
3.1.1.15.16	05378	3.1.1.20.1.1	05377	3.1.1.20.4.1.3	05376
3.1.1.15.17	05378	3.1.1.20.1.2	05377	3.1.1.20.4.1.4	05376
3.1.1.15.18	05378	3.1.1.20.1.3	05377	3.1.1.20.4.2	05376
3.1.1.15.19	05376 05353	3.1.1.20.1.4	05377	3.1.1.20.4.2.1	05359
3.1.1.16	N/A	3.1.1.20.1.5	05377	3.1.1.20.4.2.2	05359
3.1.1.16.1	N/A	3.1.1.20.1.6	05377	3.1.1.20.4.2.3	05359
3.1.1.16.2	N/A	3.1.1.20.1.7	05377	3.1.1.20.5	05359
3.1.1.16.3	N/A	3.1.1.20.1.8	05377	3.1.1.20.6	05372 05376
3.1.1.16.4	N/A	3.1.1.20.1.9	05377	3.1.1.20.6.1	05376
3.1.1.16.5	N/A	3.1.1.20.1.10	05377	3.1.1.20.6.1.1	05376
3.1.1.16.6	N/A	3.1.1.20.1.11	05377	3.1.1.20.6.1.2	05376
3.1.1.16.7	N/A	3.1.1.20.2	05360 05376	3.1.1.20.6.1.3	05376
3.1.1.16.8	N/A	3.1.1.20.2.1	05376	3.1.1.20.6.2	05376
3.1.1.16.9	N/A	3.1.1.20.2.2	05376	3.1.1.20.6.2.1	05376
3.1.1.16.10	N/A	3.1.1.20.2.3	05376	3.1.1.20.6.2.2	05376
3.1.1.16.11	N/A	3.1.1.20.2.4	05376	3.1.1.20.6.2.3	05376
3.1.1.16.14	N/A	3.1.1.20.2.5	05376	3.1.1.20.6.3	05376
3.1.1.16.15	N/A	3.1.1.20.3	05376	3.1.1.20.6.4	05376
3.1.1.16.16	N/A	3.1.1.20.3.1	05376	3.1.1.20.6.4.1	05376
				3.1.1.20.6.4.2	05376

4.1

TABLE 4-1 (Cont'd)

Requirement	JDC	Requirement	JDC	Requirement	JDC
3.1.1.20.6.4.3	05372 05376	3.1.1.20.8.1.3	05376	3.1.1.20.8.7.3	05376
3.1.1.20.6.5	05376	3.1.1.20.8.2	05376	3.1.1.20.8.8	05376
3.1.1.20.6.5.1	05376	3.1.1.20.8.2.1	05376	3.1.1.20.8.8.1	05376
3.1.1.20.6.5.2	05376	3.1.1.20.8.2.2	05376	3.1.1.20.8.8.2	05376
3.1.1.20.6.5.3	05376	3.1.1.20.8.2.3	05376	3.1.1.20.8.8.3	05376
3.1.1.20.6.6	05376	3.1.1.20.8.3	05376	3.1.1.20.8.9	05376
3.1.1.20.7	05352 05376	3.1.1.20.8.3.1	05376	3.1.1.20.8.9.1	05376
3.1.1.20.7.1	05376	3.1.1.20.8.3.2	05376	3.1.1.20.8.9.2	05376
3.1.1.20.7.1.1	05376	3.1.1.20.8.3.3	05376	3.1.1.20.8.10	05376
3.1.1.20.7.1.2	05376	3.1.1.20.8.4	05376	3.1.1.20.8.10.1	05376
3.1.1.20.7.2	05376	3.1.1.20.8.4.1	05376	3.1.1.20.8.10.2	05376
3.1.1.20.7.2.1	05376	3.1.1.20.8.4.2	05376	3.1.1.20.8.11	05376
3.1.1.20.7.2.2	05376	3.1.1.20.8.4.3	05376	3.1.1.20.8.11.1	05376
3.1.1.20.7.3	05376	3.1.1.20.8.5	05376	3.1.1.20.8.11.2	05376
3.1.1.20.7.3.1	05376	3.1.1.20.8.5.1	05376	3.1.1.20.9	05376
3.1.1.20.7.4	05376	3.1.1.20.8.5.2	05376	3.1.1.21	05353 05376
3.1.1.20.7.4.1	05376	3.1.1.20.8.5.3	05376	3.1.1.22	05378 05384
3.1.1.20.7.5	05376	3.1.1.20.8.6	05376	3.1.1.22.1	05384
3.1.1.20.7.5.1	05376	3.1.1.20.8.6.1	05376	3.1.1.22.2	05384
3.1.1.20.7.5.2	05376	3.1.1.20.8.6.2	05376	3.1.1.22.3	05384
3.1.1.20.8	05355 05376	3.1.1.20.8.6.3	05376	3.1.1.22.4	05384
3.1.1.20.8.1	05376	3.1.1.20.8.7	05376	3.1.1.22.5	05384
3.1.1.20.8.1.1	05376	3.1.1.20.8.7.1	05376	3.1.1.22.6	05384
3.1.1.20.8.1.2	05376	3.1.1.20.8.7.2	05376	3.1.1.22.7	05384

TABLE 4-1 (Cont'd)

4.1

Requirement	JDC	Requirement	JDC	Requirement	JDC
3.1.1.22.8	05384	3.1.1.24.1	05362 05383	3.1.3	05374
3.1.1.22.9	05384	3.1.1.24.2	05383	3.1.4	05391
3.1.1.22.10	05384	3.1.1.25	05378	3.1.4.1	05391
3.1.1.23	05376 05380	3.1.1.26	05386	3.1.4.2	05391
3.1.1.23.1	05380	3.1.2.1	05344 05345	3.1.4.3	05391
3.1.1.23.2	05380	3.1.2.1.1	05345	3.1.4.4	05391
3.1.1.23.3	05380	3.1.2.1.2	05344	3.1.5	05367
3.1.1.23.4	05380	3.1.2.2	05379	3.1.6	05368
3.1.1.23.5	05380	3.1.2.3	N/A	3.1.7	05371
3.1.1.23.6	05369	3.1.2.4	N/A	3.1.8	05366
3.1.1.23.7	05362 05357	3.1.2.5	N/A	3.1.9	05366
3.1.1.23.8	05358	3.1.2.6	N/A	3.1.10	N/A
3.1.1.23.9	05358	3.1.2.7	N/A	3.1.11	05390
3.1.1.23.9.1	05358	3.1.2.8	N/A	3.1.12	05394
3.1.1.23.9.2	05358	3.1.2.9	N/A	3.2.1	05363
3.1.1.24	05376 05362	3.1.2.10	N/A	3.2.2	05365

4.1.1 Test Conditions

4.1.1.1 Environmental. The assembly shall be tested under the following ambient conditions:

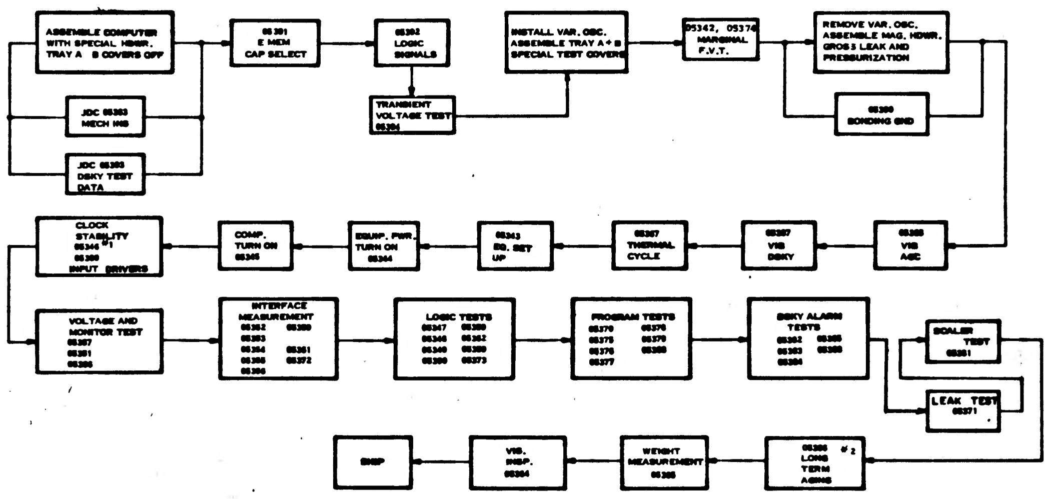
a.	Temperature:	25° ± 10°C
b.	Relative Humidity:	90% max
c.	Barometric Pressure:	28 to 32 inches of Hg

4.1.2 Nonconforming Units. Failure of the unit to pass any examination or test of this specification shall automatically classify the unit as nonconforming. Each nonconforming unit corrected by the contractor shall be reinspected. Reinspection may be limited to the test or examination which defined the nonconformance, or, when directed by the cognizant inspector, a complete retest and re-examination may be required. Nonconforming units which have not been corrected will be considered for acceptance only upon formal application by the contractor to the cognizant NASA representative. Any module replaced during testing shall have operated in the system under test for not less than fifty hours, shall be thermal cycled, and vibrated and the assembly shall be leak tested prior to final acceptance.

4.2 TESTS/VERIFICATIONS

4.2.1 Drawing Compliance. The assembly shall be visually examined for compliance to the requirements of APOLLO G&N Drawing 2003991. Particular attention shall be given to inspection for damage to surfaces, structure, and equipment, including contaminants, pin misalignment, and legibility and appearance of marking.

4.2.2 Acceptance Tests. All tests shall be performed using the JDC's listed herein in the order specified in the Assembly Test Plan as follows:


ASSEMBLE COMPUTER WITH SPECIAL HDWR. TRAY A B COVERS OFF
JDC 05393 MECH INS
JDC 05395 DSKY TEST DATA
05391 E MEM CAP SELECT
05392 LOGIC SIGNALS
TRANSIENT VOLTAGE TEST 05394
INSTALL VAR. OSC. ASSEMBLE TRAY A + B SPECIAL TEST COVERS
05342, 05374 MARGINAL F.V.T.
REMOVE VAR. OSC. ASSEMBLE MAG. HDWR. GROSS LEAK AND PRESSURIZATION
05390 BONDING GND
05388 VIB AGC
05387 VIB DSKY
05367 THERMAL CYCLE
05343 EQ. SET UP
EQUIP. PWR. TURN ON 05344
COMP. TURN ON 05345
CLOCK STABILITY 05346 #1 05380 INPUT DRIVERS
VOLTAGE AND MONITOR TEST 05357 05351 05386
INTERFACE MEASUREMENT 05352 05360 05353 05354 05361 05355 05372 05356
LOGIC TESTS 05347 05359 05348 05362 05349 05358 05350 05373
PROGRAM TESTS 05370 05376 05375 05379 05376 05380 05377
DSKY ALARM TESTS 05382 05385 05383 05389 05384
SCALER TEST 05381
LEAK TEST 05371
05386 #2 LONG TERM AGING
WEIGHT MEASUREMENT 05385
VIS. INSP. 05384
SHIP

NOTES

- # 1. THIS JDC IS PERFORMED CONTINUALLY
- # 2. THIS JDC IS PERFORMED IN PARALLEL WITH OTHER OPERATING JDC'S.
- 3. IF MORE THAN ONE JDC IS LISTED IN A BOX THE PERFORMANCE SEQUENCE IS NOT CRITICAL, THEREFORE, THEY MAY BE PERFORMED IN ANY CONVENIENT ORDER.

ASSEMBLY TEST PLAN

05342	Adder Voltage and Frequency Test
05343	Equipment Set-Up
05344	Equipment Power Turn-On
05345	Computer Power Turn-On
05346	AGC Clock Stability
05347	Central Registers Test
05348	Bank Registers Test
05349	Interrupt Registers Test
05350	Peripheral Channel-Instruction Test
05351	Marginal Voltage Test
05352	Radar Signal Measurements
05353	Downlink Signal Measurements
05354	Continuous Signal Characteristics
05355	Programmed Signal Characteristics Test
05356	C and RD Signals Test
05357	AGC Power Fail
05358	Scaler Double Frequency and Oscillator Alarm Test
05359	Hand Controller Test
05360	Input Counters Marginal Test
05361	Channel Inbits Marginal Test
05362	GoJam Initialization Test
05363	AGC Mechanical Inspection
05364	AGC Subsystem Visual Inspection
05365	Weight Measurement
05366	Long Term Aging
05367	Thermal Cycling Test
05368	Vibration Test-AGC (Random)
05369	PIPA Fail Test
05370	Voltage Variation Program Fail Test
05371	Leak Test
05372	Inlink Margin Test
05373	Increments Priority/Basic Instruction Test
05374	Marginal Frequency-Voltage and Thermal Test
05375	Worst Case Noise Erasable Memory Test
05376	Automatic Newspeak Test
05377	Timing Test
05378	Channel 30, 31, and 32 Test
05379	DSKY Test (Indicators and Keyboard)
05380	Alarms Test
05381	Scaler Test (24 hours)
05382	Standby - E Memory Test
05383	Warning Filter Alarm Test
05384	Priority of Interrupts
05385	DSKY Spacecraft Signals
05386	Monitor Signals Test
05387	Vibration Test-DSKY
05388	CTS Control of Newspeak
05389	AGC Input Drivers Signal Measurements
05390	Bonding Continuity Measurements
05391	Erasable Memory Capacitor Selection
05392	Logic Signal Measurements
05393	DSKY Test Data
05394	Transient Voltage Test

4.2.3 PROGRAM NEWSPEAK. The following information is supplied as a further explanation of the Program Newspeak JDC's 05375 thru 05386, and 05388.

4.2.3.1 Erasable Memory Checks (Ref. Paragraph 3.1.1.3).

4.2.3.1.1 Registers A, L, and Q are tested using both positive and negative numbers. Multiplication is used to check that the low order product in L is generated correctly. The Q register is checked by addition and subtraction as well as by checking for correct return addresses when the TC instructions are utilized.

4.2.3.1.2 Test ARUPT and BRUPT registers for proper loading.

4.2.3.1.3 Registers CYL and CYR are tested by loading with ± 0 and cycling 16 times to assure that no bits are either dropped or picked up. These registers are then loaded with negative full scale (40000) and cycled 17 times to assure proper cycling and end around carry.

The SR register is checked for propagation of the sign bit and for shifting of a one in the MSB to LSB. This register is also checked with ± 0.

The EDOP register is first checked with negative zero and then with a loop that loads a moving one starting with negative full scale down a plus one.

4.2.3.1.4 Test Erasable Banks 0, 1 and 2 by Register and Absolute Address.

This test checks that the same locations in erasable banks 0, 1 and 2 can be addressed by either specifying the actual address or by erasable bank register and an S-register value above 1400 octal.

4.2.3.1.5 Test Erasable Bank 0

To permit testing of bank 0 the contents must be placed in erasable bank 1. A checksum of bank 0 is taken before the contents are transferred to bank 1 and again when it is restored to its previous state.

The following tests performed on erasable banks 1 through 7 are done separately on erasable bank 0 after the contents of bank 0 are placed in bank 1. The starting address of bank 0 is 0060.

a. All locations are loaded with all ones and all zeroes and checked.

b. All locations are loaded with a moving one and moving zero pattern and checked.

c. Four checkerboards are loaded and checked -- 52525 and 25252 and opposite also 63146 and 14631 and opposite.

d. Each location is loaded with its own bank number and S-register address and checked.

4.2.3.2 Transfer Control Tests (Ref. Paragraph 3.1.1.5)

The TC instruction is checked for proper operation from fixed memory, from A and Q registers and also from erasable memory. This instruction is also checked for proper loading of Q register. The TCF instruction is checked for proper transfer in fixed memory and also for non-disturb of the Q register.

4.2.3.3 CA, TS and AD Test (Ref. Paragraph 3.1.1.5)

This test checks CA from both fixed and erasable memories for ± 0 and ± numbers. It also checks that CA does not disturb the E memory location used. This test also checks TS for ± 0 and ± numbers and checks that no skip occurs for non overflow in these cases. AD is checked for ± 0 and ± numbers from erasable memory.

4.2.3.4 CA and CCS Test (Ref. Paragraph 3.1.1.5)

This test checks the CCS instruction for proper transfer using ± 0 and ± numbers including +1. It also checks that the proper diminished absolute value is generated in these cases.

4.2.3.5 TS test with Overflow (Ref. Paragraph 3.1.1.5)

This test checks that OVSK (TS A) results in a TC +2 if the number in A contains overflow. It also checks that the accumulator contains the proper result after the OVSK. This test also checks AD from fixed memory for ± 0 and ± numbers.

4.2.3.6 Check of CCS for Decrementing (Ref. Paragraph 3.1.1.5)

This test uses the CCS instruction to decrement a number from negative full scale to positive zero simultaneously incrementing an erasable memory location. When the CCS results in +0 the erasable counter is checked for positive full scale.

4.2.3.7 Check AD using moving one loop (Ref. Paragraph 3.1.1.5)

The AD instruction is checked using a loop that generates a moving one from the LSB to the MSB.

4.2.3.8 Check AD using propagate one loop (Ref. Paragraph 3.1.1.5)

The AD instruction is checked using a loop that propagates a one from the LSB to the MSB.

4.2.3.9 LXCH Test (Ref. Paragraph 3.1.1.5)

LXCH is checked for positive and negative numbers both from erasable memory and from the Special and Central (S & C) registers.

4.2.3.10 XCH Test (Ref. Paragraph 3.1.1.5)

The XCH instruction is checked using positive and negative numbers in both erasable and special and central registers.

4.2.3.11 MASK Test (Ref. Paragraph 3.1.1.5)

The MASK instruction is checked for proper operation from fixed and erasable memories and from Special and Central registers. The MASK instruction is also checked for no edit from the editing registers.

4.2.3.12 CS Test (Ref. Paragraph 3.1.1.5)

The CS instruction is checked from fixed and erasable memory using ± 0 and ± full scale. This instruction is also checked using special and central registers.

4.2.3.13 INDEX Test (Ref. Paragraph 3.1.1.5)

This instruction is checked for erasable memory and for special and central registers. This instruction is checked further in the index generation of instructions.

4.2.3.14 INCR Test (Ref. Paragraph 3.1.1.5)

The INCR instruction is checked by a loop that increments a memory location from negative full scale to positive full scale and keeping the same count in A. When an overflow occurs in A the incremented location is checked for positive full scale. The instruction is also checked for producing overflow in A.

4.2.3.15 DXCH Test (Ref. Paragraph 3.1.1.5)

DXCH is checked using both positive and negative numbers in special and erasable locations. The following table reflects the signs of each of six combinations of numbers utilized in the test.

A	L	Erasable Hi	Erasable Low
pos	neg	neg	pos
pos	pos	+0	pos
pos	pos	pos	pos
neg	neg	neg	neg
neg	pos	neg	pos
neg	neg	pos	neg

4.2.3.16 DAS and AS Test (Ref. Paragraph 3.1.1.5)

The DAS test uses both positive and negative numbers in special and erasable locations to produce overflow and underflow in both high and low order sums.

The following table reflects the signs of the arguments, the high and low order sums and the overflow or underflow produced.

A	L	Erasable Hi	Erasable Low	Hi ans	Low ans
pos	neg	neg	pos	77777	77777
pos	pos	pos	pos	00000 - OFLO	00000 - OFLO
pos	pos	pos	pos	25252	25252
neg	neg	neg	neg	65252 - UFLO	65300 - UFLO
neg	pos	neg	pos	77776	37776 - OFLO
neg	neg	pos	neg	12345	54321

The Add to Storage test ranges from positive full scale to negative full scale to check for both overflow and underflow conditions. In addition the Q-register is also checked for duplication of the A-register in the overflow condition.

4.2.3.17 BZF Test (Ref. Paragraph 3.1.1.5)

Check that a branch is made on ±0 numbers. Also check that no branch occurs on ± numbers with and without overflow. Check that no branch occurs on a moving bit going from the LSB to the MSB, including a check on the negative of each number.

4.2.3.18 BZMF Test (Ref. Paragraph 3.1.1.5)

Check that a branch is made on ±0 and -numbers with and without overflow. Check that no branch occurs on positive numbers with overflow.

4.2.3.19 DCA Tests (Ref. Paragraph 3.1.1.5)

Check that instruction will put correct values in to A and L when accessing fixed, erasable, and special and central memory, including a DCA L. Numbers used are combinations of ±,± including zero cases and overflow in Q when doing a DCA L. When accessing erasable memory, a check is made to insure that the locations used did not change values.

4.2.3.20 DCS Test (Ref. Paragraph 3.1.1.5)

Check that instruction will put correct values in to A and L when accessing fixed, erasable, and special and central memory, including a DCS L. Numbers used are combinations of ± ± including zero cases and overflow in Q when doing a DCS L. When accessing erasable memory, a check is made to insure that the locations used did not change values.

4.2.3.21 MSU Test (Ref. Paragraph 3.1.1.5)

Check all four combinations of modular subtraction using ± numbers on both special and central and erasable memory. Also check the case where the answer is an overflow uncorrected number.

4.2.3.17 **BZF Test** (Ref. paragraph 3.1.1.5) Check that a branch is made on +0 numbers. Also check that no branch occurs on ± numbers with and without overflow. Check that no branch occurs on a moving bit going from the LSB to the MSB, including a check on the negative of each number.

4.2.3.18 **BZMF Test** (Ref. paragraph 3.1.1.5) Check that a branch is made on ±0 and -numbers with and without overflow. Check that no branch occurs on positive numbers with overflow.

4.2.3.19 **DCA Tests** (Ref. paragraph 3.1.1.5) Check that instruction will put correct values in to A and L when accessing fixed, erasable, and special and central memory, including a DCA L. Numbers used are combinations of +, ± including zero cases and overflow in Q when doing a DCA L. When accessing erasable memory, a check is made to insure that the locations used did not change values.

4.2.3.20 **DCS Tests** (Ref. paragraph 3.1.1.5) Check that instruction will put correct values in to A and L when accessing fixed, erasable, and special and central memory, including a DCS L. Numbers used are combinations of I, I including zero cases and overflow in Q when doing a DCS L. When accessing erasable memory, a check is made to insure that the locations used did not change values.

4.2.3.21 **MSU Test** (Ref. paragraph 3.1.1.5) Check all four combinations of modular subtraction using + numbers on both special and central and erasable memory. Also check the case where the answer is an overflow uncorrected number.

4.2.3.22 **QXCH Test** (Ref. paragraph 3.1.1.5) Check this instruction by using ±) and ± numbers, with and without overflow when doing QXCH A and QXCH L.

4.2.3.23 **SU Test** (Ref. paragraph 3.1.1.5) A check is made for correct subtraction by propagating a one from the LSB to the MSB.

4.2.3.24 **AUG Test** (Ref. paragraph 3.1.1.5) Check that AUG works properly on ± and ±0 numbers in both erasable and special and central memory, including generation of overflow in the A-register.

4.2.3.25 **DIM Test** (Ref. paragraph 3.1.1.5) Check that DIM works properly on ± and ±0 numbers in both erasable and special and central memory.

4.2.3.26 **INDEX Test** (Ref. paragraph 3.1.1.5) Check that the extra code index does not reset the extra code switch, that more than one index may be performed before the extra code switch is reset, use ± and ±0 numbers, check that the instruction can use fixed, erasable, and special and central memory, and also check that erasable and special and central memory location used are not changed by the index instruction.

4.2.3.27 MP Test (Ref. paragraph 3.1.1.5) Multiply combinations of ± and +0 numbers from fixed, erasable, and special and central memory, checking that the final results are coreedt and the erasable memory multipliers are not lost during the multiply.

4.2.3.28 DIVIDE Test (Ref. paragraph 3.1.1.5) Divide combinations of ±, ± 0 and ±, ±0 double precision numbers by ± numbers checking for the correct results. Division is made from erasable and special and central checking that the divisor is not changed during the division.

4.2.3.29 READ Test (Ref. paragraph 3.1.1.5) Load L and Q with ± 0 and ± overflow numbers and check that proper results are read out while not destroying contents of L and Q.

4.2.3.30 WRITE Test (REf. paragraph 3.1.1.5) Write ± 0 and ± overflow numbers into L and Q. Check that write did not change A and that proper contents were stored in L and Q.

4.2.3.31 RAND Test (Ref. Paragraph 3.1.1.5) Load L and Q with alternating bit pattern and check RAND instruction when A has reverse alternating bit pattern and NZ. Also load L and Q with ± overflow numbers and check RAND instruction when A has NZ. L and Q are checked after each RAND to insure they have not been destroyed.

4.2.3.32 WAND Test (Ref. paragraph 3.1.1.5) WAND instruction checked by writing 52525, 25252, ± 0, ± overflow numbers into L and Q and checking for correct contents of A after the instruction.

4.2.3.33 ROR Test (Ref. paragraph 3.1.1.5) Check ROR instruction by loading L and Q with alternating bit patterns and ± overflow numbers and checking the contents of A, L and Q after the ROR instruction has been performed.

4.2.3.34 WOR Test (Ref. paragraph 3.1.1.5) Check WOR instruction by loading L and Q with ± 0 and write alternate bit patterns PFS and ± overflow numbers checking A, L and Q after each write.

4.2.3.35 RXOR Test (REf. paragraph 3.1.1.5) Check RXOR instruction by loading L and Q with NZ and ± overflow numbers and after each read checking contents of A, L and Q.

4.2.3.36 Checksum (Ref. paragraph 3.1.1.4) This routine takes a double precision checksum of any or all of the six modules as specified by the user and checks the sum against pre-stored values on the module level.

4.2.3.37 Check that Time 3 overflow causes an interrupt, by presetting only time 4 to overflow in a short period of time. (Ref. paragraph 3.1.1.9)

4.2.3.38 Check that Time 4 overflow causes an interrupt, by presetting only time 4 to overflow in a short period of time. (Ref. paragraph 3.1.1.9)

4.2.3.39 EDRUPTN (Ref. paragraph 3.1.1.5) Check that EDRUPT will transfer control to the A-register if no interrupt has been requested.

4.2.3.40 NORUPTN (Ref. paragraph 3.1.1.6) Check that no interrupts occurring will cause a gojam within a 140-300 ms period.

4.2.3.41 RUPTLOCN (Ref. paragraph 3.1.1.6) Check that inhibiting interrupts for too long will cause an interrupt during a 140-300 ms period.

4.2.3.42 RELINT3N (Ref. paragraph 3.1.1.6) Check that INHINT and RELINT work by causing an interrupt while inhinting and then relinting.

4.2.3.43 PRIORN (Ref. paragraph 3.1.1.9) Basic check of priority circuit by causing a Time 3 and Time 4 interrupt while inhibiting interrupts, and check the order of execution after a RELINT has been performed.

4.2.3. 44 XPARN (Ref. paragraph 3.1.1.6) Check that 13 words of bad parity will each case a gojam.

4.2.3.45 ALLPARN (Ref. paragraph 3.1.1.7) Write all bit combinations into one location and check that no bad parity occurs.

4.2.3.46 INRUPTN (Ref. paragraph 3.1.1.6) Do not resume from a Time 6 interrupt and check that a gojam occurs within a 140-300 ms period.

4.2.3.47 TCA Trap Test (Ref. paragraph 3.1.1.6) Check that executing a TC or TCF loop will cause a gojam within a 5-15 ms period.

4.2.3.48 NTWTCHMAN (Ref. paragraph 3.1.1.6) Check that not accessing location 0067 within a .64-1.92 sec. period will cause a gojam.

4.2.3.49 SELF Test (Ref. paragraph 3.1.1.5)

4.2.3.50 I/O STARTP (Ref. paragraph 3.1.1.8) This test is designed to check the decoding circuitry of downlink channels 34 and 35. Before describing the actual test performed to insure that this is doen properly, a brief discription of the circuitry involved will be given.

In essence the downlink circuitry consists of 2 channels, 34 and 35, which contain the information to be transmitted. A five-stage counter, whose outputs are decoded to gate out one bit of information at a time. A signal, DKBSNC, enables the output data to be transmitted and causes the 5-stage counter to be "incremented." Another signal, DKSTRT, resets the five-stage counter.

Bit 7 of channel 13 may best be described by saying that it functions as a "flag bit" for the downlink data and is gated out by signal DKBSNC when the five-stage counter is in the zero state, that is, reset.

4.2.3.50 cont.

The outputs from the five-stage counter are decoded and function as follows:

Stages 4 and 5 divide channel 34 and 35 into four 8 bit sections. Stages 1, 2, and 3 are decoded and enable a single bit from an 8 bit section to be transmitted.

For clarity it will be stated that bit 16 is the first bit transmitted from a channel while the parity bit is the last bit transmitted. Channel 34 is transmitted before channel 35.

Following is a list of interface connections used to generate the required downlink signals:

GYRRST causes DKSTRT which resets the 5-stage counter
GYRSET causes DKBSNC which steps the counter
DKDATA causes XLINK1 which allows the downlink output bits to be stored in counter 45.

GYRRST and GYRSET are controlled by bit 10 of channel 14 and the contents of out counter 47. The number of times signal GYRSET is generated is determined by the contents of counter 47. Signal GYRRST is generated whenever GYRSET is not. Both occur at a frequency of 3200 cps.

Following is a list of checks performed within this test to insure proper decoding:

C(34)	C(35)	#BITSYNC'S Generated	C(45)
00177	77777	9	00000

The above test proves that only one of the four 8 bit sections is active and that it is the proper one.

37600	77777	2	00000
17600	77777	3	00000
07600	77777	4	00000

These three tests plus the first test of the next group are sufficient to prove that multiple decoding is not present within the eight bit section.

40000	77777	5	00001
37600	77777	3	00001
17600	77777	4	00001
07600	77777	5	00001
03600	77777	6	00001
01600	77777	7	00001
00600	77777	8	00001
00200	77777	9	00001

The above eight tests prove that the lower 3 stages of the 5 stages are getting decoded properly and that each of eight states is capable of gating a data bit out of channel 34.

4.2.3.50 cont.

*10000	77777	17	00000
10100	*10177	25	00000
10100	*10000	33	00000

The above three tests prove that the remaining three states of stages 4 and 5 are getting decoded properly and activate the proper 8 bit section.

*40177	10000	17	00377 (eight puls
*40000	77600	25	00377
40000	*40177	33	00377

These three tests show that each of the bits within an 8 bit section is capable of being transmitted.

*The input to counter 45 is inhibited until the position being interrogated is beyond this point.

The last check performed in this section is set channel 34 and 35 to zero, set bit 7 of channel 13 to a one and generate two BITSYNC pulses. Counter 45 is checked for 1 pulse, if this test is successful bit 7 of channel 13 is functioning properly.

4.2.3.51 I/O STPIP (Ref. paragraph 3.1.1.8) The purpose of this test is to check the GYRO signals controlled by channel 14, bits 7 through 10, and the associated circuitry of PIPA counters 37, 40 and 41.

The following interface connections are made in order to accomplish this test:

Load CH. 14				Generate Signal	Causes Counter Request
10	9	8	7		
1	0	0	0	None	None
1	0	0	1	GYXP	PINC 37
1	0	1	0	GYXP	PINC 40
1	0	1	1	GYZP	PINC 41
1	1	0	0	None	None
1	1	0	1	GYXM	MINC 37
1	1	1	0	GYXM	MINC 40
1	1	1	1	GYZM	MINC 41

Ordinarily this signal pairing would not function properly, since the BYRO signals occur at a 102.4 KC rate and are gated by computer timing signal SB1. The PIPA counter increments are generated during SBZ time. It was therefore necessary to invert the counter increment requests being generated by the GYRO signals. This was accomplished by wiring the high side of GYRO output transformer to the low side of the PIPA input transformer. Computer signal PIPSAM then converted the 102.4 KC GYRO signals to 3200 KC counter increment requests for the three PIPA counters.

Associated with the PIPA counter increment requests is a circuit which rejects the first three consecutive pulses of one type, i.e., the first three PINC requests or three MINC requests.

4.2.3.51 cont.

In order to check that all of the above circuitry is functioning properly the following tests are made for each code which is entered into channel 14.

Enter a code into channel 14 which will pre-condition the PIPA circuits so that the first three counter increment requests generated by the test code will be rejected. Enter the code to be tested into channel 14. When bit 10 of channel 14 gets reset, go check the counter which was to be incremented for the proper number of pulses. Then check that the other two counters contain positive zero, that is, they did not receive any pulses.

The number of pulses gated out for each test is octal 103. The counter being tested is checked for octal 100.

In the case of the two illegal codes, all three counters are checked for positive zero.

The term pre-condition implies that when the code to be tested will cause PINCS on a counter, the code which MINCS the same counter is used to set the PIPA rejection circuit to a known state. Therefore the first three positive increment requests will be rejected. The reverse is also true when the MINC codes for each counter are tested.

4.2.3.52 I/O Test 1V (Ref. paragraph 3.1.1.8) This test checks that out counters 50 through 54 are diminished by instruction DINC when the proper bit is written into channel 14. This is accomplished by wiring the resultant interface signals which are generated during instruction DINC into circuits which request counter increments.

Load Ch. 14 Bit	DINC OUTCTR	If Contents of OUTCTR is	Generate Interface Signal	This is Wired Into	Causes Counter Request
16/15	50	Positive	CDUXDP	CDUXP	PCDU 32
	50	Negative	CDUXDM	CDUXM	MCDU 32
14	51	Positive	CDUYDP	CDUYP	PCDU 33
	51	Negative	CDUYDM	CDUYM	MCDU 33
13	52	Positive	CDUZDP	CDUZP	PCDU 34
	52	Negative	CDUZDM	CDUZM	MCDU 34
12	53	Positive	TRNDP	TRNP	PCDU 35
	53	Negative	TRNDM	TRNM	MCDU 35
11	54	Positive	SHFTDP	SHAFTP	PCDU 36
	54	Negative	SHFTDM	SHAFTM	MCDU 36

PCDU causes a counter to be incremented in two's complement arithmetic.

The CDU-DP or M signals are generated until the contents of the out counter are diminished to minus zero. At this time the channel bit which was requesting the DINC instruction is reset and checked.

In this routine each counter pair, 32+x, 50+x (x = 0 to X = 4) is tested separately. Four tests are performed on each pair. Initially 32+x is set to -30. The following numbers are placed in 50+x.

4.2.3.52 cont.

Trial 1. $+30_{10}$

" 2. $+30_{10}$

" 3. -30_{10} (1's complement)

" 4. -30_{10} (1's complement)

The corresponding 32+x values should become -
results of trial 1. +0
" " " 2. $+30_{10}$
" " " 3. +0
" " " 4. -30 (2's complement)

When performing a trial, after one of the above numbers is placed on 50+x and its corresponding drive bit set, the program waits until the drive bit resets and then checks 32+x for the expected result. Inorder to avoid an endless loop in the case of the drive bit not resetting, a time limiting loop has been incorporated. If the drive bit does not reset within the given time (aproximately 10 msec.) the test fails.

4.2.3.53 I/O Test 2V (Ref. paragraph 3.1.1.8) This test checks that the radar control codes which are associated with bits 1 through 4 of channel 13 are functioning properly. This is accomplished by using the decoded radar signals to generate increment requests for BMAG counters 42, 43, and 44. Bit 8 of channel 13 also gets tested since the counter requests which are generated at the interface module must pass through circuitry which is enables by this bit.

Below is a sequence of events which occur when a code is entered into the lower 4 bits of channel 13.

Ch. 13 Code				Radar Siganl Generated	Counter Request Generated	Type of Increment Requested	On CTR #
4	3	2	1				
1	0	0	0	None	None	None	None
1	0	0	1	RR RANG	BMGXP	PINC	42
1	0	1	0	RR RARA	BMGXM	MINC	42
1	0	1	1	None	None	None	None
1	1	0	0	LRSVEL	BMGYP	PINC	43
1	1	0	1	LRYVEL	BMGYM	MINC	43
1	1	1	0	LRZVEL	BMGZP	PINC	44
1	1	1	1	LR RANG	BMGZM	MINC	44

The radar signals are generated at a 3200 cycle/second rate for a period of 90 ms. This results in the generation of 256 pulses each time a code is entered into channel 13.

4.2.3.53 cont.

Initially, in this test, counters 42-44 are set to +0 and three tests are performed with each radar code and bit 8 of channel 13 set.

In the case of codes 11, 14, and 16 the proper counter is initialized at -400_8. The first request should PINC the counter to -0. The second request of the same code should MINC it to -377_8. It is then set to 40400_8. After the next request of the same code it should read 40000_8.

A test is performed with each radar code and bit 8 of channel 13 reset to ascertain that the counter accessed will not change in value.

The program periodically checks that no counter has changed form +0 other than the one to which a request is sent.

Each counter request should produce a RADARUPT. The program checks to see that this has occurred.

When bit 4 in channel 13 is reset, the program knows that the proper counter should contain the expected value and that the RADARUPT should have occurred. A timing loop has been incorporated to prevent an endless loop from occurring in the event bit 4 of channel 13 was not reset.

The no signal codes (10 and 13) are used to check that no signals are generated to any counter.

4.2.3.54 I/O Test 3V (Ref. paragraph 3.1.1.8) This test checks that bit 1 of channel 14 controls the OUTLINK circuitry and that this circuitry is functioning in the prescribed manner. Bit 1 of channel 14 causes the computer to generate a FLAG bit for the OUTLINK data and then shifts the 15 bits of OUTLINK data out of counter 57. Each of these 16 bits generate either a OTLNK1 or OTLNKO signal in the interface module depending on whether or not the data bit was a "1" or a "0" respectively. These signals are then used to generate SHINC and SHANC instructions for the UPLINK counter.

OTLNK1 causes UPLINK1 which requests a SHANC on counter 45.
OTLNKO causes UPLINKO which reqhests SHINC on counter 45.

This causes the data of counter 57 to be duplicated in counter 45.

Bits 5 and 6 of channel 13 are also incorporated in this test since they control the inhibit or enable status of the UPLINK counter.

4.2.3.54 cont.

Four checks are performed here. They are -

I.
1. Set Channel 13 bits 5 and 6 to 00.
2. Set counter 57 to 25252_8 counter 45 = 0, and Channel 14 bit 1 = 1.
3. Wait a maximum of 10 ms for Channel 14 bit 1 to reset. If it has not reset within this time, test fails.
4. Delay 5 more ms.
5. Check that an UPRUPT occurred. If not, Fail.
   UPRUPT should have been caused when the flag bit was detected in bit 16 of CTR 45.
6. Check that counter 45 now contains 25252_8. If not, Fail.

II.
1. Set Channel 13 bits 6 and 5 to 10 (INHIBIT UPLINK).
2. Set counter 57 to 25252, counter 45 = 0 and channel 14 bit 1 = 1.
3. Wait a maximum of 10 ms for channel 41 bit 1 to reset. If it has not reset within this time, test fails.
4. Delay 5 more ms.
5. Check that no UPRUPT occurred. If it did, Fail.
6. Check that counter 45 still contains 0. If not, Fail.

III. Same as I above except set CTR 57 to 52525 in step 2 and expect 52525 in CTR 45 in step 6.

IV. Same as II above except set CTR 57 to 52525 in step 2.

4.2.3.55 I/O Test 4V (ref. paragraph 3.1.1.8) This test checks that bits 2 and 3 of channel 14 control the altitude meter circuitry and that this circuitry is functioning in the prescribed manner.
Bit 3 of channel 14 causes the computer to generate a flag bit for the altitude meter data and then shift the 15 data bits out of counter 60. Bit 2 selects one of the two paths by which the data may be transmitted.

Bit 2	Data Bit	Transmit Via
0	0	ALT0
	1	ALT1
1	0	ALRT0
	1	ALRT1

The wiring at the interface is such that -

ALT0 causes RRIN0,
ALT1 causes RRIN1,

ALRT0 causes LRIN0,
ALRT1 causes LRIN1,

These RR and LR signals will be converted to counter requests for

4.2.3.55 cont.

SHINC and SHANC on counter 46 when a radar code is loaded into channel 13.

The following is a list of the tests which are done to insure proper operation of the combined circuitry.

Load Ch. 14 Bits		Load Ch. 13 Bits				Data Expected in Computer
3	2	4	3	2	1	
1	0	1	0	0	0	None
		1	0	0	1	Duplicate of counter 60
		1	0	1	0	Duplicate of counter 60
1	1	1	0	0	0	None
		1	1	0	0	Duplicate of counter 60
		1	1	0	1	Duplicate of counter 60
		1	1	1	0	Duplicate of counter 60
		1	1	1	1	Duplicate of counter 60

There are two checks made for each code listed for channel 13. In the first check counter 60 is loaded with an odd bit configuration, in the second check counter 60 is loaded with an even bit configuration. The two results are then added and the answer checked for minus zero. Where no data is expected the answer is checked for positive zero.

There is one other test performed, and that is one the generation of the flag bit from the altitude meter circuitry. Unlike counter 45 there are no interrupts generated when the flag bit is sensed in position 16 of the counter and therefore this bit is not self checking.

This check consists of loading counter 60 with a plus one and waiting until this bit has been shifted one place to the left. At this time, counter 46 is checked to see that it contains the same information.

Radar code 1011 is not implemented and should not be tested.

4.2.3.56 I/O Test 5V (Ref. paragraph 3.1.1.8) This test checks that out counters 55 and 56 are diminished by instruction DINC when the proper bit is written into channel 14. This accomplished by wiring the resultant interface signals which are generated during instruction DINC into circuits which request counter increments.

4.2.3.56 cont.

Load Ch. 14 Bit	DINC OUTCTR	If Contents of OUTCTR is	Generate Interface Signal	This is Wired Into	Causes CTR Request
4	55	Positive	+THRST	BMGXP	PINC 42
	55	Negative	-THRST	BMGXM	MINC 42
5	56	Positive	+EMS	BMGYP	PINC 43
	56	Negative	-EMS	BMGYM	MINC 43

Bit 8 of channel 13 is also used since it enables the counter requests to be gated into the counter cells.

Following is a list of tests actually performed.

I.
1. Write 1 into channel 13 bit 8.
2. 0 CTR 42 (BMAGX), 0 CTR 43 (BMAGY).
3. 377_8 CTR 55.
4. Set channel 14 bits 5, 4 = 01.
5. Wait until channel 14 bit resets (100 ms is allowed).
6. Does CTR 42 = 377_8? If not, error.

II. Same as I except 77400_8 CTR 55 (step 2) and 77400_8

III.
1. Write 1 into channel 13 bit 8.
2. 0 CTR 42 0 CTR 43.
3. 377_8 CTR 56.
4. Set channel 14 bits 5, 4 - 10.
5. Wait until channel 14 bit resets (100 ms is allowed).
6. Does CTR 43 - 377_8? If not, error.

IV. Same as III except 77400 CTR 56 (step 2) and 77400_8 expected on CTR 43 (step 6).

4.2.3.57 I/O Test 6V (Ref. paragraph 3.1.1.8) This test is performed in order to check the decoding circuitry controlled by bits 5 and 6 of channel 13. These two bits are decoded such that information may be gated into the UPLINK counter, via of counter priority cells, from two different sources. That is, interface signal UPLINK or XLINK. It also checks that the circuit used for detecting excessive rates of information flow from these two sources is operative, and does control the INLINK TOO FAST bit of channel 33 when an excessive rate is detected. This is accomplished by using bit 6 of channel 14 to generate signal GYENAB and making the interface connection such that GYENAB causes XLINKO. The frequency of GYENAB is approximately 102 KC.

The following is a list of the eight tests which are performed -

4.2.3.56 cont.

Load Ch. 14 Bit	DINC OUTCTR	If Contents of OUTCTR is	Generate Interface Signal	This is Wired Into	Causes CTR Request
4	55	Positive	+THRST	BMGXP	PINC 42
	55	Negative	-THRST	BMGXM	MINC 42
5	56	Positive	+EMS	BMGYP	PINC 43
	56	Negative	-EMS	BMGYM	MINC 43

Bit 8 of channel 13 is also used since it enables the counter requests to be gated into the counter cells.

Following is a list of tests actually performed.

I.
1. Write 1 into channel 13 bit 8.
2. 0 CTR 42 (BMAGX), 0 CTR 43 (BMAGY).
3. 377_8 CTR 55.
4. Set channel 14 bits 5, 4 = 01.
5. Wait until channel 14 bit resets (100 ms is allowed).
6. Does CTR 42 = 377_8? If not, error.

II. Same as I except 77400_8 CTR 55 (step 2) and 77400_8

III.
1. Write 1 into channel 13 bit 8.
2. 0 CTR 42 0 CTR 43.
3. 377_8 CTR 56.
4. Set channel 14 bits 5, 4 - 10.
5. Wait until channel 14 bit resets (100 ms is allowed).
6. Does CTR 43 - 377_8? If not, error.

IV. Same as III except 77400 CTR 56 (step 2) and 77400_8 expected on CTR 43 (step 6).

4.2.3.57 I/O Test 6V (Ref. paragraph 3.1.1.8) This test is performed in order to check the decoding circuitry controlled by bits 5 and 6 of channel 13. These two bits are decoded such that information may be gated into the UPLINK counter, via of counter priority cells, from two different sources. That is, interface signal UPLINK or XLINK. It also checks that the circuit used for detecting excessive rates of information flow from these two sources is operative, and does control the INLINK TOO FAST bit of channel 33 when an excessive rate is detected. This is accomplished by using bit 6 of channel 14 to generate signal GYENAB and making the interface connection such that GYENAB causes XLINKO. The frequency of GYENAB is approximately 102 KC.

The following is a list of the eight tests which are performed -

4.2.3.57 cont.

Set Ch. 13		Set Ch. 14	In Ch. 33
Bits 6	5	Bit 6	Bit 11 Look for a
0	0	1	1
1	0	1	1
1	1	1	1
0	1	1	0

The four are then repeated with bit 6 of channel 14 set to zero. For these four tests bit 11 of channel 33 should remain a one. The bits of channel 33 are inverted. Therefore bit 11 will be a one until the INLINK TOO FAST signal is present.

In checks one and two, bit 5 inhibits information from entering the counter priority cells via XLINK, therefore the excessive rate of XLINKO is not detected. In check three, bit 6 inhibits reception of INLINK data from either source, again the excessive rate should not be detected.

In check number four the combination of bits 5 and 6 allows information to be gated into the INLINK cirucitry via XLINK and at this time the excessive rate of XLINKO is detected and signal INLINK TOO FAST is generated, channel 33 bit 11 set to zero.

4.2.3.58 Special Rope Test (Ref. Paragraph 3.1.1.4). Individual, time dependent checksums will be performed on each of the abbreviated rope modules. The checksum used will accomplish more than an ordinary checksum. The program will be written to detect interchanged strand wiring and interchanged inhibit wiring. The program will also check proper resetting of the cores.

4.2.3.59 Register 20-23 & NDX Generation (Ref. Paragraph 3.1.1.5). Check the proper operation of all instructions on registers 20-23. Check worst case add by adding all possible numbers to NZ. Check that INCR and AUG instructions will cause interrupts when overflow results are obtained in Time 5, and executing the RUPT by using the EDRUPT instruction. Check the proper operation of INCR on Time 1 and Time 2. Generate all instructions by using INDEX instructions. Check that gojam will reset channels 5, 6, 10, 11, 12, 13, 14, 34, and 35.

4.2.3.60 DSKY Display (Ref. Paragraph 3.1.1.14). Turn OFF all lights on the DSKY's. Turn ON all alarms, 9's +sign, and V/N flash, turn ON all 8's and -sign. Turn ON all 7's-0's consecutively without sign. Blank the DSKY.

TIMECHKS consist of 16 tests described below --

(Tests #'s 1, 2, & 3 Ref. Paragraph 3.1.1.10)
(Test #4, Ref. Paragraph 3.1.1.11)
(Tests #5 thru #16, Ref. Paragraph 3.1.1.10)

All time counters and channels 3 and 4 are checked from proper frequency of incrementing. T1 through T6 are checked for proper phasing to each other. The external clock indicates amount of time actually taken. DSKY displays the amount that should have been taken.

Test #1 - Allow channel 4 to count from 0 to 0. Should take 5120 ms.

Test #2 - Allows channel 4 to pulse 32 times. Should take 10 ms.

Test #3 - Waits for channel 3 to pulse once. Should take 5120 ms.

4.2.3.60 (Cont'd)

Test #4 - Loads and checksums erasable memory, stores CH3 and 4 time and goes into Standby. Upon returning from Standby it computes the number of increments which Ch3 and 4 should have received and displays them -- the operator can then compute whether the external clock reading is accurate. It also does a checksum on E memory to see that it remained undisturbed by the Standby mode.

Test #5 - Allows each time counter (Time 1-5) to count from 1 to 0.
thru Each should take 163,830 ms.
Test #9

Test #10 - Allows time 6 to count from 37777_8 to -0. Should take 10.23938 secs.

Test #11 - Allows time 6 to count from 40000_8 to -0. Should take 10.23938.

Test #12 - Checks amount of time that elapses between incrementing of time 3 and 4. Should be 7.5 ms.

Test #13 - Checks amount of time that elapses between incrementing of time 3 and time 5. Should be 5.0 ms.

Test #14 - Checks amount of time that elapses between incrementing of time 4 and time 1. Should be 2.5 ms.

Test #15 - Checks phasing from time 4 to time 2. Should be 2.5 ms because time 1 is set to PFS at each time 2 change.

Test #16 - Checks phasing from time 3 to time 6. Should be .3125 ms.

4.2.3.61 Worst Case Noise Erasable Memory Test (Ref. Paragraph 3.1.1.3) Banks 0 to 7 of erasable memory are loaded with the bit patterns as indicated in Table 1. Each work of bank 0 through 7 is checked in the following manner:

1. The word is read out and compared against the word that was stored.

2. One bit of the word (starting with bit 15) is complemented and together with the rest of the original word is restored into its previous location.

4.2.3.61 (Cont'd)

3. This word is then read out and checked for the proper bit configuration.

4. The original word is now restored to its proper location.

It should be noted that each bit as described in step 2 is done for all banks before the next bit in the word is complemented. This sequence of operations is repeated for all 15 bits of a word and when complete, each word that was stored originally, as indicated by Table 1, is now complemented and the process is repeated.

Upon successful completion the whole test is recycled. If an error is detected, the program will stop on a TC Trap.

Table 1

E Bank	Starting Address	Word Pattern
0	1424	0,0,1,1,0,0,1,1, etc,
1	1400	1,1,0,0,1,1,0,0, etc,
2	1400	1,1,0,0,1,1,0,0, etc,
3	1400	0,0,1,1,0,0,1,1, etc,
4	1400	0,0,1,1,0,0,1,1, etc,
5	1400	1,1,0,0,1,1,0,0, etc,
6	1400	1,1,0,0,1,1,0,0, etc,
7	1400	0,0,1,1,0,0,1,1, etc,

4.2.3.62 Warning Integrator Check Test (Ref. Paragraph 3.1.1.12). The purpose of this test is to check the warning alarm. Upon entering the test, the state of the warning alarm is examined. If on, the computer activity light is set; otherwise, it is reset. There is then a fifteen second delay during which the warning light should go OFF if it wasn't. If this does not happen, the STOP Fail routine is entered and the test terminated.

If the above check was successful, eight further checks are performed. Any of these checks which fail will not terminate the test -- just give a fifteen second indication of the failure on the DSKY and then continue to the next check.

4.2.3.62 (Cont'd)

The eight checks employ the same philosophy. Each is concerned with pulsing the test alarm bit every "Y" seconds over a period of "Z" seconds. The state of the warning bit is examined at the end of the "Z" seconds and, if it is not what is expected, there is a 15 second fail display. Otherwise, there is a 15 second success display.

Each time the test alarm bit is pulsed (i.e., every "Y" seconds during a check), the state of the warning bit is checked. When on, the computer activity light is set. When off, it is reset.

For the first four of the eight checks, the warning alarm bit is reset before the above described pulsing of the alarm bit is initiated. On the last four, the warning alarm bit is set.

During the performance of a particular check, the DSKY will display the following:

R1 = 8-"test #(1-8)"

R2 = "Y" - how often the test alarm bit is being pulsed (shown in seconds and hundredths of seconds)

R3 = "Z" - length of time over which the alarm bit is pulsed (in seconds).

At the end of the check, R2 and R3 are blanked and, if success, 8-"test #" remains in R1. Otherwise R1 becomes 9 -"test #".

The particulars for each check are as follows:

Check No.	R1 Display	R2 (Y) (1 pulse every Y.YY secs. for ZZ seconds)	R3 (Z)	Initial Warning State	End Expected Warning State
1	8-1	3.00	60	OFF	OFF
2	8-2	2.00	60	OFF	OFF or ON accepted.
3	8-3	1.00	12	OFF	ON
4	8-4	0.16	1	OFF	ON
5	8-5	0.50	60	ON	ON
6	8-6	1.00	60	ON	ON
7	8-7	2.00	60	ON	OFF or ON accepted.
8	8-8	3.00	60	ON	OFF

4.2.3.63 Supervisor. Displays failures for 15 seconds, forever, or returns to the next test. Displays number of successes and failures on DSKY at the end of a complete loop of tests. Failures display test number, address of failure, bank values, and number of failures to that point.

4.2.3.64 DSKY Checks (Ref. Paragraph 3.1.1.15). Check input of each key for proper codes. A continuous failure of the same type will terminate the test. Entries of keys within a .50 ms period will cause an alarm indication at all times.

4.2.3.65 Priority of Interrupts (Ref. Paragraph 3.1.1.12). Generate all interrupts and check that each occurs with correct priority.

4.2.3.66 DSKY Vibration. The computer is locked up and the DSKY cleared. If a keyrupt occurs while the DSKY is being vibrated, this entry is displayed in the R1 component of both DSKY's. The display represents the total number os such entries since the beginning of the test.

4.2.3.67 BEGINP Test (Ref. Paragraph 3.1.1.8). Briefly, channels 30, 31 and 32 received information, DC signals, which are controlled by switches on the CTS. Some of these signals, CH31, bits 1-12 and CH32, bits 1-10, may cause rupt 10 when enabled by the proper bit of channel 13. The breakdown is as follows:

CH13 Bit	Enables	If Ch32 contains any of the following bits	If CH33 contains any of the following bits
12	rupt 10	1 through 6	-
13	rupt 10	7 through 12	-
14	rupt 10	-	1 through 10

4.2.3.67 (Cont'd)

This test then checks that CH30, 31 and 32 received DC signals in the proper bit positions via the interface module. Also it checks to see that the interrupt is controlled by the proper bit position of channel 13 and occurs when requested.

Following is a description of the way in which this is handled.

Initially check to see that CH30, 31 and 32 have no bits present. Turn OFF COMP. ACT. This signals the operator that it is OK to stard checking the switches, beginning at CH30, switch position one.

When the program finds that the switch has been turned ON, it checks to see that it is the proper switch, if it is, it then checks the other two channels to insure that they do not have bits present. It both of these checks pass, the COMP ACT, is turned ON in the DSKY and the A register shows a five second flashing display of the bit just tested. After 5 seconds the COMP ACT. is turned OFF, this signals the operator to turn OFF the switch just tested and turn ON the next switch to the left. When a test is completed on an entire channel the next switch to be tested is switch number one of the next channel.

The following is a list of DSKY indications used in this test, and their interpretation.

NO ATT	Operator failed to turn ON next test vit within one minute of completion of testing of last bit.
KEY RELEASE	Two adjacent switches are ON for 30 seconds. This situation arises when the operator turns ON the switch to be tested before he turns OFF the switch which was just checked.
GIMBAL LOCK AND HOLD	RUPT10 was caused by wrong bit.
HOLD	Detection of an improper bit in CH30, 31 or 32. Display on DSKY as follows: Noun - Channel where error was detected Reg1 = Octal display of CH30 Reg2 - Octal display of CH31 Reg3 - Octal display of CH32
HOLD with Flashing Verb, Noun	Interrupt did not occur when requested. Display contents of CH30, 31 and 32 as previously described.

4.2.3.67 (Cont'd)

OPERATOR ERROR	Operator failed to select and option for returning from one of the three hold conditions.
FREE	The selected option has been processed.

The options for returning to the test are requested by switches 1 and 2 or 14 and 15 of channel 30.

Switch	Function
1 or 14	Test same bit over
2 or 15	Start test at next bit position
1 and 2 or 14 and 15	Start test at position one of next channel.
None of the above	Operator error.

The procedure, for using the options when a hold condition exists is as follows:

Turn ON T12
Turn OFF all channel switches
Select an option
Push fresh start
Turn OFF T12
Press Proceed - Free light comes on

Turn ON T12
Turn OFF option switches
Push fresh start
Turn OFF T12
Press Proceed - DSKY clears and switch selected for testing may be turned on.

Procedure for returning from no ATT and KEY RELEASE conditions.

Turn ON T12
Correct condition which caused ALARM
Push fresh start
Turn OFF T12
Push Proceed - Routine starts test where it left off - if the same condition exists at this time, the operator will get a hold condition which is an error.

5. PREPARATION FOR DELIVERY

5.1 **GENERAL.** Preparation for delivery shall be in accordance with Specification ND 1002214. The Computer Assy and DSKY's shall be pressurized for shipment at 2.0 ± 0.5 psig with dry nitrogen at ambient room temperature.

6. NOTES. None.

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PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

INDICATOR DRIVER MODULE

DRAWING NO. 2003952

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA
6JAN67	A	32575	Initial Release		—

This specification consists of pages 1 to 14 inclusive.

APPROVALS	NASA/MSC	Eldon C Hall 11/18/66 W Stameris 8 Dec 1966 MIT/IL	C B McFadden 10/11/66 N.G. Parke 10/11/66 BC Dinton 10/11/66 E Bradshaw RAY

APOLLO G&N Specification
PS 2016009 Rev A
Original Issue Date:
Release Authority: TDRR
Class A Release

ADDENDUM NOTICE

This Specification has been prepared as an Addendum to:

Specification No. PS 2003952
Revision B

FOR

INDICATOR DRIVER MODULE

Used With

APOLLO G&N System

The exact content of specification PS 2003952 used as the basic document for this addendum is the revision referenced above, and the exceptions stated below.

1. SCOPE

This specification establishes the detail requirements for complete identification and acceptance of the Indicator Driver Module, Part Number 2003952-031.

2. APPLICABLE DOCUMENTS. Same as PS 2003952. Rev. B

3. REQUIREMENTS

3.1 PERFORMANCE. Same as PS 2003952.

3.1.1 Thermal Conditioning. Same as PS 2003952.

3.1.2 Continuity. Same as PS 2003952.

3.1.3 Insulation Resistance. Same as PS 2003952.

3.1.4 Definition of Insulation Resistance - Pin Group A. Same as PS 2003952.

3.1.5 Insulation Resistance - Pin Group B. Same as PS 2003952.

3.1.6 Insulation Resistance - Pin Group C. Same as PS 2003952.

3.1.7 Insulation Resistance - Pin Group D. Same as PS 2003952.

3.1.7.1 Same as PS 2003952.

3.1.7.2 Same as PS 2003952.

3.1.7.3 Same as PS 2003952.

3.1.8 Insulation Resistance - Pin Group E. Same as PS 2003952.

3.1.8.1 Same as PS 2003952.

3.1.8.2 Same as PS 2003952.

3.1.8.3 Same as PS 2003952.

3.1.8.4 Same as PS 2003952.

3.1.8.5 Same as PS 2003952.

3.1.8.6 Same as PS 2003952.

3.1.9 Insulation Resistance - Pin Group F. Same as PS 2003952.

3.1.9.1 Same as PS 2003952.

3.1.9.2 Same as PS 2003952.

3.1.9.3 Same as PS 2003952.

3.1.9.4 Same as PS 2003952.

3.1.9.5 Same as PS 2003952.

3.1.9.6 Same as PS 2003952.

3.1.10 Resistance - Pin Group G. Same as PS 2003952.

3.1.11 Resistance - Pin Group H. Same as PS 2003952.

3.1.12 Front to Back Resistance Ratio. Same as PS 2003952.

3.1.13 Resistance. Same as PS 2003952.

3.1.14 Capacitance. Same as PS 2003952.

3.1.15 Inductance. Same as PS 2003952.

3.1.16 Input Voltage. The module shall perform as specified herein when supplied with the following voltages:

(a) 17.5 ± 0.1 vdc
(b) 19.0 ± 0.1 vdc
(c) 28.0 ± 0.1 vdc
(d) 35.5 ± 0.1 vdc

3.1.17 Set and Reset Pins. Same as PS 2003952.

3.1.18 Relay Contact Closures. With a voltage of 17.5 ± 0.1 vdc applied for 15.0 +0.0, -1.5 msec to the module input pins listed in Table 3-1, and module pins 66, 67, and 71 connected to 0 vdc, contact closures shall be made between the module output pins as specified in Table 3-1.

Table 3-1 (Same as PS 2003952).

3.1.19 Relay Contact Closures. With a voltage of 17.5 ± 0.1 vdc applied to module pins 23, 44, 62, 65, and 77 for 15.0 +0.0, -1.5 msec, and module pins 66, 67, and 71 connected to 0 vdc, contact closures shall be made between module pin 32 and module pins 17, 22, 24, 29, 30, 34, 36, 39, 40, 41, 42, 43, 49, 50, 53, 54, 55, 56, 78, 83, and 84.

3.1.19.1 With a voltage of 17.5 ± 0.1 vdc applied to module pins 66, 67, and 71, and module pins 23, 44, 62, 65, and 77 connected to 0 vdc, contact closure shall remain between the module pins listed in paragraph 3.1.19.

3.1.20 Relay Contact Closure. With a voltage of 17.5 ± 0.1 vdc applied to module pins 14, 35, 51, 61, and 73 for 15.0 +0.0, -1.5 msec, and module pins 66, 67, and 71 connected to 0 vdc, contact closures shall be made between module pin 16 and module pins 17, 22, 24, 29, 30, 34, 36, 39, 40, 41, 42, 43, 49, 50, 53, 54, 55, 56, 78, 83, and 84.

3.1.20.1 With a voltage of 17.5 ± 0.1 vdc applied to module pins 66, 67, and 71 and module pins 14, 35, 51, 61, and 73 connected to 0 vdc, contact closure shall remain between the module pins listed in paragraph 3.1.20.

3.1.21 Relay Contact Closures. With a voltage of 17.5 ± 0.1 vdc applied to module pins 28, 48, 59, 75, and 81 for 15.0 +0.0, -1.5 msec, and module pins 47, 69 and 88 connected to 0 vdc the following conditions shall exist:

(a) Contact closure shall be made between the pairs of module pins listed below:

37 and 25
21 and 15
58 and 46
76 and 32
82 and 74
38 and 57
18 and 27
60 and 57
70 and 32
79 and 32

3.1.21 (Continued)

(b) No contact closure shall be made between the pairs of module pins listed below:

31 and 37
20 and 21
45 and 58
63 and 76
13 and 82
9 and 38
9 and 18
64 and 60
13 and 70
13 and 79

3.1.21.1 With a voltage of 17.5 ± 0.1 vdc applied to module pins 47, 69, and 88, and module pins 28, 48, 59, 75, and 81 connected to 0 vdc, contact conditions shall remain as specified in paragraph 3.1.21.

3.1.22 Relay Contact Closures. With a voltage of 17.5 ± 0.1 vdc applied to module pins 19, 33, 52, 72 and 80 for 15.0 +0.0, -1.5 msec, and module pins 47, 69, and 88 connected to 0 vdc the following conditions shall exist:

(a) Contact closure shall be made between the pairs of module pins listed below:

31 and 37
20 and 21
45 and 58
63 and 76
13 and 82
9 and 38
9 and 18
64 and 60
13 and 70
13 and 79

(b) No contact closure shall be made between the pairs of module pins listed below:

37 and 25
21 and 15
58 and 46
76 and 32
82 and 74
38 and 57
18 and 27
60 and 57
70 and 32
79 and 32

3.1.22.1 With a voltage of 17.5 ± 0.1 vdc applied to module pins 47, 69, and 88, and module pins 19, 33, 52, 72, and 80 connected to 0 vdc, contact conditions shall remain as specified in paragraph 3.1.22.

3.1.23 Relay Contact Closures. Same as PS 2003952.

3.1.23.1 Same as PS 2003952.

3.1.23.2 With a voltage of 19.0 ± 0.1 vdc applied to module pins 4 and 7, and module pin 26 connected to 0 vdc, the following conditions shall exist:

(a) Contact closure shall be made between the pairs of module pins listed below:

11 and 1
8 and 10
3 and 6

(b) No contact closure shall be made between the pairs of module pins listed below:

11 and 12
2 and 8
3 and 6

3.1.24 Alarm Drivers. Same as PS 2003952.

3.1.25 Y Line Drivers. Same as PS 2003952.

3.1.26 X Line Drivers. Same as PS 2003952.

3.1.27 Diode Decoding. Same as PS 2003952.

3.1.27.1 Output Pulses. Same as PS 2003952.

NOTE: During the dynamic tests specified in paragraphs 3.1.24 thru 3.1.27 module pin 105 shall be connected to 0 vdc, and module pin 112 shall be connected to a 28.0 vdc supply.

3.1.28 Marginal Voltages and Thermal Extremes:

3.1.28.1 Low Marginal Voltage/Low Temperature. The module shall perform as specified in paragraph 3.1.18 thru 3.1.27 when the ambient temperature and the input voltage requirements are set as follows:

(a) 17.0 volt input	17.0 ± 0.1 vdc
(b) 19.0 volt input	19.0 ± 0.1 vdc
(c) 28.0 volt input	19.5 ± 0.1 vdc
(d) ambient temperature	-10^{o}C $+0C^{o}$ $-2.8C^{o}$

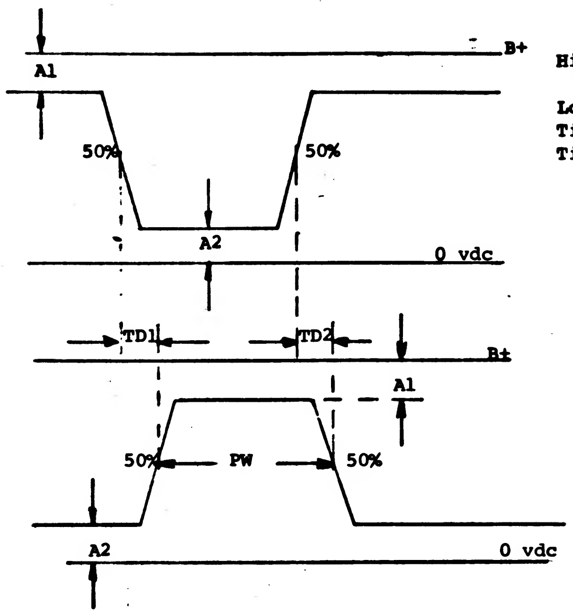

Figure 3-1B

High Level (A1)	NMT 1.5% of B+ below B+
Low Level (A2)	24%-30% of B+
Time Delay (TD1)	65 ± 40 usec
Time Delay (TD2)	20 ± 15 usec

Figure 3-1C

High Level (A1)	NMT 0.4V below B+
Low Level (A2)	NMT 0.1V
Pulse Width (PW)	15 ± 10 msec

Figure 3-1 Alarm Drivers Pulse Characteristics

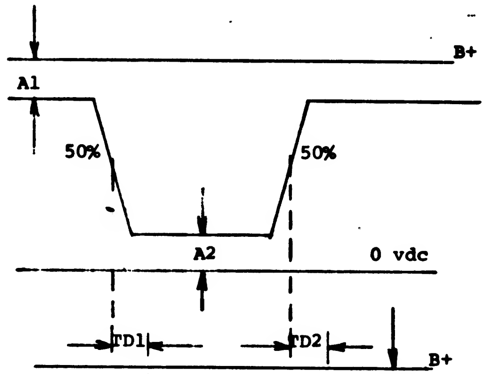

Figure 3-3A

High Level(A1)	NMT 1.5% of B+ below B+
Low Level(A2)	24%-30% of B+
Time Delay(TD1)	65 ± 40 usec
Time Delay (TD2)	20 ± 15 usec

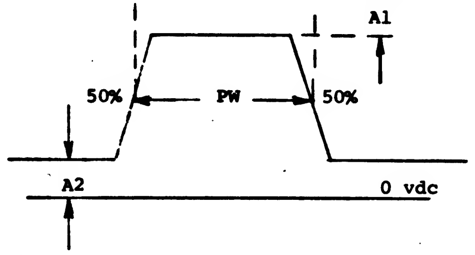

Figure 3-3B

High Level(A1)	NMT 0.4V below B+
Low Level(A2)	NMT 10% of B+
Pulse Width (PW)	15 ± 10 msec

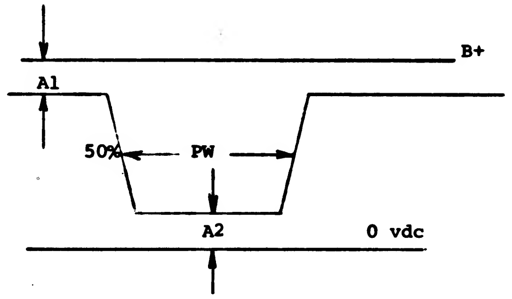

Figure 3-3C

High Level(A1)	NMT 0.4V below B+
Low Level(A2)	NMT 0.1 volt
Pulse Width(PW)	15 ± 10 msec

Figure 3-3 Y Line Drivers Output Pulse Characteristics

3.1.28.2 **Low Marginal Voltage/High Temperature.** The module shall perform as specified in paragraph 3.1.18 thru 3.1.27 when the ambient temperature and the input voltage requirements are set as follows:

(a)	17.0 volt input	17.0 ± 0.1 vdc
(b)	19.0 volt input	19.0 ± 0.1 vdc
(c)	28.0 volt input	19.5 ± 0.1 vdc
(d)	ambient temperature	$80^\circ C \; ^{+2.8C^\circ}_{-0C^\circ}$

3.1.28.3 **High Marginal Voltage.** The module shall perform as specified in paragraph 3.1.18 thru 3.1.27 when the ambient temperature and the input voltage requirements are set as follows:

(a)	17.0 volt input	35.5 ± 0.1 vdc
(b)	19.0 volt input	35.5 ± 0.1 vdc
(c)	28.0 volt input	35.5 ± 0.1 vdc
(d)	ambient temperature	25°C ± 3°C

3.1.29 Vibration. Same as PS 2003952.

3.2 PRODUCT CONFIGURATION

3.2.1 Drawings. Same as PS 2003952.

3.2.2 Weight. Same as PS 2003952.

4. QUALITY ASSURANCE PROVISIONS

4.1 General. Same as PS 2003952.

4.1.1 Nonconforming Units. Same as PS 2003952.

4.1.2 Test Conditions. Same as PS 2003952.

4.1.2.1 Environmental. Same as PS 2003952.

4.1.2.2 Module Case Ground. Same as PS 2003952.

4.2 TESTS

4.2.1 Drawing Compliance. Same as PS 2003952.

4.2.2 Thermal Conditioning. Same as PS 2003952.

4.2.3 Continuity. Same as PS 2003952.

4.2.4 Insulation Resistance. Same as PS 2003952.

4.2.5 Insulation Resistance - Pin Group A. Same as PS 2003952.

4.2.6 Insulation Resistance - Pin Group B. Same as PS 2003952.

4.2.7 Insulation Resistance - Pin Group C. Same as PS 2003952.

4.2.8 Insulation Resistance - Pin Group D. Same as PS 2003952.

4.2.8.1 Same as PS 2003952.

4.2.8.2 Same as PS 2003952.

4.2.8.3 Same as PS 2003952.

4.2.9 Insulation Resistance - Pin Group E. Same as PS 2003952.

4.2.9.1 Same as PS 2003952.

4.2.9.2 Same as PS 2003952.

4.2.9.3 Same as PS 2003952.

4.2.9.4 Same as PS 2003952.

4.2.9.5 Same as PS 2003952.

4.2.9.6 Same as PS 2003952.

4.2.10 Insulation Resistance - Pin Group F. Same as PS 2003952.

4.2.10.1 Same as PS 2003952.

4.2.10.2 Same as PS 2003952.

4.2.10.3 Same as PS 2003952.

4.2.10.4 Same as PS 2003952.

4.2.10.5 Same as PS 2003952.

4.2.10.6 Same as PS 2003952.

4.2.11 Resistance - Pin Group G. Same as PS 2003952.

4.2.12 Resistance - Pin Group H. Same as PS 2003952.

4.2.13 Front to Back Resistance Ratio. Same as PS 2003952.

4.2.14 Resistance. Same as PS 2003952.

4.2.15 Capacitance. Same as PS 2003952.

4.2.16 Inductance. Same as PS 2003952.

4.2.17 Input Voltage. Same as PS 2003952.

4.2.18 Relay Contact Closures. Same as PS 2003952.

4.2.19 Relay Contact Closures. Apply an input of 17.5 ± 0.1 vdc to the designated module pins as specified in paragraph 3.1.19. Verify contact closure by switching not less than 375 vdc between the module pins specified in paragraph 3.1.19.

4.2.19.1 Apply an input of 17.5 ± 0.1 vdc to the designated module pins as specified in paragraph 3.1.19.1. Verify that the contact closure conditions remain as specified in paragraph 4.2.19.

4.2.20 Relay Contact Closures. Apply an input of 17.5 ± 0.1 vdc to the designated module pins as specified in paragraph 3.1.20. Verify contact closure by switching not less than 375 vdc between the module pins specified in paragraph 3.1.20.

4.2.20.1 Apply an input of 17.5 ± 0.1 vdc to the designated module pins as specified in paragraph 3.1.20.1. Verify that the contact closure conditions remain as specified in paragraph 4.2.20.

4.2.21 **Relay Contact Closures**. Apply an input of 17.5 ± 0.1 vdc to the designated module pins as specified in paragraph 3.1.21. Verify contact closure by switching not less than 375 vdc between the module pins specified in paragraph 3.1.21 (a). Verify that no contact closure is made between the module pins specified in paragraph 3.1.21 (b).

4.2.21.1 Apply an input of 17.5 ± 0.1 vdc to the designated module pins as specified in paragraph 3.1.21.1. Verify that the contact closure conditions remain as specified in paragraph 4.2.21.

4.2.22 **Relay Contact Closures**. Apply an input of 17.5 ± 0.1 vdc to the designated module pins as specified in paragraph 3.1.22. Verify contact closure by switching not less than 375 vdc between the module pins specified in paragraph 3.1.22 (a). Verify that no contact closure is made between the module pins specified in paragraph 3.1.22 (b).

4.2.22.1 Apply an input of 17.5 ± 0.1 vdc to the designated module pins as specified in paragraph 3.1.22.1. Verify that the contact closure conditions remain as specified in paragraph 4.2.22.

4.2.23 **Relay Contact Closures**. Same as PS 2003952.

4.2.23.1 Same as PS 2003952.

4.2.23.2 Apply an input of 19.0 ± 0.1 vdc to the designated module pins as specified in paragraph 3.1.23.2. Verify contact closure by switching not less than 375 vdc between the module pins specified in paragraph 3.1.23.2 (a). Verify that no contact closure is made between the module pins specified in paragraph 3.1.23.2 (b).

4.2.24 Alarm Drivers. Same as PS 2003952.

4.2.24.1 Input Source. Same as PS 2003952.

4.2.24.2 Output Load. Same as PS 2003952.

4.2.25 Y Line Drivers. Same as PS 2003952.

4.2.25.1 Input Source. Same as PS 2003952.

4.2.25.2 Output Load. Same as PS 2003952.

4.2.26 X Line Drivers. Same as PS 2003952.

4.2.26.1 Low Level Input. Same as PS 2003952.

4.2.26.2 High Level Input. Same as PS 2003952.

4.2.26.3 Output Load. The output load shall be a 62 ohm ± 5% resistance connected between each module output pin and a 28 vdc supply.

4.2.27 Diode Decoding. Same as PS 2003952.

4.2.27.1 Input Source. Same as PS 2003952.

4.2.27.2 Output Load. The output load shall be an 18 Kohm ± 5% resistance connected between each module output pin and a 28.0 vdc supply.

4.2.27.3 Same as PS 2003952.

4.3 WORKMANSHIP

4.3.1 Marginal Voltages and Thermal Extremes.

4.3.1.1 Low Marginal Voltage/Low Temperature. Same as PS 2003952.

4.3.1.2 Low Marginal Voltage/High Temperature. Same as PS 2003952.

4.3.1.3 High Marginal Voltage/High Temperature. Same as PS 2003952.

4.3.2 Vibration. Same as PS 2003952.

4.3.3 Weight. Same as PS 2003952.

5. PREPARATION FOR DELIVERY

5.1 GENERAL. Same as PS 2003952.

6. NOTES: Same as PS 2003952.

APOLLO G&N Specification
PS 2016009 Rev B
Original Issue Date: 6 JAN 67
Release Authority: TDRR 32575
Class A Release

PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

INDICATOR DRIVER MODULE

DRAWING NO. 2003952

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA
6 JAN 67	A	32575	Initial Release		—
6/13/67	B	33941	1, 8, 9	DMS FA	DMS FA

This specification consists of pages 1 to 14inclusive.

APPROVALS				
APPROVALS	NASA/MSC	Eldred Hall 11/18/66	W Stameris 8 Dec 1966 MIT/IL	10/11/66 10/11/66 RAY

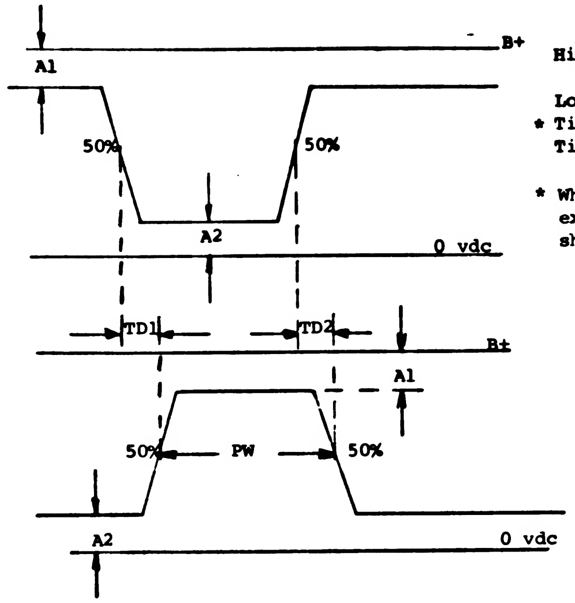

Figure 3-1B

High Level (A1)	NMT 1.5% of B+ below B+
Low Level (A2)	24%-30% of B+
* Time Delay (TD1)	65 ± 40 usec
Time Delay (TD2)	20 ± 15 usec

* When measured at high voltage extreme this characteristic shall be 45 $^{+45}_{-27}$ µsec.

Figure 3-1C

High Level (A1)	NMT 0.4V below B+
Low Level (A2)	NMT 0.1V
Pulse Width (PW)	15 ± 10 msec

Figure 3-1 Alarm Drivers Pulse Characteristics

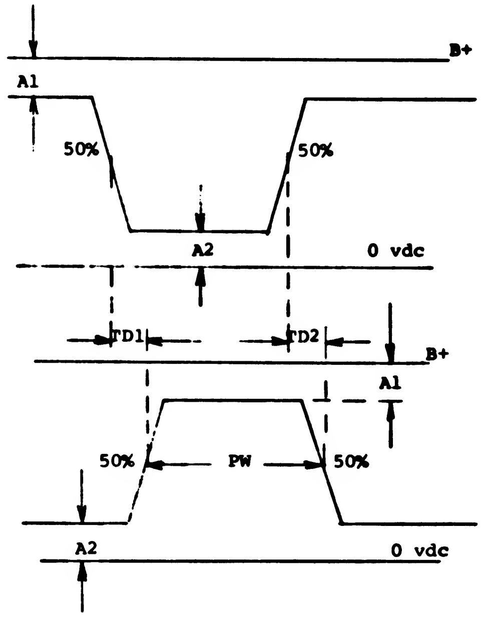

Figure 3-3A

High Level(A1)	NMT 1.5% of B+ below B+
Low Level(A2)	24%-30% of B+
*Time Delay(TD1)	65 ± 40 usec
Time Delay (TD2)	20 ± 15 usec

*When measured at high voltage extreme this characteristic shall be 45 $^{+45}_{-27}$ µsec.

Figure 3-3B

High Level(A1)	NMT 0.4V below B+
Low Level(A2)	NMT 10% of B+
Pulse Width (PW)	15 ± 10 msec

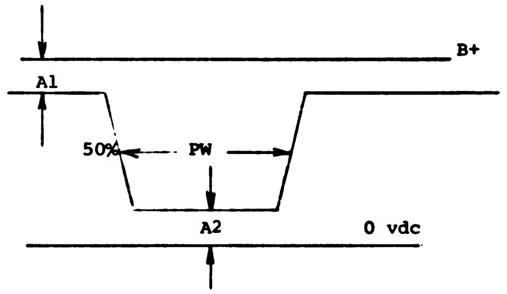

Figure 3-3C

High Level(A1)	NMT 0.4V below B+
Low Level(A2)	NMT 0.1 volt
Pulse Width(PW)	15 ± 10 msec

Figure 3-3 Y Line Drivers Output Pulse Characteristics

APOLLO G&N Specification
PS 2016009 Rev C
Original Issue Date: 6 JAN 67
Release Authority: TDRR 32575
Class A Release

PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

INDICATOR DRIVER MODULE

DRAWING NO. 2003952

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				MIT	NASA
6 JAN 67	A	32575	Initial Release		—
6/13/67	B	33941	1, 8, 9	sms FA	sms FA
7/13-67	C	34127	1, 2, 3	sms FA	sms FA

This specification consists of pages 1 to 14 inclusive.

APPROVALS	NASA/MSC	MIT/IL	RAY
		Eldred Hall 11/14/66 W Stameris 8 Dec 1966	C H McFadden 10/11/66 N.G. Parke 10/11/66 R C Davidson 10/11/66

APOLLO G&N Specification
PS 2016009 Rev C
Original Issue Date:
Release Authority: TDRR
Class A Release

ADDENDUM NOTICE

This Specification has been prepared as an Addendum to:

Specification No. PS 2003952

Revision D

FOR

INDICATOR DRIVER MODULE

Used With

APOLLO G&N System

The exact content of specification PS 2003952 used as the basic document for this addendum is the revision referenced above, and the exceptions stated below.

1. SCOPE

This specification establishes the detail requirements for complete identification and acceptance of the Indicator Driver Module, Part Number 2003952-031.

2. APPLICABLE DOCUMENTS. Same as PS 2003952. Rev. D

3. REQUIREMENTS

3.1 PERFORMANCE. Same as PS 2003952.

3.1.1 Thermal Conditioning. Same as PS 2003952.

3.1.2 Continuity. Same as PS 2003952.

3.1.3 Insulation Resistance. Same as PS 2003952.

3.1.4 Definition of Insulation Resistance - Pin Group A. Same as PS 2003952.

3.1.5 Insulation Resistance - Pin Group B. Same as PS 2003952.

3.1.6 Insulation Resistance - Pin Group C. Same as PS 2003952.

3.1.7 Insulation Resistance - Pin Group D. Same as PS 2003952.

3.1.7.1 Same as PS 2003952.

3.1.7.2 Same as PS 2003952.

3.1.7.3 Same as PS 2003952.

3.1.8 Insulation Resistance - Pin Group E. Same as PS 2003952.

3.1.8.1 Same as PS 2003952.

3.1.8.2 Same as PS 2003952.

3.1.8.3 Same as PS 2003952.

APOLLO G&N Specification
PS 2016009 Rev D
Original Issue Date: 6 JAN 67
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Class A Release

PROCUREMENT SPECIFICATION

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INDICATOR DRIVER MODULE

DRAWING NO. 2003952

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Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA
6 JAN 67	A	32575	Initial Release		—
6/13/67	B	33941	1, 8, 9	EMS FA	EMS FA
/13-67	C	34127	1, 2, 3	EMS FA	EMS FA
8-3-67	D	34283	1, 2, 3	FA	FA

This specification consists of pages 1 to 14 inclusive.

APPROVALS	NASA/MSC	Eldred Hall 11/18/66 W Stameris 8 Dec 1966 MIT/IL	10/11/66 10/11/66 RAY

APOLLO G&N Specification
PS 2016009 Rev D
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ADDENDUM NOTICE

This Specification has been prepared as an Addendum to:

Specification No. PS 2003952
Revision E

FOR

INDICATOR DRIVER MODULE

Used With

APOLLO G&N System

The exact content of specification PS 2003952 used as the basic document for this addendum is the revision referenced above, and the exceptions stated below.

1. SCOPE

This specification establishes the detail requirements for complete identification and acceptance of the Indicator Driver Module, Part Number 2003952-031.

2. APPLICABLE DOCUMENTS. Same as PS 2003952 Rev. E

3. REQUIREMENTS

3.1 PERFORMANCE. Same as PS 2003952.

3.1.1 Thermal Conditioning. Same as PS 2003952.

3.1.2 Continuity. Same as PS 2003952.

3.1.3 Insulation Resistance. Same as PS 2003952.

3.1.4 Definition of Insulation Resistance - Pin Group A. Same as PS 2003952.

3.1.5 Insulation Resistance - Pin Group B. Same as PS 2003952.

3.1.6 Insulation Resistance - Pin Group C. Same as PS 2003952.

3.1.7 Insulation Resistance - Pin Group D. Same as PS 2003952.

3.1.7.1 Same as PS 2003952.

3.1.7.2 Same as PS 2003952.

3.1.7.3 Same as PS 2003952.

3.1.8 Insulation Resistance - Pin Group E. Same as PS 2003952.

3.1.8.1 Same as PS 2003952.

3.1.8.2 Same as PS 2003952.

3.1.8.3 Same as PS 2003952.

APOLLO G&N Specification
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Ⓜ 9-20-67	E	34886	Complete Retype	E. Hall	A. Metzger

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APPROVALS	NASA/MSC	EC Hall 9/15/67 W Stameris 15 Sept 67 MIT/IL	Robert J Kerman 9-19-67 RAY

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Revision E

FOR

INDICATOR DRIVER MODULE

Used With

APOLLO G&N System

The exact content of specification PS 2003952 used as the basic document for this addendum is the revision referenced above, and the exceptions stated below.

APOLLO G&N Specification
PS 2016009 Rev F
Original Issue Date: 6 January 1967
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Class A Release

PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

INDICATOR DRIVER MODULE

DRAWING NO. 2003952

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA
10-20-67	E	34886	Complete Retype	E. Hall	A. Metzger
12-21-67	F	35335	1, 2	FD	FH

This specification consists of pages 1 to 13 inclusive

APPROVALS	NASA/MSC	EC Hall 9/15/67 W Stameris 15 Sept 67 MIT/IL	Robert J Kerman 9-19-67 RAY

APOLLO G&N Specification
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Original Issue Date:
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Class A Release

ADDENDUM NOTICE

This Specification has been prepared as an Addendum to:

Specification No. PS 2003952

Revision F

FOR

INDICATOR DRIVER MODULE

Used With

APOLLO G&N System

The exact content of specification PS 2003952 used as the basic document for this addendum is the revision referenced above, and the exceptions stated below.

APOLLO G&N Specification
PS 2016015 Rev A
Original Issue Date: 13 FEB 67
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PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

DISPLAY AND KEYBOARD ASSEMBLY

DRAWING NO. 2003994

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA
(M) 4-13-67	A	33603	1,13,14,15,16,17	EMS FK	EMS FK

This specification consists of pages 1 to 18 inclusive.

APPROVALS	NASA/MSC	EC Hall 1/30/67	WStameris 30 Jan 67		12-7-66
		MIT/IL			RAY

3.1.13.1 The Random vibration shall be Gaussian distributed with the exception that magnitude limiting shall occur at a peak to rms "g" ratio of 3 to 1.

Vibration in each of three mutually perpendicular axis shall be for 2 minutes as follows: 3DB/octave Rollup 10 HZ to $0.04g^2$/HZ at 70 HZ, $0.04g^2$/HZ to 420 HZ, 3DB/octave Rolloff from 420 HZ to 2000 HZ.

Tolerance limits between 10 HZ and 50 HZ shall be ± 3DB;
*Tolerance limits between 50 HZ and 1000 HZ shall be ± 1.5DB;
Tolerance limits between 1000 HZ and 2000 HZ shall be ± 3DB;

*In the event the ± 1.5 db from 50 to 1000 HZ cannot be met with existing facilities, the tolerance may be broadened to ± 3 db providing the overall g rms level is held to ± 10 percent.

3.1.14 Leak Rate. With the DSKY pressurized to 2 PSIG at 25 ± 2°C using a mixture of 90% nitrogen and 10% helium, the leak rate shall not exceed 1.0×10^{-3} cc/sec/atm.

3.1.15 Aging. The DSKY shall have accumulated not less than two hundred hours operating time prior to completion of test.

3.1.16 Spare and Not Connected Terminals. The following DSKY connector J9 pins are provided as spare and NC terminals.

Connector J9 Pin Numbers	Signal	Designation
75	W-210	SPARE
74	W-213	SPARE
73	W-241	SPARE
13	W-246	SPARE
34 (N)	SD326	SPARE
37 (N)	SD328	SPARE
56 ([illegible])	SD444	SPARE
34 (M)	SD445	SPARE

3.2 PRODUCT CONFIGURATION

3.2.1 Drawings. The configuration of the assembly shall be in accordance with Apollo G&N Drawing 2003994 and all drawings and engineering data referenced thereon.

3.2.2 Weight. The weight of each DSKY shall be measured and recorded.

4. QUALITY ASSURANCE PROVISIONS

4.1 GENERAL. The contractor responsible for the manufacture of the assembly shall be responsible for the accomplishment of each test required herein. See Table 4-1, Product Performance and Configuration Requirement/Quality Verification Cross Reference Index.

TABLE 4-1

Requirement	JDC	Requirement	JDC
3.1.1	05393	3.1.10	05388,05379, 05385,05376
3.1.2	05344,05345	3.1.11	05388,05379, 05385,05376
3.1.2.1	05394,05344, 05345,05351	3.1.12	05367,05388
3.1.2.2	05344,05345	3.1.13	05387
3.1.3	05379,05385	3.1.13.1	05387
3.1.4	05379,05385	3.1.14	05371
3.1.5	05382,05379, 05385	3.1.15	05366
3.1.6	05388,05379, 05385,05376	3.1.16	N.A.
3.1.7	05388,05379, 05385,05376	3.2.1	05364,05393
3.1.8	05388,05379, 05385,05376	3.2.2	05365
3.1.9	05388,05379, 05385,05376		

4.1.1 Test Conditions

4.1.1.1 Environmental. The assembly shall be tested under the following ambient conditions:

a. Temperature: 25° ± 10°C
b. Relative Humidity: 90% max
c. Barometric Pressure: 28 to 32 inches of Hg

4.1.2 Nonconforming Units. Failure of the unit to pass any examination or test of this specification shall automatically classify the unit as nonconforming. Each nonconforming unit corrected by the contractor shall be reinspected. Reinspection may be limited to the test or examination which defined the nonconformance, or, when directed by the cognizant inspector, a complete retest and re-examination may be required. Nonconforming units which have not been corrected will be considered for acceptance only upon formal application by the contractor to the cognizant NASA representative.

4.2 TESTS

4.2.1 Drawing Compliance. The assembly shall be visually examined for compliance to the requirements of APOLLO G&N Drawing 2003994. Particular attention shall be given to inspection for damage to surfaces, structure, and equipment, including contaminants, pin misalignment, and legibility and appearance of marking.

4.2.2 Acceptance Tests. All tests shall be performed using the JDC's listed herein in the order specified in the Assembly Test Plan (paragraph 4.2.2.1).

a. The Acceptance Tests must be performed with one (1) Computer and two (2) DSKY's. If any of the units are missing, Hangar Queen units shall be used during the tests. (*).
The Hangar Queen units shall not be subjected to mechanical inspection, vibration, thermal cycling, weight measurement, leak test or to the requirements of long term aging or Test Data JDC. A failure isolated to a Hangar Queen shall not be cause for rejection of the unit undergoing acceptance tests.

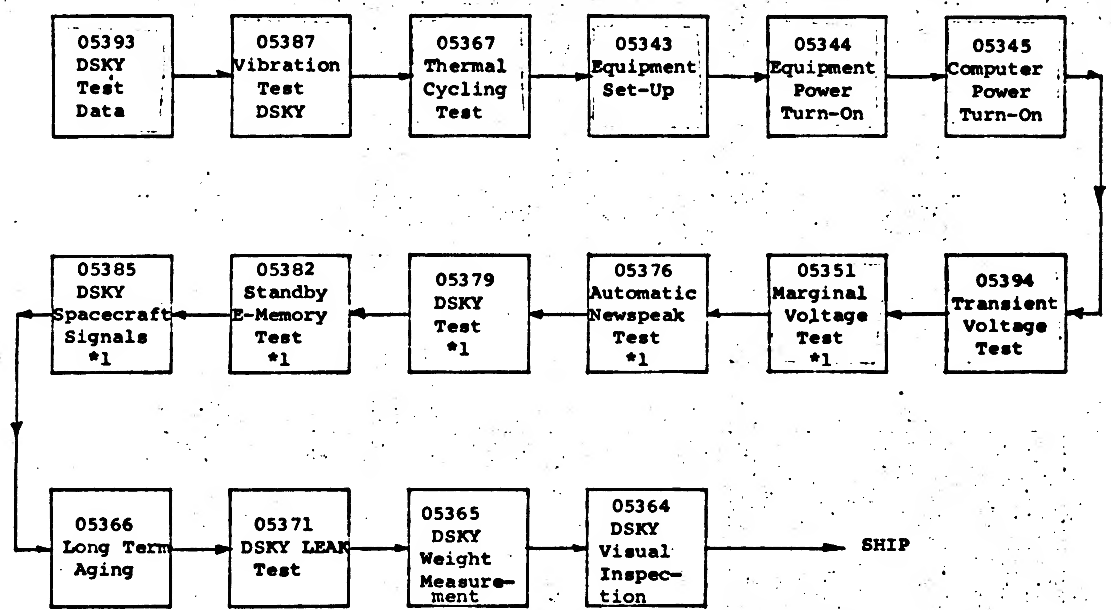
b. To perform the tests specified herein, Fixed Memory Modules containing Newspeak Program are required in the B1 and B2 positions and Warning Test Rope Assemblies are required in the B3, B4, B5 and B6 positions. These modules must meet the requirements for factory test equipment.

(*) Definition of Hangar Queen

A Hangar Queen Unit shall be defined as a Computer or DSKY which is capable of passing the following JDC's:

1.	05394	Transient Voltage Test
2.	05343	Equipment Setup
3.	05344	Equipment Power Turn On
4.	05345	Computer Power Turn On
5.	05351	Marginal Voltage Test
6.	05376	Automatic Newspeak Test
7.	05379	Dsky Test (Indicators & Keyboard)
8.	05382	Standby - E Memory Test
9.	05384	Priority of Interrupts
10.	05385	Dsky Spacecraft Signals
11.	05388	CTS Control of Newspeak

The equipment shall be tested in accordance with the above requirements during preliminary testing of the unit (s) which will be sold.



4.2.2.1 Assembly Test Plan

*1. The performance sequence of these JDC's is not critical, therefore they may be performed in any convenient order.

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PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

DISPLAY AND KEYBOARD ASSEMBLY

DRAWING NO. 2003994

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA
4-13-6	A	33693	1,13,14,15,16,17	DMS FK	DMS FK
[illegible]	B	33 33	1,12,13,14,15,16,17,18,19	DMS FK	DMS FK

This specification consists of pages 1 to 19 inclusive.

APPROVALS	NASA/MSC	EC Hall 1/30/67	W Stameris 20 Jan 67 MIT/IL		12-7-66 RAY	12-7-66

3.1.13.1 The Random vibration shall be Gaussian distributed with the exception that magnitude limiting shall occur at a peak to rms "g" ratio of 3 to 1.

Vibration in each of three mutually perpendicular axis shall be for 2 minutes as follows: 3DB/octave Rollup 10 HZ to $0.04g^2$/HZ at 70 HZ, $0.04g^2$/HZ to 420 HZ, 3DB/octave Rolloff from 420 HZ to 2000 HZ.

Tolerance limits between 10 HZ and 50 HZ shall be ± 3DB;
*Tolerance limits between 50 HZ and 1000 HZ shall be ± 1.5DB;
Tolerance limits between 1000 HZ and 2000 HZ shall be ± 3DB;

*In the event the ± 1.5 db from 50 to 1000 HZ cannot be met with existing facilities, the tolerance may be broadened to ± 3 db providing the overall g rms level is held to ± 10 percent.

3.1.14 Leak Rate. With the DSKY pressurized to 2 PSIG at 25 ± 2°C using a mixture of 90% nitrogen and 10% helium, the leak rate shall not exceed 1.0×10^{-3} cc/sec/atm.

3.1.15 Aging. The DSKY shall have accumulated not less than two hundred hours operating time prior to completion of test.

3.1.16 Spare and Not Connected Terminals. The following DSKY connector J9 pins are provided as spare and NC terminals.

Connector J9 Pin Numbers	Signal	Designation
75	W-210	SPARE
74	W-213	SPARE
73	W-241	SPARE
13	W-246	SPARE
34 (N)	SD326	SPARE
37 (N)	SD328	SPARE
56 (M)	SD444	SPARE
34 (M)	SD445	SPARE

3.2 PRODUCT CONFIGURATION

3.2.1 Drawings. The configuration of the assembly shall be in accordance with Apollo G&N Drawing 2003994 and all drawings and engineering data referenced thereon.

3.2.2 Weight. The weight of each DSKY shall be measured and recorded.

4. QUALITY ASSURANCE PROVISIONS

4.1 GENERAL. The contractor responsible for the manufacture of the assembly shall be responsible for the accomplishment of each test required herein. See Table 4-1, Product Performance and Configuration Requirement/Quality Verification Cross Reference Index.

TABLE 4-1

Requirement	JDC	Requirement	JDC
3.1.1	05393	3.1.10	05388,05379, 05385,05376
3.1.2	05344,05345	3.1.11	05388,05379, 05385,05376
3.1.2.1	05394,05344, 05345,05351	3.1.12	05367,05388
3.1.2.2	05344,05345	3.1.13	05387
3.1.3	05379,05385	3.1.13.1	05387
3.1.4	05379,05385	3.1.14	05371
3.1.5	05382,05379, 05385	3.1.15	05366
3.1.6	05388,05379, 05385,05376	3.1.16	N.A.
3.1.7	05388,05379, 05385,05376	3.2.1	05364,05393
3.1.8	05388,05379, 05385,05376	3.2.2	05365
3.1.9	05388,05379, 05385,05376		

4.2.2 Acceptance Tests. All tests shall be performed using the JDC's listed herein in the order specified in the Assembly Test Plan (paragraph 4.2.2.1).

a. The Acceptance Tests must be performed with one (1) Computer and two (2) DSKY's. If any of the units are missing, Hangar Queen units shall be used during the tests. (*).
The Hangar Queen units shall not be subjected to mechanical inspection, vibration, thermal cycling, weight measurement, leak test or to the requirements of long term aging or Test Data JDC. A failure isolated to a Hangar Queen shall not be cause for rejection of the unit undergoing acceptance tests.

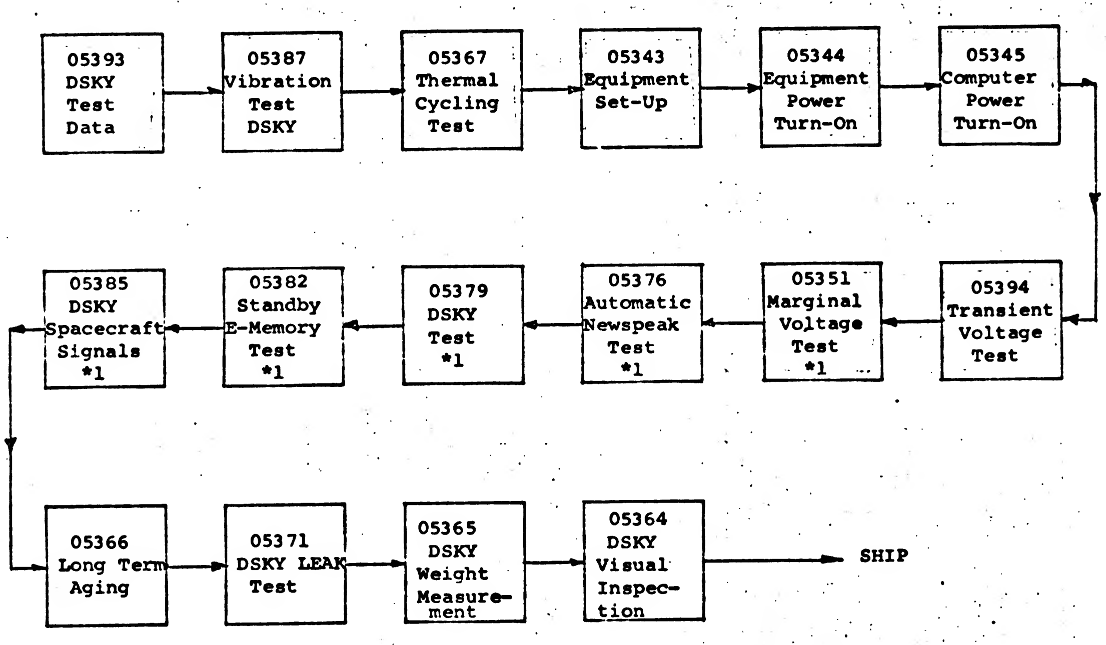
b. To perform the tests specified herein, Fixed Memory Modules containing Newspeak Program are required in the B1 and B2 positions and Warning Test Rope Assemblies are required in the B3, B4, B5 and B6 positions. These modules must meet the requirements for factory test equipment.

(*) Definition of Hangar Queen

A Hangar Queen Unit shall be defined as a Computer or DSKY which is capable of passing the following JDC's:

1.	05394	Transient Voltage Test
2.	05343	Equipment Setup
3.	05344	Equipment Power Turn On
4.	05345	Computer Power Turn On
5.	05351	Marginal Voltage Test
6.	05376	Automatic Newspeak Test
7.	05379	Dsky Test (Indicators & Keyboard)
8.	05382	Standby - E Memory Test
9.	05384	Priority of Interrupts
10.	05385	Dsky Spacecraft Signals
11.	05388	CTS Control of Newspeak

The equipment shall be tested in accordance with the above requirements during preliminary testing of the unit (s) which will be sold.


05393 DSKY Test Data
05387 Vibration Test DSKY
05367 Thermal Cycling Test
05343 Equipment Set-Up
05344 Equipment Power Turn-On
05345 Computer Power Turn-On
05394 Transient Voltage Test
05351 Marginal Voltage Test *1
05376 Automatic Newspeak Test *1
05379 DSKY Test *1
05382 Standby E-Memory Test *1
05385 DSKY Spacecraft Signals *1
05366 Long Term Aging
05371 DSKY LEAK Test
05365 DSKY Weight Measurement
05364 DSKY Visual Inspection
SHIP

4.2.2.1 Assembly Test Plan

*1. The performance sequence of these JDC's is not critical, therefore they may be performed in any convenient order.

4.2.2.2 List of JDC's:

05343	Equipment Set-Up
05344	Equipment Power Turn-On
05345	Computer Turn-On
05351	Marginal Voltage Test
05364	Dsky Visual Inspection
05365	Dsky Weight Measurement
05366	Long Term Aging
05367	Thermal Cycling Test
05371	Dsky Leak Test
05376	Automatic Newspeak Test
05379	Dsky Test (Indicators & Keyboard)
05382	Standby E Memory Test
05385	Dsky Space Craft Signals
05387	Vibration Test-Dsky
05388	CTS Control of Newspeak
05393	Dsky Test Data
05394	Transient Voltage Test

5. PREPARATION FOR DELIVERY

5.1 GENERAL. Preparation for delivery shall be in accordance with Specification ND 1002214. The DSKYs shall be pressurized for shipment at 2.0 ± 0.5 psig with dry nitrogen at ambient room temperature.

6. NOTES: None

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PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

DISPLAY AND KEYBOARD ASSEMBLY

DRAWING NO. 2003994

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals MIT	NASA
4-13-67	A	33693	1,13,14,15,16,17	DMS FG	DMS FG
-8-6	B	33933	1,12,13,14,15,16,17,18,19	DMS FG	DMS FG
-13-	C	34128	1, 4, 19	DMS FG	DMS FG

This specification consists of pages 1 to 19 inclusive.

APPROVALS	NASA/MSC	EC Hall 1/30/67	W Stameris 30 Jan 67 MIT/IL	R.P. [illegible] 12-7-66 W J [illegible] 12-7-66 BC [illegible] 12/7/66 RAY

3.1.2.2 AC Voltages. The AC voltage supplied to the assemblies shall be 75 VRMS at 400 ± 8 cps, single phase variable up to 115 ± 5 VRMS and capable of being turned off. This voltage is applied to the following DSKY connector pins as the designated signals.

NAV DSKY		MAIN DSKY	
Signal - Name	J9 Conn. Pin	Signal - Name	J9 Conn. Pin
W-343 115V 400 cps	38	W-437 115V 400 cps	38
W-344 115V 400 cps RET	40	W-438 115V 400 cps RET	40

3.1.2.3 The DSKY shall operate properly when tested with a Computer during the following marginal voltage conditions while running Newspeak Program:

	+4V	+14V	+28V
LOW	3.40 ± 0.01	12.10 ± 0.01	21.5 ± 0.1
HIGH	4.60 ± 0.01	16.40 ± 0.01	

3.1.3 Input Sync Pulse. An 800 ± 16 cps sync pulse shall be applied to the DSKY assemblies through the following connector pins.

	DSKY J9 Connector Pins	
Signal - Name	Main	Nav
CC212 ELSNCN	-	7
CC242 ELSNCM	7	-

3.1.4 Legend Brightness Control. The brightness of the legends (NOUN, VERB, PROGRAM, and the horizontal bars above each register) shall be variable from OFF to maximum brightness by input signals to the DSKY connectors as follows:

	DSKY J9 Connector Pins	
Signal - Name	Main	Nav
WD345 DIMMER	-	5
WD346 DIMMER RET.	-	4
RD442 DIMMER	5	-
WD443 DIMMER RET.	4	-

3.1.5 Keyboard. With all keys except "STBY" individually pressed, signals DE201 through DE205 from the NAV DSKY and signals DE253 through DE257 from the Main DSKY shall produce the codes specified in Table 3-1. With no keys except STBY depressed, signal D-206 from the NAV DSKY and signal D-209 from the Main DSKY shall be present. Keys RSET and STBY on each DSKY shall produce signals D-207 and D-208, respectively, when pressed.

3.1.6 Flashing Alarm Characters. With the flashing timing pulse, signals CB236 and CB244, applied to pins 46 and 72 of J9, respectively, the alarm indicators KEY REL and OPR ERR shall flash.

3.2 PRODUCT CONFIGURATION

3.2.1 Drawings. The configuration of the assembly shall be in accordance with Apollo G&N Drawing 2003994 and all drawings and engineering data referenced thereon.

3.2.2 Weight. The weight of each DSKY shall be measured and recorded.

4. QUALITY ASSURANCE PROVISIONS

4.1 GENERAL. The contractor responsible for the manufacture of the assembly shall be responsible for the accomplishment of each test required herein. See Table 4-1, Product Performance and Configuration Requirement/Quality Verification Cross Reference Index.

TABLE 4-1

Requirement	JDC	Requirement	JDC
3.1.1	05393,	3.1.10	05388,05379, 05385,05376
3.1.2	05344,05345	3.1.11	05388,05379, 05385,05376
3.1.2.1	05394,05344 05345	3.1.12	05367,05388
3.1.2.2	05344,05345	3.1.13	05387
3.1.2.3	05351		
3.1.3	05379,05385	3.1.13.1	05387
3.1.4	05379,05385	3.1.14	05371
3.1.5	05382,05379 05385	3.1.15	05366
3.1.6	05388,05379 05385,05376	3.1.16	N.A.
3.1.7	05388,05379 05385,05376	3.2.1	05364,05393
3.1.8	05388,05379 05385,05376	3.2.2	05365
3.1.9	05388,05379 05385,05376		

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PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

DISPLAY AND KEYBOARD ASSEMBLY

DRAWING NO. 2003994

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA
4-13-67	A	33693	1,13,14,15,16,17	DMS FK	DMS FK
-8-67	B	33933	1,12,13,14,15,16,17,18,19	DMS FK	DMS FK
-13-6	C	34128	1, 4, 15	DMS FK	DMS FK
9-12-67	D	34586	1, 14, 15, 18, 19	LB FK	LB FK

This specification consists of pages 1 to 19 inclusive.

APPROVALS	NASA/MSC	EC Hall 1/30/67 W Stameris 30 Jan 67 MIT/IL	12-7-66 RAY

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PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

DISPLAY AND KEYBOARD ASSEMBLY

DRAWING NO. 2003994

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA
4-13-67	A	33693	1,13,14,15,16,17	DMS FK	DMS FK
[illegible]-8-67	B	33933	1,12,13,14,15,16,17,18,19	DMS FK	DMS FK
[illegible]-13-[illegible]	C	34126	1, 4, 19	DMS FK	DMS FK
9-12-67	D	349[illegible]	1, 14, 15, 18, 19	[illegible] FK	[illegible] FK
11-16-67	E	35076	1, 2	FK	FK

This specification consists of pages 1 to 19 inclusive.

APPROVALS	NASA/MSC	EC Hall 1/30/67	WStameris 30 Jan 67 MIT/IL		12-7-66 RAY

APOLLO G&N Specification
PS 2016015 Rev -
Original Issue Date: 13 FEB 67
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Class A Release

PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

DISPLAY AND KEYBOARD ASSEMBLY

DRAWING NO. 2003994

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA

This specification consists of pages 1 to 17 inclusive.

APPROVALS	NASA/MSC	EC Hall 1/30/67 WStameris 30 Jan 67 MIT/IL	W J Flaherty 12-7-66 12-7-66 RAY

APOLLO G&N Specification
PS 2016015 Rev -
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PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

DISPLAY AND KEYBOARD ASSEMBLY

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				MIT	NASA

This specification consists of pages 1 to 17 inclusive.

APPROVALS	NASA/MSC	EC Hall 1/30/67 WStameris 30 Jan 67 MIT/IL	12-7-66 RAY

1. SCOPE

1.1 This specification establishes the detail requirements for complete identification and acceptance of the Display and Keyboard Assembly Part No. 2003994-011.

2. APPLICABLE DOCUMENTS

The following documents form a part of this specification to the extent specified herein.

2.1 Effective Issues. Unless otherwise specified herein, Military and Government Standards and Specifications shall be the issue in effect on the date of request for proposal or invitation to bid.

SPECIFICATIONS

APOLLO G&N

ND 1002214	General Specification for Preservation, Packaging, Packing and Container Marking of APOLLO Guidance and Navigation Major Assemblies, Assemblies, Subassemblies, Parts and Associated Ground Support Equipment.

APOLLO G&N

PS 2003994	Procurement Specification, Display and Keyboard Assembly

DRAWINGS

APOLLO G&N

2003994	DISPLAY AND KEYBOARD ASSEMBLY

(Copies of Specifications, Standards, Drawings, Bulletins and Publications required by suppliers in connection with specific procurement functions should be obtained from the Procuring Activity or as directed by the Contracting Officer).

3.1.2.2 AC Voltages. The AC voltage supplied to the assemblies shall be 75 VRMS at 400 ± 8 cps, single phase variable up to 115 ± 5 VRMS and capable of being turned off. This voltage is applied to the following DSKY connector pins as the designated signals.

NAV DSKY		MAIN DSKY	
Signal - Name	J9 Conn. Pin	Signal - Name	J9 Conn. Pin
W-343 115V 400 cps	38	W-437 115V 400 cps	38
W-344 115V 400 cps RET	40	W-438 115V 400 cps RET	40

3.1.3 Input Sync Pulse. An 800 ± 16 cps sync pulse shall be applied to the DSKY assemblies through the following connector pins.

Signal - Name		DSKY J9 Connector Pins	
		Main	Nav
CC212	ELSNCN	-	7
CC242	ELSNCM	7	-

3.1.4 Legend Brightness Control. The brightness of the legends (NOUN, VERB, PROGRAM, and the horizontal bars above each register) shall be variable from OFF to maximum brightness by input signals to the DSKY connectors as follows:

Signal - Name		DSKY J9 Connector Pins	
		Main	Nav
WD345	DIMMER	-	5
WD346	DIMMER RET.	-	4
RD442	DIMMER	5	-
WD443	DIMMER RET.	4	-

3.1.5 Keyboard. With all keys except "STBY" individually pressed, signals DE201 through DE205 from the NAV DSKY and signals DE253 through DE257 from the Main DSKY shall produce the codes specified in Table 3-1. With no keys except STBY depressed, signal D-206 from the NAV DSKY and signal D-209 from the Main DSKY shall be present. Keys RSET and STBY on each DSKY shall produce signals D-207 and D-208, respectively, when pressed.

3.1.6 Flashing Alarm Characters. With the flashing timing pulse, signals CB236 and CB244, applied to pins 46 and 72 of J9, respectively, the alarm indicators KEY REL and OPR ERR shall flash.

3.1.7 Flashing Noun Characters. With the Flasher Timing Pulse, signal CB238 applied to pin 70 of J9 and the Noun numerical characters programmed for 8's (ref. Tables 3-2 and 3-3), the numerical characters shall flash.

3.1.8 Flashing Verb Characters. With the Flasher Timing Pulse, signal CB238, applied to pin 70 of J9 and the Verb numerical characters programmed for 8's (ref. Tables 3-2 and 3-3), the numerical characters shall flash.

3.1.9 Numerical Electroluminescent Indicators. With the appropriate RLYWD and RLYBT combinations of logic "ones" and "zeros" applied as specified in Tables 3-2 and 3-3, the corresponding Noun, VERB, and Program legend numerical characters and the numerical characters of all registers shall be displayed.

3.1.10 Isolated Relay Indicators. When the codes specified in Table 3-4 are present, the corresponding isolated relay indicator shall be illuminated. Contact closure shall exist between pins of J9 as specified in Table 3-4.

3.1.11 Status and Caution Indicators. With the signal applied to an input pin of J9 as specified in Table 3-5 the corresponding status or caution indicator shall be illuminated. Contact closure shall exist between pins of J9 as specified in Table 3-5.

TABLE 3-1 KEY CODES

OUTPUT PINS

KEY	DE257 DE205	DE256 DE204	DE255 DE203	DE254 DE202	DE253 DE201	D-206 D-209	D-208 D-208	D-207 D-207	MAIN SIGNALS NAV SIGNALS
KEY REL	1	1	0	0	1	0	0	0	
VERB	1	0	0	0	1	0	0	0	
NOUN	1	1	1	1	1	0	0	0	
ENTR	1	1	1	0	0	0	0	0	
CLR	1	1	1	1	0	0	0	0	
+	1	1	0	1	0	0	0	0	
-	1	1	0	1	1	0	0	0	
0	1	0	0	0	0	0	0	0	
1	0	0	0	0	1	0	0	0	
2	0	0	0	1	0	0	0	0	
3	0	0	0	1	1	0	0	0	
4	0	0	1	0	0	0	0	0	
5	0	0	1	0	1	0	0	0	
6	0	0	1	1	0	0	0	0	
7	0	0	1	1	1	0	0	0	
8	0	1	0	0	0	0	0	0	
9	0	1	0	0	1	0	0	0	
RSET	1	0	0	1	0	0	1	0	
STBY	0	0	0	0	0	1	0	1	

TABLE 3-1 KEY CODES

OUTPUT PINS

KEY	DE257	DE256	DE255	DE254	DE253	D-206	D-208	D-207	MAIN SIGNALS
	DE205	DE204	DE203	DE202	DE201	D-209	D-208	D-207	NAV SIGNALS
KEY REL	1	1	0	0	1	0	0	0	
VERB	1	0	0	0	1	0	0	0	
NOUN	1	1	1	1	1	0	0	0	
ENTR	1	1	1	0	0	0	0	0	
CLR	1	1	1	1	0	0	0	0	
+	1	1	0	1	0	0	0	0	
-	1	1	0	1	1	0	0	0	
0	1	0	0	0	0	0	0	0	
1	0	0	0	0	1	0	0	0	
2	0	0	0	1	0	0	0	0	
3	0	0	0	1	1	0	0	0	
4	0	0	1	0	0	0	0	0	
5	0	0	1	0	1	0	0	0	
6	0	0	1	1	0	0	0	0	
7	0	0	1	1	1	0	0	0	
8	0	1	0	0	0	0	0	0	
9	0	1	0	0	1	0	0	0	
RSET	1	0	0	1	0	0	1	0	
STBY	0	0	0	0	0	1	0	1	

TABLE 3-2 FLASHING CHARACTERS

SIGNAL J9 CONN. PIN	CE228 68	CE227 43	CE226 24	CE225 11	CE224 12	CHARACTER 2 10 9 8 7 6	CHARACTER 1 5 4 3 2 1
	1	0	1	1		PROGRAM CHAR 2	PROGRAM CHAR 1
	1	0	1	0		VERB CHAR 2	VERB CHAR 1
	1	0	0	1		NOUN CHAR 2	NOUN CHAR 1
	1	0	0	0			Reg 1 CHAR 5
	0	1	1	1	R1 (+)	Reg 1 CHAR 4	Reg 1 CHAR 3
	0	1	1	0	R1 (-)	Reg 1 CHAR 2	Reg 1 CHAR 1
	0	1	0	1	R2 (+)	Reg 2 CHAR 5	Reg 2 CHAR 4
	0	1	0	0	R2 (-)	Reg 2 CHAR 3	Reg 2 CHAR 2
	0	0	1	1		Reg 2 CHAR 1	Reg 3 CHAR 5
	0	0	1	0	R3 (+)	Reg 3 CHAR 4	Reg 3 CHAR 3
	0	0	0	1	R3 (-)	Reg 3 CHAR 2	Reg 3 CHAR 1

TABLE 3-3 FLASHING CHARACTERS

NUMERICAL DISPLAYS	CE223	CE222	CE221	CE220	CE219	CE218	CE217	CE216	CE215	CE214	SIGNALS
	67	42	23	10	3	66	41	22	9	2	J9 PIN NUMBER
	10	9	8	7	6	5	4	3	2	1	CHARACTER BITS
BLANK											
0	0	0	0	0	0	0	0	0	0	0	
1	1	0	1	0	1	1	0	1	0	1	
2	0	0	0	1	1	0	0	0	1	1	
3	1	1	0	1	1	1	1	0	1	1	
4	0	1	1	1	1	0	1	1	1	1	
5	1	1	1	1	0	1	1	1	1	0	
6	1	1	1	0	0	1	1	1	0	0	
7	1	0	0	1	1	1	0	0	1	1	
8	1	1	1	0	1	1	1	1	0	1	
9	1	1	1	1	1	1	1	1	1	1	

TABLE 3-4 ISOLATED RELAY INDICATORS

SIGNAL	CE228	CE227	CE226	CE225	CE222	CE221	CE220	CE219	CE218	CE217	INDICATOR ILLUMINATED	CONTACT CLOSURE BETWEEN PINS
J9 PIN NUMBER	68	43	24	11	42	23	10	3	66	41		
	1	1	0	0	1	x	x	x	x	x	PROG	57 and 31
	1	1	0	0	x	1	x	x	x	x	TRACKER	57 and 31
	1	1	0	0	x	x	x	1	x	x	GIMBAL BLOCK	57 and 31
	1	1	0	0	x	x	x	x	x	1	NO ATT	
	1	1	0	0	x	x	1	x	x	x		17 and 34
	1	1	0	0	x	x	0	x	x	x		6 and 34
	1	1	0	0	x	x	x	x	1	x		33 and 56
	1	1	0	0	x	x	x	x	0	x		16 and 56

x indicates don't care.

TABLE 3-5 STATUS AND CAUTION INDICATORS

Signal Input	Logic Input	J9 Input Pin	Indicator Illuminated	Contact Closure Between J9 Pins	Signal - Name Main	Signal - Name Nav
CB235	1	47	UPLINK ACTY		UPLACT	UPLACT
CB231	1	25	STBY	58 and 35	STANBY	STANBY
	0	25		59 and 35		
CB258	1	71	TEMP	57 and 31	SD440 G&N Caution	SD352A G&N Caution
CB232	1	44	RESTART	57 and 31		
	0			31 and 53	SD440C RESTART	SD352C RESTART
CB230	1	26	COMPACTY		COMACT	COMACT
CB233	1	69		37 and 61	SD407	SD338
	0			19 and 37	INJ SEQU START	INJ SEQU START
CB236	1	46	KEY REL		KYRLS	KYRLS
CB244	1	72	OPR ERR		OPEROR	OPEROR
CB234	1	18		36 and 60	SD409 CUTOFF	SD340 CUTOFF
	0			36 and 85		
CB237	1	45		55 and 84	SD441 CIRCUIT	SD342 CIRCUIT
				15 and 32	SD451A CIRCUIT	SD3250 CIRCUIT
	0			57 and 84	SD441 CIRCUIT	SD342 CIRCUIT
				14 and 32	SD451C CIRCUIT	WD325C CIRCUIT

TABLE 3-5 STATUS AND CAUTION INDICATORS (Cont'd)

Signal Input	Logic Input	J9 Input Pin	Indicator Illuminated	Contact Closure Between J9 Pins	Signal - Name	
					Main	Nav
CB229	1	27		80 and 81	SD452A ISS WARNING	SD324A ISS WARNING
				57 and 83	SD439A ISS WARNING	SD351 ISS WARNING
	0			54 and 83	WD439C ISS WARNING	SD351 ISS WARNING
				82 and 81	WD452 ISS WARNING	SD324C ISS WARNING

Pin 57 of connector J9 is common for SD signals 342, 351, 352, and 439 thru 441.

3.1.12 **Thermal Cycle Extremes.** The DSKY shall be subjected to the thermal cycle specified below. The AGC shall be exercised using a rope program during the thermal cycle. The DSKY shall be pressurized at 2.0 ± 0.2 psig at $25^{\circ}C \pm 3^{\circ}C$.

a. Set ambient temperature to $0^{\circ}C \, ^{+0C^{\circ}}_{-2.8C^{\circ}}$ for 8 ± 1 hours (power OFF and computer installed on coldplate).

b. Increase the ambient temperature to $65^{\circ}C \, ^{+2.8C^{\circ}}_{-0C^{\circ}}$ in not less than 40 minutes. This temperature shall be maintained for 3 hours.

c. Decrease the ambient temperature to $0^{\circ}C \, ^{+0C^{\circ}}_{-2.8C^{\circ}}$ in not less than 40 minutes. This temperature shall be maintained for 1.5 hours.

d. Increase the ambient temperature to $65^{\circ}C \, ^{+2.8C^{\circ}}_{-0C^{\circ}}$ in not less than 40 minutes. This temperature shall be maintained for 1.5 hours.

e. Decrease the ambient temperature to $0^{\circ}C \, ^{+0C^{\circ}}_{-2.8C^{\circ}}$ in not less than 40 minutes. This temperature shall be maintained for 1.5 hours.

f. Increase the ambient temperature to $65^{\circ}C \, ^{+2.8C^{\circ}}_{-0C^{\circ}}$ in not less than 40 minutes. This temperature shall be maintained for 1.5 hours.

g. Decrease the ambient temperature to room ambient (approxi. $25^{\circ}C$) in not less than 20 minutes.

3.1.13 **Vibration.** The DSKY shall be exercised using a rope program while subjected to the random vibration limits specified below:

3.1.12 Thermal Cycle Extremes. The DSKY shall be subjected to the thermal cycle specified below. The AGC shall be exercised using a rope program during the thermal cycle. The DSKY shall be pressurized at 2.0 ± 0.2 psig at $25^{\circ}C \pm 3^{\circ}C$.

a. Set ambient temperature to $0^{\circ}C\ {}^{+0C^{\circ}}_{-2.8C^{\circ}}$ for 8 ± 1 hours (power OFF and computer installed on coldplate).

b. Increase the ambient temperature to $65^{\circ}C\ {}^{+2.8C^{\circ}}_{-0C^{\circ}}$ in not less than 40 minutes. This temperature shall be maintained for 3 hours.

c. Decrease the ambient temperature to $0^{\circ}C\ {}^{+0C^{\circ}}_{-2.8C^{\circ}}$ in not less than 40 minutes. This temperature shall be maintained for 1.5 hours.

d. Increase the ambient temperature to $65^{\circ}C\ {}^{+2.8C^{\circ}}_{-0C^{\circ}}$ in not less than 40 minutes. This temperature shall be maintained for 1.5 hours.

e. Decrease the ambient temperature to $0^{\circ}C\ {}^{+0C^{\circ}}_{-2.8C^{\circ}}$ in not less than 40 minutes. This temperature shall be maintained for 1.5 hours.

f. Increase the ambient temperature to $65^{\circ}C\ {}^{+2.8C^{\circ}}_{-0C^{\circ}}$ in not less than 40 minutes. This temperature shall be maintained for 1.5 hours.

g. Decrease the ambient temperature to room ambient (approxi. $25^{\circ}C$) in not less than 20 minutes.

3.1.13 Vibration. The DSKY shall be exercised using a rope program while subjected to the random vibration limits specified below:

3.1.13.1 The Random vibration shall be Gaussian distributed with the exception that magnitude limiting shall occur at a peak to rms "g" ratio of 3 to 1.

Vibration in each of three mutually perpendicular axis shall be for 2 minutes as follows: 3DB/octave Rollup 10 HZ to $0.04g^2$/HZ at 70 HZ, $0.04g^2$/HZ to 420 HZ, 3DB/octave Rolloff from 420 HZ to 2000 HZ.

Tolerance limits between 10 HZ and 50 HZ shall be ± 3DB;
*Tolerance limits between 50 HZ and 1000 HZ shall be ± 1.5DB;
Tolerance limits between 1000 HZ and 2000 HZ shall be ± 3DB;

*In the event the ± 1.5 db from 50 to 1000 HZ cannot be met with existing facilities, the tolerance may be broadened to ± 3 db providing the overall g rms level is held to ± 10 percent.

3.1.14 Leak Rate. With each DSKY pressurized to 30.0 ± 1.0 psia with dry nitrogen at 25°C ± 2C°, the leak rate shall not exceed 1.0 psia for a period of 24.0 ± 0.5 hours.

3.1.15 Aging. The DSKY shall have accumulated not less than two hundred hours operating time prior to completion of test.

3.1.16 Spare and Not Connected Terminals. The following DSKY connector J9 pins are provided as spare and NC terminals.

Connector J9 Pin Numbers	Signal	Designation
75	W-210	SPARE
74	W-213	SPARE
73	W-241	SPARE
13	W-246	SPARE
34 (N)	SD326	SPARE
37 (N)	SD328	SPARE
56 (M)	SD444	SPARE
34 (M)	SD445	SPARE

3.1.13.1 The Random vibration shall be Gaussian distributed with the exception that magnitude limiting shall occur at a peak to rms "g" ratio of 3 to 1.

Vibration in each of three mutually perpendicular axis shall be for 2 minutes as follows: 3DB/octave Rollup 10 HZ to $0.04g^2$/HZ at 70 HZ, $0.04g^2$/HZ to 420 HZ, 3DB/octave Rolloff from 420 HZ to 2000 HZ.

Tolerance limits between 10 HZ and 50 HZ shall be ± 3DB;
*Tolerance limits between 50 HZ and 1000 HZ shall be ± 1.5DB;
Tolerance limits between 1000 HZ and 2000 HZ shall be ± 3DB;

*In the event the ± 1.5 db from 50 to 1000 HZ cannot be met with existing facilities, the tolerance may be broadened to ± 3 db providing the overall g rms level is held to ± 10 percent.

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34 (N)	SD326	SPARE
37 (N)	SD328	SPARE
56 (M)	SD444	SPARE
34 (M)	SD445	SPARE

3.2 PRODUCT CONFIGURATION

3.2.1 Drawings. The configuration of the assembly shall be in accordance with Apollo G&N Drawing 2003994 and all drawings and engineering data referenced thereon.

3.2.2 Weight. The weight of each DSKY shall be measured and recorded.

4. QUALITY ASSURANCE PROVISIONS

4.1 GENERAL. The contractor responsible for the manufacture of the assembly shall be responsible for the accomplishment of each test required herein. See Table 4-1, Product Performance and Configuration Requirement/Quality Verification Cross Reference Index.

TABLE 4-1

Requirement -	JDC	Requirement -	JDC
3.1.1	05438		
3.1.2	05422,05423	3.1.10	05433,05435
3.1.2.1	05422,05423	3.1.11	05433,05435
3.1.2.2	05422,05423	3.1.12	05430
3.1.3	05433,05435	3.1.13	05436
3.1.4	05433,05435	3.1.13.1	05436
3.1.5	05433,05435	3.1.14	05431
3.1 6	05433,05435	3.1.15	05429
3.1.7	05433,05435	3.1.16	N.A.
3.1.8	05433,05435	3.2.1	05426,05438
3.1.9	05433,05435	3.2.2	05428

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3.1.2	05422,05423	3.1.10	05433,05435
3.1.2.1	05422,05423	3.1.11	05433,05435
3.1.2.2	05422,05423	3.1.12	05430
3.1.3	05433,05435	3.1.13	05436
3.1.4	05433,05435	3.1.13.1	05436
3.1.5	05433,05435	3.1.14	05431
3.1 6	05433,05435	3.1.15	05429
3.1.7	05433,05435	3.1.16	N.A.
3.1.8	05433,05435	3.2.1	05426,05438
3.1.9	05433,05435	3.2.2	05428

4.1.1 Test Conditions

4.1.1.1 Environmental. The assembly shall be tested under the following ambient conditions:

a.	Temperature:	25° ± 10°C
b.	Relative Humidity:	90% max
c.	Barometric Pressure:	28 to 32 inches of Hg

4.1.2 Nonconforming Units. Failure of the unit to pass any examination or test of this specification shall automatically classify the unit as nonconforming. Each nonconforming unit corrected by the contractor shall be reinspected. Reinspection may be limited to the test or examination which defined the nonconformance, or, when directed by the cognizant inspector, a complete retest and re-examination may be required. Nonconforming units which have not been corrected will be considered for acceptance only upon formal application by the contractor to the cognizant NASA representative.

4.2 TESTS

4.2.1 Drawing Compliance. The assembly shall be visually examined for compliance to the requirements of APOLLO G&N Drawing 2003994. Particular attention shall be given to inspection for damage to surfaces, structure, and equipment, including contaminants, pin misalignment, and legibility and appearance of marking.

4.2.2 Acceptance Tests. All tests shall be performed using the JDC's listed herein in the order specified in the Assembly Test Plan as follows:

4.1.1 **Test Conditions**

4.1.1.1 Environmental. The assembly shall be tested under the following ambient conditions:

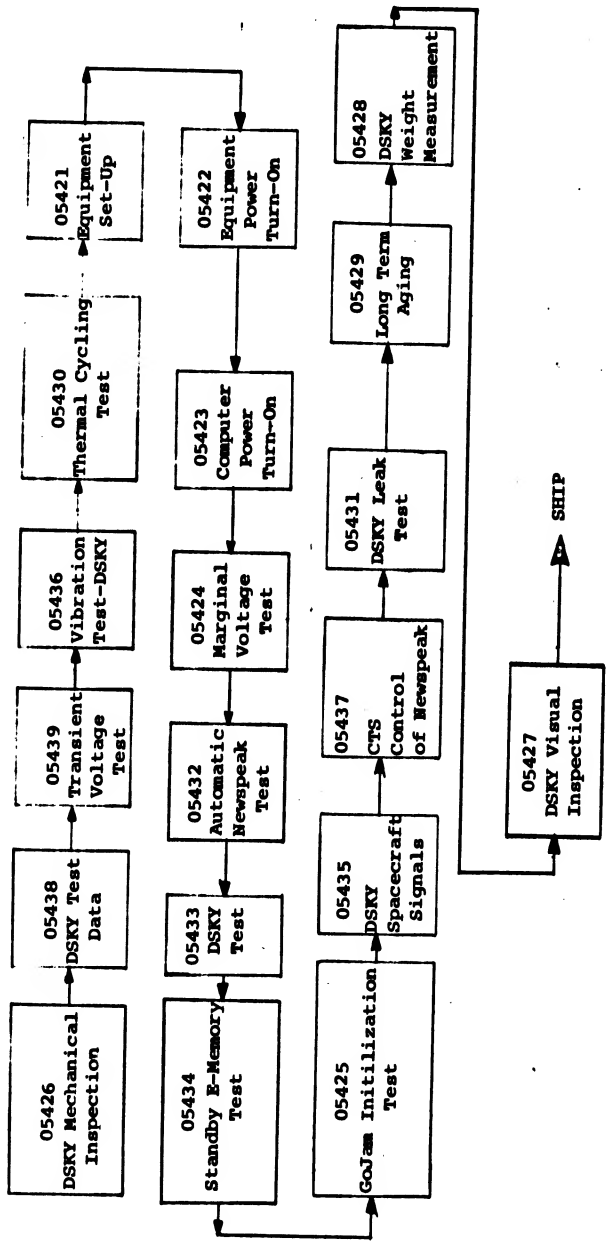
a. Temperature: $25^{\circ} \pm 10^{\circ}C$
b. Relative Humidity: 90% max
c. Barometric Pressure: 28 to 32 inches of Hg

4.1.2 **Nonconforming Units**. Failure of the unit to pass any examination or test of this specification shall automatically classify the unit as nonconforming. Each nonconforming unit corrected by the contractor shall be reinspected. Reinspection may be limited to the test or examination which defined the nonconformance, or, when directed by the cognizant inspector, a complete retest and re-examination may be required. Nonconforming units which have not been corrected will be considered for acceptance only upon formal application by the contractor to the cognizant NASA representative.

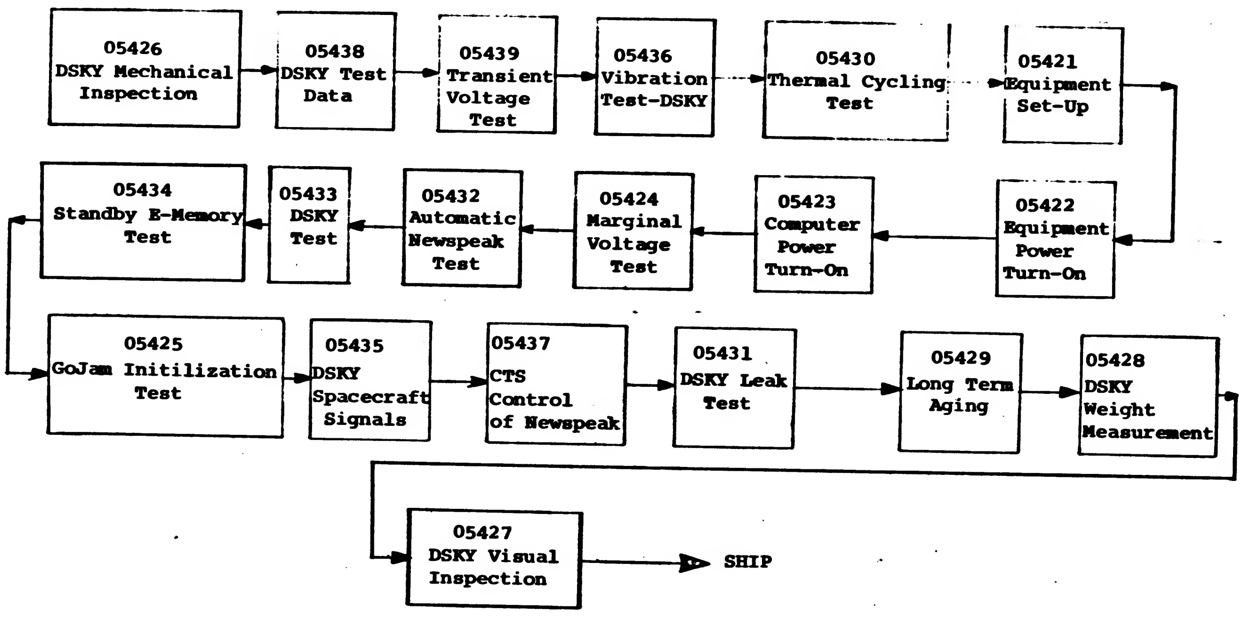
4.2 TESTS

4.2.1 **Drawing Compliance**. The assembly shall be visually examined for compliance to the requirements of APOLLO G&N Drawing 2003994. Particular attention shall be given to inspection for damage to surfaces, structure, and equipment, including contaminants, pin misalignment, and legibility and appearance of marking.

4.2.2 Acceptance Tests. All tests shall be performed using the JDC's listed herein in the order specified in the Assembly Test Plan as follows:


05426 DSKY Mechanical Inspection
05438 DSKY Test Data
05439 Transient Voltage Test
05436 Vibration Test-DSKY
05430 Thermal Cycling Test
05421 Equipment Set-Up
05422 Equipment Power Turn-On
05423 Computer Power Turn-On
05424 Marginal Voltage Test
05432 Automatic Newspeak Test
05433 DSKY Test
05434 Standby E-Memory Test
05425 GoJam Initilization Test
05435 DSKY Spacecraft Signals
05437 CTS Control of Newspeak
05431 DSKY Leak Test
05429 Long Term Aging
05428 DSKY Weight Measurement
05427 DSKY Visual Inspection
SHIP

4.2.2.1 Assembly Test Plan.



4.2.2.1 Assembly Test Plan.

4.2.2.2 List of JDC's:

05421	Equipment Set-Up
05422	Equipment Power Turn-On
05423	Computer Power Turn-On
05424	Marginal Voltage Test
05425	GoJam Initilization Test
05426	DSKY Mechanical Inspection
05427	DSKY Visual Inspection
05428	DSKY Weight Measurement
05429	Long Term Aging
05430	Thermal Cycling Test
05431	DSKY Leak Test
05432	Automatic Newspeak Test
05433	DSKY Test (Indicators & Keyboard)
05434	Standby E-Memory Test
05435	DSKY Space Craft Signals
05436	Vibration Test-DSKY
05437	CTS Control of Newspeak
05438	DSKY Test Data
05439	Transient Voltage Test

5. PREPARATION FOR DELIVERY

5.1 GENERAL. Preparation for delivery shall be in accordance with Specification ND 1002214. The DSKYs shall be pressurized for shipment at 2.0 ± 0.5 psig with dry nitrogen at ambient room temperature.

6. NOTES: None.

APOLLO G&N Specification
PS 2016016 Rev -
Original Issue Date: 11 MAR 68
Release Authority: TDRR 35869
Class A Release

PROCUREMENT SPECIFICATION
PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS
FIXED MEMORY MODULE B1-B6 ASSEMBLY
DRAWING NO. 2003972

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA

This specification consists of pages 1 to 21 inclusive.

APPROVALS	NASA/MSC	EC Hall 3/6/68 W Stameris 6 mar 68 MIT/IL	CCB 3/11/68	F. Goddard 2-23-68 RAY

3.1.9 **Sense Outputs.** With the input and timing waveforms as specified in paragraph 4.2.9, the sense outputs shall be as specified in Figure 3 and as follows:

3.1.9.1 The maximum ouput on MFT and sense lines, parity through sign shall be as follows:

V_p & V_M NMT 350 mv at 25°C

The minimum output on the MFT shall be as follows:

V_p & V_M NLT 145 mv at 25°C

V_p & V_M NLT 175 mv at -10°C

V_p & V_M NLT 120 mv at 70°C

The minimum V_1 output on sense lines -10°C = 50 MV, +25°C = 45MV
+70°C = 45MV.

Test Sequence:

A. Ambient Electrical Test Number One
B. Thermal Conditioning per 3.1.1.
C. Vibration per 3.1.11
D. Thermal Extremes Electrical Test per 3.1.10
E. Continuity and Isolation Tests per 3.1.5 and 3.1.3
E. Ambient Temperature Test Number Two.

The MFT V_p minimum and V_M minimum shall not change by more than ± 25 mv from Ambient Test Number One to Ambient Test Number Two.

3.1.9.2 Sense line zero noise (V_0 measured between 1.1 $^{+0.03}_{-0.05}$ µsec and 2.3 $^{+0.05}_{-0.05}$ µsec after the start of Logic Reset (FR) shall be NMT 25 mv. See Figure 3.

3.1.9.3 An all zero output shall occur when Logic STAGAT is zero. V_0 max = NMT 5 mv, 1.1 to 2.3 µsec after RSET.

TABLE IV

Requirements	Verification
3.1.1	4.2.2
3.1.2	4.2.3
3.1.3	4.2.4
3.1.4	4.2.5
3.1.5.1	4.2.6.1
3.1.5.2	4.2.6.2
3.1.5.3	4.2.6.3
3.1.7	4.2.7
3.1.8	4.2.8
3.1.9.1	4.2.9.1
3.1.9.2	4.2.9.2
3.1.9.3	4.2.9.3
3.1.9.4	4.2.9.4
3.1.10.1	4.3.1.1
3.1.10.2	4.3.1.2
3.1.11	4.3.2
3.2.1	4.2.1
3.2.2	4.2.10

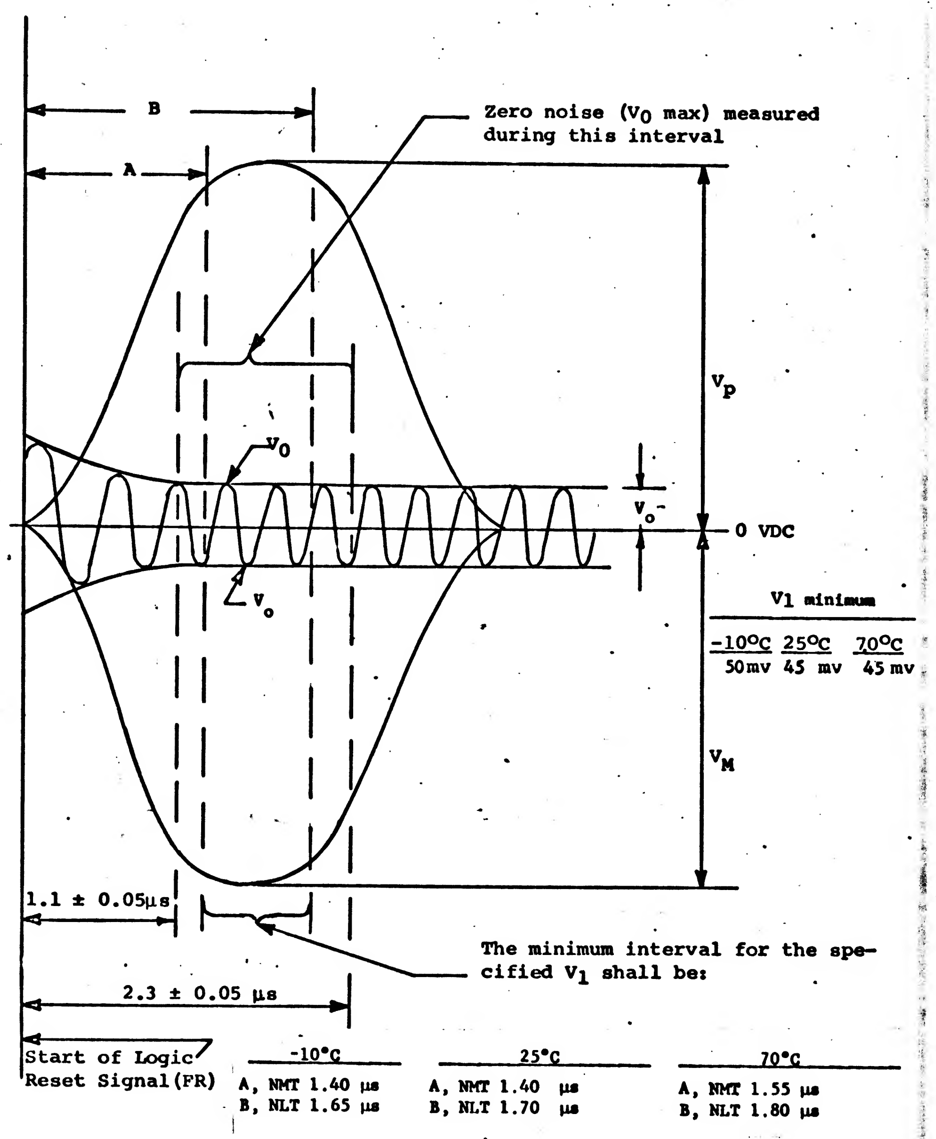
4.1.1 Test Conditions

4.1.1.1 **Evironmental.** Unless otherwise specified, the assemblies shall be tested under the following ambient conditions:

a.	Temperature	25°C ± 10C°
b.	Relative Humidity	90% max
c.	Barometric Pressure	28 to 32 inches of Hg.

4.1.2 **Nonconforming Units.** Failure of the unit to pass any examination or test of this specification shall automatically classfy the unit as nonconforming. Each nonconforming unit corrected by the contractor shall be reinspected. Reinspection may be limited to the test or examination which defined the nonconformance, or, when directed by the cognizant inspector, a complete retest and reexamination may be required. Nonconforming units which have not been corrected will be considered for acceptance only upon formal application by the contractor to the cognizant NASA representative.

4.1.3 **Input Voltage.** Input voltage, when required, shall be as specified in Paragraph 3.1.3.


B
A
Zero noise (V0 max) measured during this interval
V0
Vo
Vo⁻
VP
0 VDC
VM
1.1 ± 0.05µs
2.3 ± 0.05 µs
Start of Logic Reset Signal(FR)
The minimum interval for the specified V1 shall be:

V1 minimum

-10°C	25°C	70°C
50mv	45 mv	45 mv

The minimum interval for the specified V_1 shall be:

-10°C	25°C	70°C
A, NMT 1.40 µs	A, NMT 1.40 µs	A, NMT 1.55 µs
B, NLT 1.65 µs	B, NLT 1.70 µs	B, NLT 1.80 µs

FIGURE 3 ROPE OUTPUT WAVEFORM CHARACTERISTICS

APOLLO G&N Specification
PS 2016017 Rev A
Original Issue Date: 18 MAY 1967
Release Authority: TDRR 33806
Class A Release

PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENT

FIXED MEMORY SENSE AMPLIFIER MODULE B14

DRAWING NO. 2003981

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA
[illegible]	[illegible]	3[illegible]13	1,3,4,5	[illegible]	[illegible]

This specification consists of pages 1 to 5 inclusive.

APPROVALS	NASA/MSC	EC Hall ~~3/3/67~~ 4/7/67	MIT/IL 4/7/67	ICCB 5/18/67	RAY

3.1.7.2 With the input voltage adjusted to 16.5 ± 0.1 VDC, and an ambient temperature of $-10^{\circ}\mathrm{C}\ ^{+0\mathrm{C}^{\circ}}_{-2.8\mathrm{C}^{\circ}}$, the module shall operate as specified in sections 3.1.5 and 3.1.6, except threshold voltage shall be 35 $^{+7}_{-4}$ mv, PNP output amplitudes may increase by 20%, and the gain resolution of Paragraph 3.1.5.3 shall be NMT 4.2 mv. The only times measured shall be:

T_2	$70\ ^{+40}_{-20}$ ns
T_4	$140\ ^{+80}_{-40}$ ns
T_7	$180\ ^{+140}_{-60}$ ns
T_5 , T_6	NMT 125 ns
T_8	NMT 1.125 μs
T OFF	NMT 0.45 μs

3.1.7.3 With the input voltage adjusted to 16.5 ± 0.1 VDC, and an ambient temperature of $70^{\circ}\mathrm{C}\ ^{+2.8\mathrm{C}^{\circ}}_{-0\mathrm{C}^{\circ}}$, the module shall operate as specified in sections 3.1.5 and 3.1.6, except threshold voltage shall be 35 $^{+4}_{-7}$ mv, PNP output amplitudes may increase by 20%, and the gain resolution of Paragraph 3.1.5.3 shall NMT 4.2 mv. The only times measured shall be:

T_2	$70\ ^{+40}_{-20}$ ns
T_4	$140\ ^{+80}_{-60}$ ns
T_7	$180\ ^{+140}_{-60}$ ns
T_5, T_6	NMT 125 ns
T_8	NMT 1.125 μs
T OFF	NMT 0.45 μs

4. QUALITY ASSURANCE PROVISIONS: Same as PS 2003981

5. PREPARATION FOR DELIVERY: Same as PS 2003981

6. NOTES: None

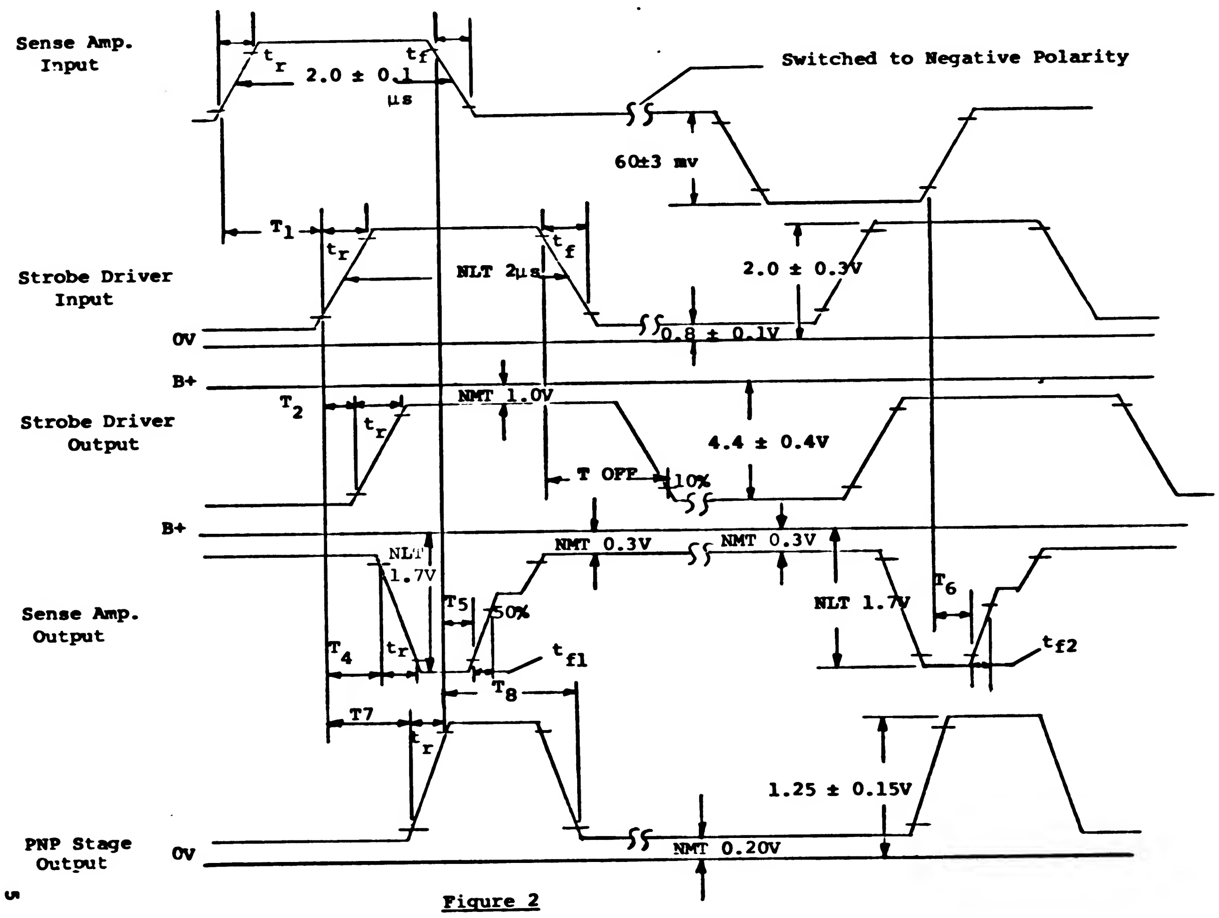

Sense Amp. Input
Strobe Driver Input
Strobe Driver Output
Sense Amp. Output
PNP Stage Output
0V
B+
B+
0V
Switched to Negative Polarity
t_r
t_f
2.0 ± 0.1 μs
60±3 mv
T_1
t_r
t_f
NLT 2μs
2.0 ± 0.3V
0.8 ± 0.1V
T_2
t_r
NMT 1.0V
4.4 ± 0.4V
T OFF
10%
NMT 0.3V
NMT 0.3V
NLT 1.7V
NLT 1.7V
T_4
t_r
T_5
50%
t_{f1}
T_8
T_6
t_{f2}
T7
t_r
1.25 ± 0.15V
NMT 0.20V

Figure 2

APOLLO G&N Specification
PS 2016017 Rev -
Original Issue Date: 18 MAY 1967
Release Authority: TDRR 33806
Class A Release

PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENT

FIXED MEMORY SENSE AMPLIFIER MODULE B14

DRAWING NO. 2003981

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA

This specification consists of pages 1 to 5 inclusive.

APPROVALS	NASA/MSC	EC Hall 3/3/67 4/7/67	~~2/10/67~~ MIT/IL 4/7/67	ICCB 3/17/67	1-30-67 BC RAY

APOLLO G&N Specification
PS 2016017 Rev -
Original Issue Date:
Release Authority: TDRR
Class A Release

ADDENDUM NOTICE

This Specification has been prepared as an Addendum to:

Specification No. PS 2003981
Revision F

FOR

FIXED MEMORY SENSE AMPLIFIER MODULE B14
Used With
APOLLO G&N System

The exact content of specification PS 2003981 used as the basic document for this addendum is the revision referenced above, and the exceptions stated below.

1. SCOPE

This specification establishes the detail requirements for complete identification and acceptance of the Fixed Memory Sense Amplifier Module Part Number 2003981-031.

2. APPLICABLE DOCUMENTS: Same as PS 2003981

3. REQUIREMENTS: Same as PS 2003981 except as stated below.

3.1.6 Delay Time

3.1.6.1 Strobe Driver Output (STROBE, STROBF). The Strobe Driver output shall be as shown in Figure 2, and shall have the following characteristics when an input as specified in section 4.1.5.2 is applied.

Amplitude (high)	NMT 1.0V below B+
Amplitude (low)	4.4 ± 0.4V below B+
Rise Time (t_r)	NMT 60 nanosec
T_2	70 ± 20 nanosec
T OFF	NMT 0.375 μsec

3.1.7 Marginal Voltages and Temperature Extremes.

3.1.7.1 With the input voltage adjusted to 12.2 ± 0.1 VDC, and an ambient temperature of $-10^{\circ}C\,^{+0C^{\circ}}_{-2.8C^{\circ}}$, the module shall operate as specified in sections 3.1.5 and 3.1.6, except threshold voltage shall be $35\,^{+7}_{-4}$ mv, and PNP output amplitudes may decrease by 20%.

The only times measured shall be:

T_2	70 +40 -20 ns
T_4	140 +80 -40 ns
T_7	180 +140 -60 ns
T_5, T_6	NMT 125 ns
T_8	NMT 1.125 μs
T OFF	NMT 0.45 μs

3.1.7.2 With the input voltage adjusted to 16.5 ± 0.1 VDC, and an ambient temperature of $-10^{\circ}C \, {}^{+0C^{\circ}}_{-2.8C^{\circ}}$, the module shall operate as specified in sections 3.1.5 and 3.1.6, except threshold voltage shall be $35 \, {}^{+7}_{-4}$ mv, and PNP output amplitudes may increase by 20%. The only times measured shall be:

T_2	$70 \, {}^{+40}_{-20}$ ns
T_4	$140 \, {}^{+80}_{-40}$ ns
T_7	$180 \, {}^{+140}_{-60}$ ns
T_5, T_6	NMT 125 ns
T_8	NMT 1.125 µs
T OFF	NMT 0.45 µs

3.1.7.3 With the input voltage adjusted to 16.5 ± 0.1 VDC, and an ambient temperature of $70^{\circ}C \, {}^{+2.8C^{\circ}}_{-0C^{\circ}}$, the module shall operate as specified in sections 3.1.5 and 3.1.6, except threshold voltage shall be $35 \, {}^{+4}_{-7}$ mv, and PNP output amplitudes may increase by 20%. The only times measured shall be:

T2	$70 \, {}^{+40}_{-20}$ ns
T4	$140 \, {}^{+80}_{-40}$ ns
T7	$180 \, {}^{+140}_{-60}$ ns
T5, T6	NMT 125 ns
T8	NMT 1.125 µs
T OFF	NMT 0.45 µs

4. QUALITY ASSURANCE PROVISIONS: Same as PS 2003981
5. PREPARATION FOR DELIVERY: Same as PS 2003981
6. NOTES: None

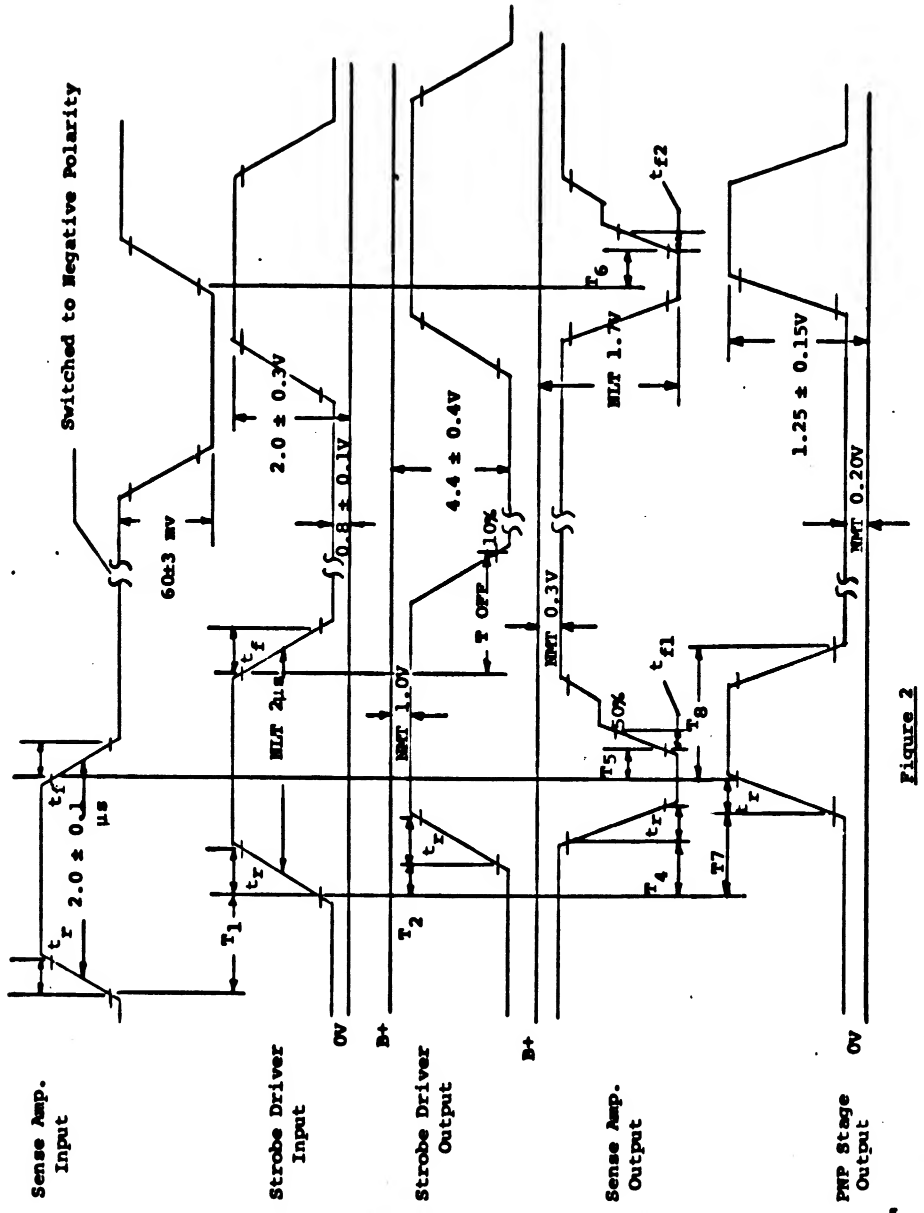

Sense Amp. Input
Strobe Driver Input
Strobe Driver Output
Sense Amp. Output
PNP Stage Output
0V
B+
B+
0V
Switched to Negative Polarity
t_r
2.0 ± 0.1 µs
t_f
60±3 mv
T_1
t_r
t_f
MLT 2µs
2.0 ± 0.3V
0.8 ± 0.1V
T_2
t_r
MMT 1.0V
T OFF
10%
4.4 ± 0.4V
MMT 0.3V
T_4
t_r
T_5
50%
t_{f1}
T_8
MLT 1.7V
T_6
t_{f2}
T_7
t_r
MMT 0.20V
1.25 ± 0.15V

Figure 2

APOLLO G&N Specification
PS 2016018 Rev -
Original Issue Date: 18 MAY 1967
Release Authority: TDRR 33806
Class A Release

PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

ERASABLE MEMORY SENSE AMPLIFIER MODULE B13

DRAWING NO. 2003982

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA

This specification consists of pages 1 to 5 inclusive.

APPROVALS	NASA/MSC	3/3/67	3/10/67 MIT/IL	CCB 5/18/67	RAY

APOLLO G&N Specification
PS 2016018 Rev -
Original Issue Date:
Release Authority: TDRR
Class A Release

ADDENDUM NOTICE

This Specification has been prepared as an Addendum to:

Specification No. PS 2003982
Revision F

FOR

ERASABLE MEMORY SENSE AMPLIFIER MODULE B13

Used With

APOLLO G&N System

The exact content of specification PS 2003982 used as the basic document for this addendum is the revision referenced above, and the exceptions stated below.

1. SCOPE

This specification establishes the detail requirements for complete identification and acceptance of the Erasable Memory Sense Amplifier Module B13 Part Number 2003982-031.

2. APPLICABLE DOCUMENTS: Same as PS 2003982.

3. REQUIREMENTS: Same as PS 2003981 except as stated below.

3.1.6 Delay Time

3.1.6.1 Strobe Driver Output (STROBE, STROBF). The Strobe Driver output shall be as shown in Figure 2, and shall have the following characteristics when an input as specified in section 4.1.5.2 is applied.

Amplitude (high)	NMT 1.0V below B+
Amplitude (low)	4.4 ± 0.4V below B+
T_2	70 ± 20 nanosec
T OFF	NMT 0.375 µsec
Rise Time (t_r)	NMT 60nanosec

3.1.7 Marginal Voltage and Temperature Extremes.

3.1.7.1 With the input voltage adjusted to 12.2 + 0.1 VDC, and an ambient temperature of $-10^{\circ}C\,^{+0C^{\circ}}_{-2.8C^{\circ}}$, the module shall operate as specified in paragraphs 3.1.5 and 3.1.6, except threshold voltage shall be 18^{+7}_{-4} mv, and PMP output amplitudes may decrease by 20%. The only times measured shall be:

T_2	70 +40 -20 ns
T_4	140 +80 -40 ns
T_7	180 +140 -60 ns
T_5, T_6	NMT 125 ns
T_8	NMT 1.125 µs
T OFF	NMT 0.45 µs

3.1.7.2 With the input voltage adjusted to 16.5 ± 0.1 VDC, and an ambient temperature of $-10^{\circ}\mathrm{C}\ ^{+0\mathrm{C}^{\circ}}_{-2.8\mathrm{C}^{\circ}}$, the module shall operate as specified in paragraphs 3.1.5 and 3.1.6, except threshold voltage shall be 18 $^{+7}_{-4}$ mv, and PNP output amplitudes may increase by 20%. The only times measured shall be:

T_2	70 $^{+40}_{-20}$ ns
T_4	140 $^{+80}_{-40}$ ns
T_7	180 $^{+140}_{-60}$ ns
T_5, T_6	NMT 125 ns
T_8	NMT 1.125 µs
T OFF	NMT 0.45 µs

3.1.7.3 With the input voltage adjusted to 16.5 ± 0.1 VDC, and an ambient temperature of $70^{\circ}\mathrm{C}\ ^{+2.8\mathrm{C}^{\circ}}_{-0\mathrm{C}^{\circ}}$, the module shall operate as specified in Paragraphs 3.1.5 and 3.1.6, except threshold voltage shall be 18 $^{+4}_{-7}$ mv, and PNP output amplitudes may increase by 20%. The only times measured shall be:

T_2	70 $^{+40}_{-20}$ ns
T4	140 $^{+80}_{-40}$ ns
T_7	180 $^{+140}_{-60}$ ns
T5, T6	NMT 125 ns
T8	NMT 1.125 µs
T OFF	NMT 0.45 µs

4. QUALITY ASSURANCE PROVISIONS: Same as PS 2003982

5. PREPARATION FOR DELIVERY: Same as PS 2003982

6. NOTES: None

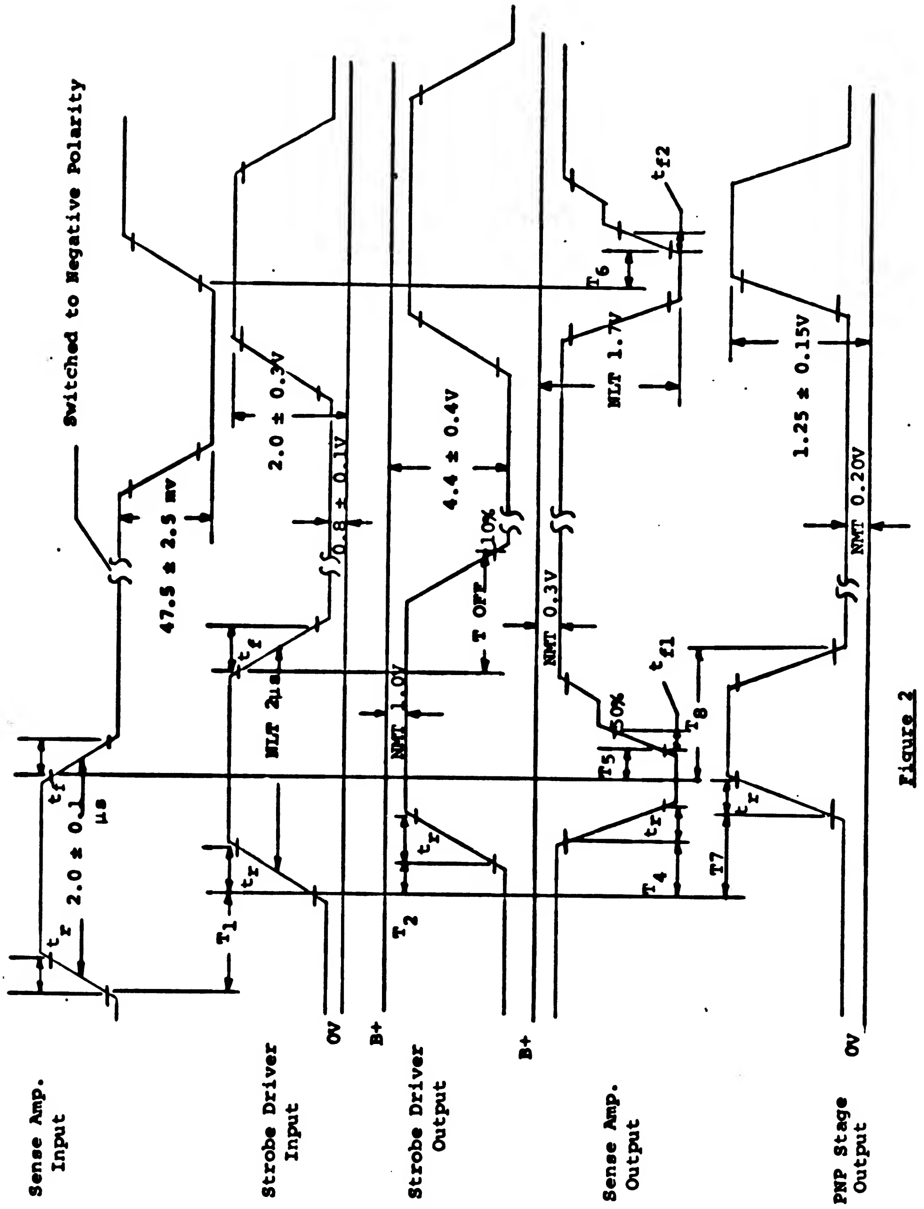

Sense Amp. Input
Strobe Driver Input
Strobe Driver Output
Sense Amp. Output
PNP Stage Output
0V
B+
B+
0V
Switched to Negative Polarity
t_r
2.0 ± 0.1 μs
t_f
47.5 ± 2.5 mv
T_1
t_r
NLT 2μs
t_f
2.0 ± 0.3V
0.8 ± 0.1V
T_2
t_r
NMT 1.0V
T OFF
10%
4.4 ± 0.4V
T_4
t_r
T_5
50%
T_8
t_{f1}
NMT 0.3V
NLT 1.7V
T_6
t_{f2}
T7
t_r
NMT 0.20V
1.25 ± 0.15V

Figure 2

APOLLO G&N Specification
PS 2016020 Rev. A
Original Issue Date: 17 AUG 1967
Release Authority: TDRR #34351
Class A Release

PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENT

APOLLO GUIDANCE COMPUTER SUBSYSTEM

DRAWING NO. 2003991

Record of Revisions

Ⓜ Ⓐ

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA
11-16-67	A	35077	1, 2, 3	FA	FA

This specification consists of pages 1 to 4 inclusive.

APPROVALS	NASA/MSC	Eldon C Hall 6/16/67 8/8/67	W Stameris 16 June 67 MIT		14 June 67 6/15/67 RAY

APOLLO G&N Specification
PS 2016020 Rev. A
Original Issue Date:
Release Authority: TDRR
Class A Release

ADDENDUM NOTICE

This Specification has been prepared as an Addendum to:

Specification No. PS 2016007

Revision E

FOR

APOLLO GUIDANCE COMPUTER SUBSYSTEM

The exact content of specification PS 2016007 used as the basic document for this addendum is the revision referenced above, and the exceptions stated below.

1.0 SCOPE

This specification establishes the detail requirements for complete identification and acceptance of the Apollo Guidance Computer, and DSKY, Part Number 2003993 -021 and -031 and 2003200-051, hereinafter called the AGC and the Display and Keyboard Assy, Part Number 2003994-011 and -021 hereinafter called the DSKY.

2.0 APPLICABLE DOCUMENTS: Same as PS 2016007.

3.0 REQUIREMENTS: Same as PS 2016007 except Paragraph 3.1.1.18 where Signal D-207 of Table 3-9 "Input Signals" shall read as follows:

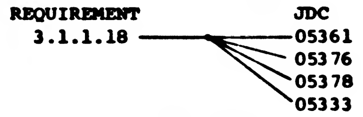
SIGNAL NAME	AGC CONNECTOR A51 PIN NUMBER	DSKY CONNECTOR J9 PIN NUMBER	CHANNEL-BIT POSITION and BIT CONTENT
D-207 STBY	502	28 (MAIN&NAV)	CH32-14 ZERO

NOTE: The requirements of PS 2016007 shall not apply to DSKY 2003950.

4.0 QUALITY ASSURANCE REQUIREMENTS: Same as PS 2016007 except

Paragraph 4.1, Table 4-1, shall be as follows for

Requirement 3.1.1.18

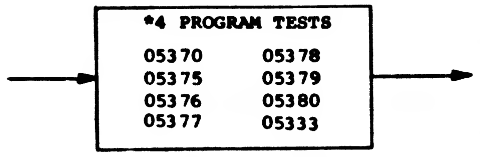


Paragraph 4.2.2

JDC listing shall have the following added

05333 Astronaut Proceed Test

Assembly Test Plan shall be modified as follows:



APOLLO G&N Specification
PS 2016020 Rev. B
Original Issue Date: 17 AUG 1967
Release Authority: TDRR # 34351
Class A Release

PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENT

APOLLO GUIDANCE COMPUTER SUBSYSTEM

DRAWING NO. 2003991

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA
11-16-67	A	35077	1, 2, 3	FA	FA
12-21-67	B	35321	1, 2, 3	SB FA	SB FA

This specification consists of pages 1 to 4 inclusive.

APPROVALS	A. C. Metzger NASA/MSC	Eldon C Hall 6/16/67 8/8/67	W Stameris 16 June 67 MIT/IL	ECB	F. M. Shepard 14 June 67 R. P. Zagrodnik 6/15/67 RAY

APOLLO G&N Specification
PS 2016020 Rev. B
Original Issue Date:
Release Authority: TDRR
Class A Release

ADDENDUM NOTICE

This Specification has been prepared as an Addendum to:

Specification No. PS 2016007

Revision J

FOR

APOLLO GUIDANCE COMPUTER SUBSYSTEM

The exact content of specification PS 2016007 used as the basic document for this addendum is the revision referenced above, and the exceptions stated below.

1.0 SCOPE

This specification establishes the detail requirements for complete identification and acceptance of the Apollo Guidance Computer, and DSKY, Part Number 2003993-021, -031 and -041 and 2003200-051, hereinafter called the AGC and the Display and Keyboard Assy, Part Number 2003994-011 and -021, hereinafter called the DSKY.

2.0 APPLICABLE DOCUMENTS: Same as PS 2016007.

3.0 REQUIREMENTS: Same as PS 2016007 except Paragraph 3.1.1.18 where Signal D-207 of Table 3-9 "Input Signals" shall read as follows:

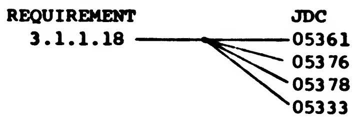
SIGNAL NAME	AGC CONNECTOR A51 PIN NUMBER	DSKY CONNECTOR J9 PIN NUMBER	CHANNEL-BIT POSITION and BIT CONTENT
D-207 STBY	502	28 (MAIN&NAV)	CH32-14 ZERO

NOTE: The requirements of PS 2016007 shall not apply to DSKY 2003950.

4.0 QUALITY ASSURANCE REQUIREMENTS: Same as PS 2016007 except

Paragraph 4.1, Table 4-1, shall be as follows for

Requirement 3.1.1.18

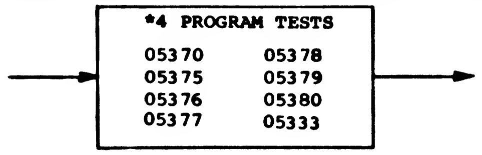


Paragraph 4.2.2

JDC listing shall have the following added

05333 Astronaut Proceed Test

Assembly Test Plan shall be modified as follows:



APOLLO G&N Specification
PS 2016020 Rev. C
Original Issue Date: 17 AUG 1967
Release Authority: TDRR #34351
Class A Release

PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENT

APOLLO GUIDANCE COMPUTER SUBSYSTEM

DRAWING NO. 2003991

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA
11-16-67	A	35077	1, 2, 3	FA	FA
12-21-67	B	35321	1, 2, 3	SB FA	SB FA
12-21-67	C	35328	1, 2	SB FA	SB FA

This specification consists of pages 1 to 4 inclusive.

APPROVALS	NASA/MSC	Eldon C Hall 6/16/67 8/8/67	W Stameris 16 June 67 8 Aug 67 MIT/IL	C&B	E. M. Shepard 14 June 67 6/15/67 RAY

APOLLO G&N Specification
PS 2016020 Rev. C
Original Issue Date:
Release Authority: TDRR
Class A Release

ADDENDUM NOTICE

This Specification has been prepared as an Addendum to:

Specification No. PS 2016007

Revision K

FOR

APOLLO GUIDANCE COMPUTER SUBSYSTEM

The exact content of specification PS 2016007 used as the basic document for this addendum is the revision referenced above, and the exceptions stated below.

APOLLO G&N Specification
PS 2016020 Rev. D
Original Issue Date: 17 AUG 1967
Release Authority: TDRR #34351
Class A Release

PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENT

APOLLO GUIDANCE COMPUTER SUBSYSTEM

DRAWING NO. 2003993 and 2003994

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA
11-16-67	A	35077	1, 2, 3	FA	FA
12-21-67	B	35321	1, 2, 3	FA	FA
12-21-67	C	35328	1, 2	FA	FA
4/26/68	D	36116	1, 2	FA	FA

This specification consists of pages 1 to 4 inclusive.

APPROVALS	NASA/MSC	Eldon C Hall 6/16/67 8/8/67	W Stameris 16 June 67 MIT/IL		14 June 67 6/15/67 RAY

APOLLO G&N Specification
PS 2016020 Rev. -
Original Issue Date: 17 AUG 1967
Release Authority: TDRR #34351
Class A Release

PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENT

APOLLO GUIDANCE COMPUTER SUBSYSTEM

DRAWING NO. 2003991

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA

This specification consists of pages 1 to 4 inclusive.

APPROVALS	A. C. Metzger NASA/MSC	Eldon C Hall 6/16/67 8/8/67	W Stameris 16 June 67 8 Aug 67 MIT/IL	CCB	F. M. Shepard 14 June 67 R. G. Ragan 6/15/67 RAY

APOLLO G&N Specification
PS 2016020 Rev. -
Original Issue Date:
Release Authority: TDRR
Class A Release

ADDENDUM NOTICE

This Specification has been prepared as an Addendum to:

Specification No. PS 2016007

Revision D

FOR

APOLLO GUIDANCE COMPUTER SUBSYSTEM

The exact content of specification PS 2016007 used as the basic document for this addendum is the revision referenced above, and the exceptions stated below.

1.0 SCOPE

This specification establishes the detail requirements for complete identification and acceptance of the Apollo Guidance Computer, and DSKY, Part Number 2003993 -021 and -031 and 2003200-051, hereinafter called the AGC and the Display and Keyboard Assy, Part Number 2003994-011 hereinafter called the DSKY.

2.0 APPLICABLE DOCUMENTS: Same as PS 2016007.

3.0 REQUIREMENTS: Same as PS 2016007 except Paragraph 3.1.1.18 where Signal D-207 of Table 3-9 "Input Signals" shall read as follows:

SIGNAL NAME	AGC CONNECTOR A51 PIN NUMBER	DSKY CONNECTOR J9 PIN NUMBER	CHANNEL-BIT POSITION and BIT CONTENT
D-207 STBY	502	28 (MAIN&NAV)	CH32-14 ZERO

NOTE: The requirements of PS 2016007 shall not apply to DSKY 2003950.

4.0 QUALITY ASSURANCE REQUIREMENTS: Same as PS 2016007 except

Paragraph 4.1, Table 4-1, shall be as follows for

Requirement 3.1.1.18

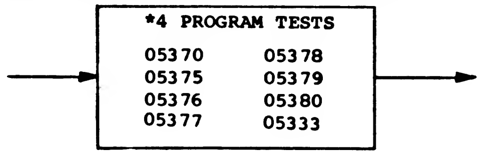
REQUIREMENT	JDC
3.1.1.18	05361
	05376
	05378
	05333

Paragraph 4.2.2

JDC listing shall have the following added

05333 Astronaut Proceed Test

Assembly Test Plan shall be modified as follows:



*4 PROGRAM TESTS

05370
05375
05376
05377
05378
05379
05380
05333

5.0 PREPARATION FOR DELIVERY: Same as PS 2016007.

6.0 NOTES: None

APOLLO G&N Specification
PS 2016026 Rev -
Original Issue Date: 31 JAN 68
Release Authority: TDRR 35523
Class A Release

PROCUREMENT SPECIFICATION
PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS
COMPUTER TEST SET ASSEMBLY
DRAWING NO. 2014042

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA

This specification consists of pages 1 to 8 inclusive.

APPROVALS	NASA/MSC	10/20/67	W Stameris 31 Oct 67 MIT/IL	CCB 31 Jan 68	D. M. Sleeper 8 AUG 67 P. Ouellette 8/23/67 RAY

1. SCOPE

This specification establishes the detail requirements for complete identification and acceptance of the Computer Test Set Assembly, Part Number 2014042-071, hereinafter called CTS.

2. APPLICABLE DOCUMENTS. Same as PS 2014042.

3. REQUIREMENTS: Same as PS2014042 except as stated below:

3.1.4 AGC Stops.

3.1.4.13 CTS Request (System Mode and WORDLOCK) BLOCK II only.

3.1.9 Monitor.

3.1.9.1 The CTS shall provide a means of trapping data in all CTS display registers excepting A and Fixed Extension. The data trap condition shall be enabled by the Counter Stop RPTR switch and an "OR" of the AGC Alarms 1, 2, 3, 4, 5, 15, 16, 17, 18 and PARITY FAIL (BLOCK II only).

3.1.17 System-Subsystem Test.

3.1.17.2 DELETE

3.1.18 Alarms.

3.1.18.1 The CTS shall provide a means of inhibiting the AGC Alarms 1, 2, 3, 4, 5, 15, 16, 17, 18 and Parity Fail upon the occurrence of any alarm above. Coincident Alarms shall be allowed (BLOCK II only).

3.1.25 Interface.

3.1.25.5.5.2 Block II PIPA. The CTS shall be capable of driving the Block II AGC PIPA Input Counters in the ONE SHOT, TAPE READER and OUT-IN modes.

3.1.25.5.5.3 Block II PIPA FREE RUN. The CTS shall be capable of driving all six or any five outputs of the six Block II PIPA Counter Inputs simultaneously. The STANDARD RATE mode shall be used to test the both-pulse and no pulse PIPA ALARMS, and the TWO PHASE mode shall be used to test the missing pulse PIPA ALARM.

3.1.12 Vacuum. The module shall be capable of operating as part of an AGC in an atmosphere of NMT 1 mm/Hg with coldplate coolant temperature at 35 ± 5°F. It shall produce the proper Self-Check and Parity Checks as applicable to that particular program assembly of which the module is a part.

3.2 PRODUCT CONFIGURATION

3.2.1 Drawings. The configuration of the assembly shall be in accordance with APOLLO G&N Dwgs. 2003972/2010802 and all drawings and engineering data referenced thereon.

3.2.2 Weight. Weight of the module shall be recorded.

4. QUALITY ASSURANCE PROVISIONS

4.1 GENERAL. The responsible contractor of the assembly shall be responsible for the accomplishment of each test required herein. See Table IV, Product Performance and Configuration Requirement/Quality Verification Cross Reference Index.

TABLE IV

Requirements	Verification	Applicable JDC
3.1.1	4.2.2	04255
3.1.2	4.2.3	04255
3.1.3	4.2.4	04255
3.1.4	4.2.5	04255
3.1.5.1	4.2.6.1	04255
3.1.5.2	4.2.6.2	04255
3.1.5.3	4.2.6.3	04255
3.1.7	4.2.7	04255
3.1.8	4.2.8	04255
3.1.9.1	4.2.9.1	04255
3.1.9.2	4.2.9.2	04255
3.1.9.3	4.2.9.3	04255
3.1.9.4	4.2.9.4	04255
3.1.10.1	4.3.1.1	04255
3.1.10.2	4.3.1.2	04255
3.1.10.3	4.3.1.3	04256
3.1.11	4.3.2	04255
3.1.12	4.3.3	04257 or 04258
3.2.1	4.2.1	04255
3.2.2	4.2.10	04255

APOLLO G&N Specification
PS 2016042 Rev. B
Original Issue Date: 31 OCT 69
Release Authority: TDRR 37902
Class A Release

PROCUREMENT SPECIFICATION
PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS
FIXED MEMORY MODULE B1-B6 ASSEMBLY

Record of Revisions

Ⓜ

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA
5/4/70	A	38029	1, 19, 10	DMS F.G.	DMS F.G.
6/24/70	B	38057	1, 10	DMS F.G.	DMS F.G.

This specification consists of pages 1 to 24 inclusive.

APPROVALS					
	9-4-69 NASA/MSC	CC Hall 8/1/69	1 Aug 69 MIT/IL	10/31/69 CCB	D.M. Sleeper 20 Feb 69 3/1/69 RAY

APOLLO G&N Specification
PS 2016042 Rev. -
Original Issue Date: 31 OCT 69
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Class A Release

PROCUREMENT SPECIFICATION
PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS
FIXED MEMORY MODULE B1-B6 ASSEMBLY

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA

This specification consists of pages 1 to 24 inclusive.

APPROVALS	9-4-69 NASA/MSC	CC Hall 8/1/69 1 aug 69 MIT/IL	10/31/69 CCB	D. M. Sleeper 20 Feb 69 8/1/69 RAY

TABLE III

PIN NO.	to	PIN NO.	PIN NO.	to	PIN NO.
402		102	415		115
405		105	416		116
406		106	417		117
407		107	418		118
408		108	419		119
409		109	420		120
410		110	103		104
411		111	121		122
412		112	123		124
413		113	404		403
414		114	422		421
			424		423

3.1.5.3 The resistance between pins 401 and 101 shall be not less than 6 ohms, nor more than 25 ohms.

3.1.6 Input Voltage. The assembly shall function as specified herein when supplied with 14.0 ± 0.5 Vdc through a 3000 ohm ± 5% resistor to pin 201.

*3.1.7 Program Content. When the contents of the Fixed Memory Module are compared to the tester tape programmed in accordance with ND 1002378, each core shall contain the correct information.

3.1.8 Clear Mode. With the input and timing waveforms as specified in paragraph 4.2.8, the output waveform at the manufacturer's test sense line (pins 101 and 401) shall be as shown in Figure 3 and defined as follows:

Zero noise (V_0 max), measured between 1.1 ± 0.05 μsec

and 2.3 ± 0.05 μsec after the start of Logic Reset (FCR), shall be NMT 25 mv.

*NOTE: For tester tapes not prepared per ND 1002378 check sum & parity checks may be made in an AGC computer.

3.1.12 Vacuum. The module shall be capable of operating as part of an AGC in an atmosphere of NMT 1 mm/Hg with coldplate coolant temperature at 35 ± 5°F. It shall produce the proper Self-Check and Parity Checks as applicable to that particular program assembly of which the module is a part.

3.2 PRODUCT CONFIGURATION

3.2.1 Drawings. The configuration of the assembly shall be in accordance with APOLLO G&N Dwgs. 2003972/2010802 and all drawings and engineering data referenced thereon.

3.2.2 Weight. Weight of the module shall be recorded.

4. QUALITY ASSURANCE PROVISIONS

4.1 GENERAL. The responsible contractor of the assembly shall be responsible for the accomplishment of each test required herein. See Table IV, Product Performance and Configuration Requirement/Quality Verification Cross Reference Index.

TABLE IV

Requirements	Verification	Applicable JDC
3.1.1	4.2.2	04255
3.1.2	4.2.3	04255
3.1.3	4.2.4	04255
3.1.4	4.2.5	04255
3.1.5.1	4.2.6.1	04255
3.1.5.2	4.2.6.2	04255
3.1.5.3	4.2.6.3	04255
3.1.7	4.2.7	04255
3.1.8	4.2.8	04255
3.1.9.1	4.2.9.1	04255
3.1.9.2	4.2.9.2	04255
3.1.9.3	4.2.9.3	04255
3.1.9.4	4.2.9.4	04255
3.1.10.1	4.3.1.1	04255
3.1.10.2	4.3.1.2	04255
3.1.10.3	4.3.1.3	04256
3.1.11	4.3.2	04255
3.1.12	4.3.3	04257
3.2.1	4.2.1	04255
3.2.2	4.2.10	04255

4.3.2 Vibration. Subject the module to the vibration limits specified in paragraph 3.1.11, and verify that the module meets the continuity requirements of paragraph 3.1.11.

4.3.3 Vacuum. With the ambient atmospheric pressure vaired as specified in paragraph 3.1.12, test the module per JDC 04257 and verify its successful performance, using a qualified computer and Dsky's.

4.3.4 Qualified Computer. A computer shall be deemed qualified by successfully passing the following tests.

JDC	05343	Equipment Set-Up
	05344	Equipment Power Turn-On
	05345	Computer Power Turn-On
	05391	E-Memory Capacitor Selection
	05342	Adder Voltage Frequency Test
	05374	Marginal Frequency, Voltage, Thermal Test
	05394	Transient Voltage Test
	05351	Marginal Voltage Test
	05376	Automatic Newspeak Test
	05379	DSKY Test (Indicator & Keyboard)
	05382	Standby E-Memory Test
	05385	DSKY Spacecraft Signals
	05384	Priority of Interrupts
	05388	CTS Control of Newspeak

4.3.5 Qualified Dsky's. A DSKY shall be deemed qualified by successfully passing the following tests:

JDC	05343	Equipment Set-Up
	05344	Equipment Power Turn-On
	05345	Computer Power Turn-On
	05391	E Memory Capacitor Selection
	05342	Adder Voltage Frequency Test
	05374	Marginal Frequency, Voltage, Thermal Test
	05394	Transient Voltage Test
	05351	Marginal Voltage Test
	05376	Automatic Newspeak Test
	05379	DSKY Test (Indicator & Keyboard)
	05382	Standby E-Memory Test
	05385	DSKY Spacecraft Signals
	05384	Priority of Interrupts
	05388	CTS Control of Newspeak

APOLLO G&N Specification
PS 2016043 Rev. -
Original Issue Date: 5 FEB 69
Release Authority: TDRR 37323
Class A **Release**

PROCUREMENT SPECIFICATION
PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS
INDICATOR, EL DIGITAL (MODIFIED)
DRAWING NO. 2003988

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA

This specification consists of pages 1 to 11 inclusive.

APPROVALS	NASA/MSC	E C Hall 31 Jan 69 W. Stameris 31 Jan 69 MIT/IL	D. M. Sloop 27 Jan 69 31 Jan RAY

1. SCOPE

1.1 This specification establishes the detail requirements for complete identification and acceptance of an Indicator, EL Digital (Modified), part numbers as specified on the assembly drawing 2003988.

2. APPLICABLE DOCUMENTS

The following documents form a part of this specification to the extent specified herein.

2.1 Effective Issues. Unless otherwise specified herein, Military and Government Standards and specifications shall be the issue in effect on the date of request for proposal or invitation to bid.

SPECIFICATIONS

APOLLO G&N

ND 1002367	Specification, Acceptance Retest Requirements, AGC/DSKYS.
ND 1002214	General Specification, for Preservation, Packaging, Packing and Container Marking of APOLLO Guidance and Navigation Major Assemblies, Assemblies, Subassemblies, Parts and Associated Ground Support Equipment.
PS 2016035	Procurement Specification Product Configuration and Acceptance Test Requirements, Indicator, EL Digital.

DRAWINGS

APOLLO G&N

2004746	Indicator, Digital, Thermal Vacuum
2003988	E/L and Cover Assembly

(Copies of Specifications, Standards, Drawings, Bulletins and Publications required by suppliers in connection with specific procurement functions should be obtained from the Procuring Activity or as directed by the Contracting Officer).

2.2 Conflicting requirements. In the event of conflict between the requirements of the contract, this Specification and the documents listed in this section, the following order of precedence shall apply and the contractor shall notify MIT Apollo Management of the conflict as soon as it is determined.

a. The contract

b. This Specification

c. Documents listed in this section.

3. REQUIREMENTS

3.1 PERFORMANCE. The EL Indicator shall be subjected to and meet the following requirements.

3.1.1 As Received EL Indicator. The indicator to be used as a basis for modification shall be in accordance with PS 2016035 or the retest requirements of ND 1002367, Paragraph 4.2.2 (b). Special attention should be given to the hermetic seal requirement and structural internal support.

3.1.2 Modified EL Indicator. The modified indicator shall meet the following requirements.

3.1.2.1. Input Voltage. The assembly shall perform as specified below when supplied with 250 ± 10 VRMS, 800 ± 5 CPS, unless otherwise specified.

3.1.2.2 Indicator Illumination. The input voltage specified in Paragraph 3.1.2.1 shall be applied to the pin combinations specified in Table 3-1. All pins in Column "A" shall be connected together. All pins in Column "B" shall be connected together. The voltage shall be applied between pins in Column "A" and/or "B" and ground (pins 155 and 156) and the corresponding portions of the EL Panel shall illuminate after subjection to the thermal cycle requirements of 3.1.3 and vibration requirements of 3.1.4 and a vacuum environment of 10^{-2} TORR.

TABLE 3-1

A-Pins	B-Pins
1 thru 7 Inc.	8 thru 14 Inc.
15 thru 21 Inc.	22 thru 28 Inc.
29 thru 35 Inc.	38 thru 44 Inc.
45 thru 51 Inc.	52 thru 58 Inc.
59 thru 65 Inc.	66 thru 72 Inc.
75 thru 81 Inc.	82 thru 88 Inc.
89 thru 95 Inc.	96 thru 102 Inc.
103 thru 109 Inc.	119 thru 125 Inc.
112 thru 118 Inc.	133 thru 139 Inc.
126 thru 132 Inc.	147 thru 153 Inc.
140 thru 146 Inc.	154
110	111
73	74
36	37
157	159
160	

3.1.2.3 Safety Glass Bond. The optical cement used to bond the safety glass shall show no discoloration, cracking, crazing or other signs of substandard workmanship when examined under ten (10X) magnification.

3.1.2.4 Structural Integrity. The modified indicator shall withstand an external vacuum of less than 10^{-2} TORR without sustaining damage to the glass, or safety glass bond.

3.1.2.5 Transmittance. The entire modification process and subsequent quality testing shall cause no more than 25% loss in light intensity when compared to the as received condition.

3.1.3 THERMAL CYCLE

The Assembly shall perform as specified in paragraph 3.1.2.2 after being thermal cycled. The Assembly shall be subjected to the thermal cycle specified below:

a. Decrease the ambient temperature from room ambient (approx. $25^{\circ}C$ to $0^{\circ}C\ {}^{+\,0^{\circ}C}_{-2.8^{\circ}C}$ in not less than 20 minutes This temperature shall be maintained for 30 minutes.

b. Increase the ambient temperature to $65^{\circ}C\ {}^{+\,2.8^{\circ}C}_{-\,0^{\circ}C}$ in not less than 40 minutes. This temperature shall be maintained for 30 minutes.

c. Decrease the ambient temperature to $0^{\circ}C\ {}^{+\,0^{\circ}C}_{-\,2.8^{\circ}C}$ in not less than 40 minutes. This temperature shall be maintained for 30 minutes.

d. Increase the ambient temperature to $65^{\circ}C\ {}^{+\,2.8^{\circ}C}_{-\,0^{\circ}C}$ in not less than 40 minutes. This temperature shall be maintained for 30 minutes.

e. Decrease the ambient temperature to $0^{\circ}C\ {}^{+\,0^{\circ}C}_{-2.8^{\circ}C}$ in not less than 40 minutes. This temperature shall be maintained for 30 minutes.

3.1.3 THERMAL CYCLE (Cont.)

f. Increase the ambient temperature to $65^\circ C \, {}^{+\,2.8^\circ C}_{-0^\circ C}$ in not less than 40 minutes. This temperature shall be maintained for 30 minutes.

g. Decrease the ambinet temperature to room ambient (approx. $25^\circ C$) in not less than 20 minutes.

3.1.4 Vibration. The assembly shall perform as specified in paragraph 3.1.2.2 after being vibrated.

3.1.4.1 Vibration Limits. The assembly shall be subjected to sinusoidal vibration as follows:

a. Frequency Range	20 to 2000 to 20 CPS
b. Frequency Sweep Rate	1 octave/minute for a total traversal time of ≈ 15 minutes
c. Acceleration	10 g's peak from 40 to 2000 to 40 CPS
d. Amplitude	0.12" D.A. from 20 to 40 and 40 to 20 CPS
e. Planes	each of three mutually perpendicular axes

3.2 PRODUCT CONFIGURATION

3.2.1 Drawings. The configuration of the modified indicator shall be in accordance with APOLLO G&N Drawing 2003988 and all drawings and engineering data and processes referenced thereon.

4. QUALITY ASSURANCE PROVISIONS

4.1 GENERAL. The contractor responsible for the modification of the assembly shall be responsible for the accomplishment of each test required herein. See Table 4-1, Product Performance and Configuration Requirement/Quality Verification Cross Reference Index.

TABLE 4-1

Requirement	Verification
3.1.1	4.2.1
3.1.1	4.2.2.4
3.1.2.1	4.2.1
3.1.2.2	4.2.1
3.1.2.3	4.2.2.3
3.1.2.4	4.2.2.3
3.1.2.5	4.2.2.5
3.1.3	4.2.2.1
3.1.4	4.2.2.2

4.1.1 Nonconforming Units. Failure of the unit to pass any examination or test of this specification shall automatically classify the unit as nonconforming. Each nonconforming unit corrected by the contractor shall be reinspected. Reinspection may be limited to the test or examination which defined the nonconformance or, when directed by the cognizant inspector, a complete retest and re-examination may be required.

4.1.2 Test Conditions

4.1.2.1 Environmental. The assembly shall be tested under the following ambient conditions:

a.	Temperature	77° ± 18°F
b.	Relative Humidity	90% max
c.	Barometric Pressure:	28 to 32 inches Hg.

4.1.2.2 Module Case Ground. The tests specified in Paragraph 3.1.2 shall be conducted with pin 158 connected to ground (0 VDC).

4.2 Tests

4.2.1 Pre-modification Checkout. Inspect all units in accordance with PS 2016035 or ND 1002367 as applicable and as specified below:

4.2.1.1 Intensity. When performing intensity testing per Paragraph 4.2.1, accept only those units having 8.0 foot lamberts minimum.

4.2.1.2 Thermal-Vacuum Screen. The as received and spare EL Indicators shall be subjected to the following thermal vacuum screen test.

The EL assembly 1006315 shall have (2) strain gauges mounted on its glass display surface. One gauge (Ref. #6) vertically mounted in the center of the EL, the other gauge (Ref. #8) shall be horizontally mounted in the center of the lower half of the EL. (See Figure #1).

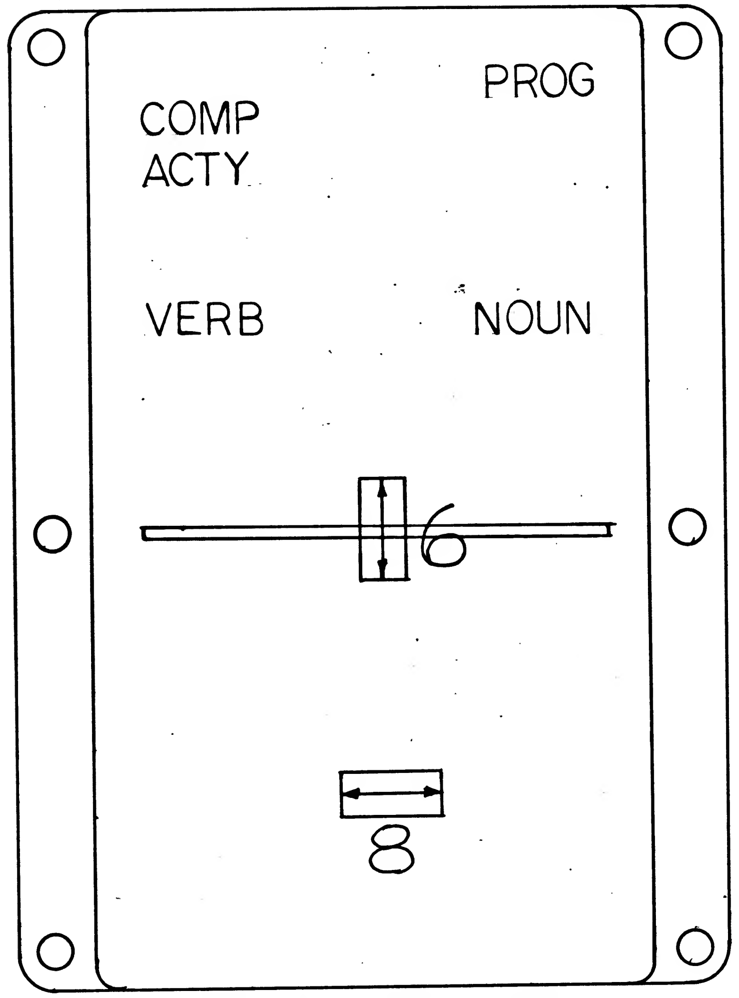

FIGURE 1 Strain Gauge Locations

4.2.1.2 Thermal-Vacuum Screen. (Continued)

The EL shall be mounted in DSKY frame or equivalent, for the following thermal vacuum test.

While maintaining a pressure of 0.1 PSIA or less, increase the temperature at a rate of approximately 20°F/hr until a temperature of $150^{\circ}\mathrm{F} \begin{array}{l} + 2^{\circ}\mathrm{F} \\ - 3^{\circ}\mathrm{F} \end{array}$ is reached. Temperature monitored on the glass.

a. If gauge #6 does not indicate a compressive strain EL is not acceptable for modification. (Lack of compressive strain indicates a defective center bar to glass bond.)

b. If gauges #6 and #8 both indicate a strain relief, unit is not acceptable. (Indicates leak in EL hermetic seal.)

Conduct visual mechanical inspection on completion of above test.

Units successfully passing the above shall be identified with Part Number 2004746 and are suitable for use in laminating safety glass per APOLLO G&N DWG 2003988.

4.2.2 Post Modification Checkout

4.2.2.1 Thermal Cycle

Subject the assembly to thermal cycle tests as specified in 3.1.3. Verify that the assembly performs in accordance with 3.1.3.

4.2.2.2 Vibration

Subject the module to the vibration test specified in para. 3.1.4. Verify that the module performs in accordance with para. 3.1.4.

4.2.2.3 Vacuum, Non-Operating.

The modified indicators shall be tested for 15 minutes in a bell jar evacuated to at least 10^{-2} TORR vacuum. There shall be no mechanical damage, discoloration, cracking, crazing or other signs of substandard workmanship per para. 3.1.2.3 when viewed with 10X magnification.

4.2.2.4 **Illumination and Intensity.** Perform the illumination and intensity portions of Paragraph 4.2.1, and assure compliance with Paragraph 3.1.1.

4.2.2.5 **Intensity Transmittance.** Compute the percent transmittance change of the safety glass lamination process by the following and assure compliance with Paragraph 3.1.2.5.

$$100\% \times \frac{\text{Pre-modification Intensity} - \text{Post Modification Intensity}}{\text{Pre-Modification Intentity}}$$

4.2.2.6 **Drawing Compliance.** The module shall be visually examined for compliance to the requirements of APOLLO G&N DWG 2003988.

5. PREPARATION FOR DELIVERY

5.1 GENERAL. Preparation for delivery shall be in accordance with Specification ND 1002214.

6. NOTES: None.

APOLLO G & N Specification
PS 2016046 Rev. A
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PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

APOLLO GUIDANCE COMPUTER SUBSYSTEM

DRAWING NO. 2003993 and 2003994

Record of Revisions

(M)

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA
10-15-70	A	38257	INITIAL RELEASE		

This specification consists of pages 1 to 6 inclusive.

APPROVALS	A. C. Me NASA/MSC	W Stameris 20 May 70 MIT/IL E.C Hall 1/04/70	RAY

APOLLO G & N Specification
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ADDENDUM NOTICE

This Specification has been prepared as an Addendum to:

Specification No. PS 2016007

Revision L

FOR

APOLLO GUIDANCE COMPUTER SUBSYSTEM

The exact content of specification PS 2016007 used as the basic document for this addendum is the revision referenced above, and the exceptions stated below.

1.0 SCOPE

This specification establishes the detail requirements for complete identification and acceptance of the Apollo Guidance Computer and DSKY, Part Number 2003993-071 and -081, hereinafter called the AGC and the Display and Keyboard Assy, Part Number 2003994-011 and -021 hereinafter called the DSKY.

2.0 APPLICABLE DOCUMENTS: Same as PS 2016007.

3.0 REQUIREMENTS: Same as PS 2016007 except; paragraph 3.1.1.18, paragraph 3.1.1.15.20 Table 3 - 7, and Table 3 - 9.

In paragraph 3.1.1.18 Signal D-207 of Table 3-9 "Input Signals" shall read as follows:

SIGNAL NAME	AGC CONNECTOR A51 PIN NUMBER	DSKY CONNECTOR J9 PIN NUMBER	CHANNEL-BIT POSITION and BIT CONTENT
D-207 STBY	502	28 (MAIN & NAV)	CH32-14 ZERO

Paragraph 3.1.1.15.20 shall read:

CHANNEL 77. Channel 77 shall consist of bit positions 1 through 9. Control pulse WCH shall clear channel 77. Control pulse RCH shall read the content of channel bit positions 1 through 9 into corresponding write lines. Control pulses WCH and RCH shall function as specified provided the octal address specified in Table 3-7 is entered into the S register. Information shall be entered into channel 77 bit positions 1, 3, 4, 5, 6, 7, 8 and 9 by alarm signals MPAL/, MCTRAL/, MSCAFL/, MWATCH/, MVFAL/, MCTRAL/, MSCAFL/, and MSCDBL/ as specified below. Alarm signal MPAL/ shall enter information into channel 77 bit position2 as specified below, only if signal MT05 is true.

ALARM SIGNAL	BIT POSITION
MPAL/	1
MPAL/	2
MTCAL/	3
MRPTAL/	4
MWATCH/	5
MVFAIL/	6
MCTRAL/	7
MSCAFL/	8
MSCDBL/	9

The Channel 77 Alarm Test, JDC 4454 performs the following tests automatically in conjunction with LAMESH:

1. Tests to determine that the Restart Monitor does not affect the normal operation of the Computer.

2. Tests at the end of the LAMESH cycle that all of the following alarms have been turned on.

   a. MPAL - CH77, Bit 1
   b. MTCAL - CH77, Bit 3
   c. MRPTAL - CH77, Bit 4
   d. MWATCH - CH77, Bit 5

3. Test that each of the following alarms can be turned on one at a time by LAMESH:

   a. MPAL - CH77, Bit 1
   b. MTCAL - CH77, Bit 3
   c. MRPTAL - CH77, Bit 4
   d. MWATCH - CH77, Bit 5

In addition, the V Fail Alarm, CH77, Bit 6 is turned on manually by lowering 28 VDC. CH77, Bit 6 is then read through the DSKY in conjunction with LAMESH.

Table 3-7 shall be extended to include channel 77 requirements as follows:

TABLE 3-7

OCTAL ADDRESS	NAME OF CONTENTS	READ AND WRITE LINES																CONTROL PULSES
		16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
0077	RESTART MONITOR	-	-	-	-	-	-	-	9	8	7	6	5	4	3	2	1	RCH
		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	WCH

NOTE: The requirements of PS 2016007 shall not apply to DSKY 2003950.

4.0 QUALITY ASSURANCE REQUIREMENTS: Same as PS 2016007 except Paragraph 4.1, Table 4-1, shall be as follows for Requirements 3.1.1.18, 3.1.5, 3.1.6, and 3.1.1.15.20.

REQUIREMENT	JDC
3.1.1.15.20	04454
3.1.1.18	05361 05376 05378 05333

3.1.5	05367 04757
**3.1.5 ALTERNATE	04251
3.1.6	05368 04758 04850
**3.1.6 ALTERNATE	04850 04252

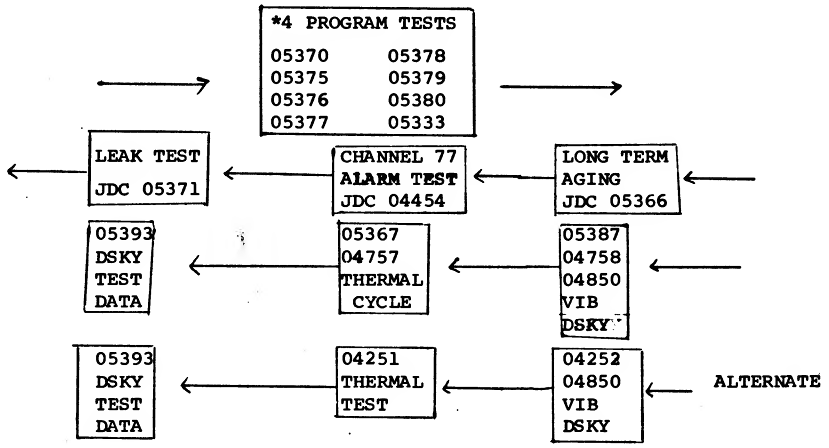
**NOTE: Alternate JDC's and Flow Diagram are to be used with the La Mesh Ropes.

Paragraph 4.2.2

JDC listing shall have the following added:

04757	DSKY Relay Thermal Test (Adapter Box)
04758	DSKY Relay Vibration Test (Adapter Box)
04850	DSKY Relay Vibration Test
05333	Astronaut Proceed Test
04251	Thermal Cycling Test DSKY/CRITICAL Relays using LAMESH PROGRAM.
04252	Vibration Test DSKY/CRITICAL Relays using LAMESH PROGRAM.
04454	Channel 77 Alarm Test

Assembly Test Plan shall be modified as follows:



5.0 PREPARATION FOR DELIVERY:

5.1 GENERAL: Preparation for Delivery shall be in accordance with Specification ND 1002214. The computer assembly and DSKY's shall be pressurized for shipment at 2.5 PSIG Max with a mixture of 90% Dry Nitrogen and 10% Helium at ambient room temperature.

6.0 NOTES: None

APOLLO G&N Specification
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PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

INTERROGATOR ELECTRONIC COMPONENT ASSEMBLY

DRAWING NO. 2900076

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Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA
1-7-66	A	MXC-208173	2		
—	B		3, 4 Was 4 pages, now 5 pages		
4-26-66	C	28347	2, 3, 4, 5 Was 5 pages, now 4 pages.	WK	--

This specification consists of page 1 to 4 inclusive.

APPROVALS	A. C. METZGER NASA/MSC	2-9-66 WKupfer 10Feb66 J M Watson MIT/IL	ACSP

ADDENDUM NOTICE

This specification has been prepared as an addendum to:

Specification No. PS2900076
Revision **E**
Release Date

FOR

INTERROGATOR ELECTRONIC COMPONENT ASSEMBLY

Used With

The APOLLO G&N System

The exact content of Specification PS2900076 used as the basic document for this addendum is the revision referenced above plus the following specification change notices to Specification PS2900076.

1. SCOPE

1.1 PURPOSE. This specification establishes the detail requirements for complete identification and acceptance of the Interrogator Electronic Component Assembly, hereafter called the Interrogator, Part Number 2900076-021.

2. APPLICABLE DOCUMENTS

2.1 Same as basic specification.

2.2 Same as basic specification.

3. REQUIREMENTS

3.1 Same as basic specification.

3.1.1 Same as basic specification.

3.1.1.1 Same as basic specification.

3.1.1.2 Same as basic specification.

3.1.1.3 Same as basic specification.

3.1.1.4 Same as basic specification.

3.1.1.5 Same as basic specification.

3.2 Same as basic specification.

3.2.1 Same as basic specification.

APOLLO G&N Specification
PS2016109 REV —
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PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

TEST CONTROL ASSEMBLY

DRAWING NO. 2900027

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA

This specification consists of page 1 to 15 inclusive.

APPROVALS	A. C. METZGER NASA/MSC	J. M. Watson 3-23-66	W Kupfer 29 Mar 66 MIT/IL		Carpenter KCSP	J F Durrenberger

1. SCOPE

1.1 PURPOSE. This specification establishes the detail requirements for complete identification and acceptance of the Test Control Assembly, hereafter referred to as the assembly, Part Number 2900027-021.

2. APPLICABLE DOCUMENTS

2.1 EFFECTIVE ISSUES. The following documents form a part of this specification to the extent specified herein. Unless otherwise specified, Military Standards and Specifications shall be the issue in effect on the date of request for proposal or invitation to bid.

SPECIFICATIONS

APOLLO G&N

ND1002214	General Specification for Preservation, Packaging, Packing and Container Marking of APOLLO Guidance and Navigation Major Assemblies, Assemblies, Subassemblies, Parts and Associated Ground Support Equipment

DRAWINGS

APOLLO G&N

2900027	Test Control Assembly

(Copies of specifications, standards, drawings, bulletins, and publications required by suppliers in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

2.2 CONFLICTING REQUIREMENTS. In event of a conflict between requirements, the following order of precedence shall apply. The contractor shall also notify MIT/IL APOLLO Management of the conflict.

a. The contract
b. This specification
c. Documents listed in this section

3. REQUIREMENTS

3.1 PERFORMANCE

3.1.1 **DC Resistance.** DC resistance shall be in accordance with Table I.

3.1.2 **Lamp Indications and Outputs.** The assembly lamp indications and outputs shall be as specified in Table II.

3.2 PRODUCT CONFIGURATION

3.2.1 **Drawings.** The configuration of the assembly shall be in accordance with Drawing 2900027 and all drawings and engineering data referenced thereon.

TABLE I

DC RESISTANCE

FROM	TO	RESISTANCE (Ohms)	CONDITIONS
J1-X	J1-W	>5	
J1-X	J1-Y	>100K	
J1-P	J1-a	<1	
J1-X	J1-c	>100K	
J1-X	J1-KK	<1	
J1-X	J1-NN	<1	
J1-X	J4-HH	<1	
J1-P	J1-Z	<1	
J1-P	J1-V	<1	OIA ON/ISS POWER DISABLED switch depressed
J1-U	J3-S	<2	OIA ON/ISS POWER DISABLED switch depressed
J1-U	J1-Y	>1K	OIA ON/ISS POWER DISABLED switch depressed
J1-b	J1-c	>100K	
J1-W	J3-k	<1	
J1-W	J3-DD	<1	
J1-A	Chassis	<1	
J2-w	J3-B	<1	
J2-x	J3-A	<1	
J3-n	J3-m	1050±15	G&N POWER ADJUST fully ccw
J3-n	J3-m	1800±150	G&N POWER ADJUST fully cw

TABLE II

LAMP INDICATIONS AND OUTPUTS

28±3 VDC INPUT		SWITCH ACTUATION	LAMP INDICATION (Illuminated unless otherwise specified)	CONDITIONS	OUTPUT AND RESISTANCE MEASUREMENTS
Hi	Lo				
J1-P J1-W J1-b J2-j J3-C J3-G J3-J J4-KK	J1-X J1-c J2-BB J4-t J4-k J4-n J4-PP		OPTICS IN COMPUTER/DAC OPERATE MODING ENABLED OIA ON INERTIAL OPTICS/RR CDU FOLLOW OIA PILOT POWER ENABLE section of CONTINUOUS GYRO TORQUE/ENABLE WHEEL RUNUP 400 CPS POWER ON MASTER RESET INHIBIT COMPUTER POWER FAIL	J2-GG connected to J2-n J2-DD connected to J2-FF Depressed to off if illuminated Illuminated for first 90 sec Depressed to off if illuminated Depressed to off if illuminated	28±3 vdc at J3-a (Hi) and J1-X (Lo) 2K ±5% from J1-c to J2-g
		ZERO OPTICS	DAC OPERATE (EXT) MASTER RESET (EXT) ZERO OPTICS		28±3 vdc at J2-K (Hi) and J1-X (Lo) 2K ±5% from J1-c to J3-GG 2K ±5% from J1-c to J3-FF
		TRACKER ON	ZERO OPTICS (EXT) TRACKER ON		2K ±5% from J1-c to J3-FF 2K ±5% from J1-c to J2-U
		ZERO OPTICS	TRACKER ON (EXT) ZERO OPTICS		
		OPTICS IN COMPUTER/DAC OPERATE	ZERO OPTICS (EXT) DAC OPERATE MASTER RESET		
		OPTICS/RR CDU ZERO/COMMAND	OPTICS/RR CDU FOLLOW (EXT) MASTER RESET (EXT) OPTICS/RR CDU ZERO/COMMAND		2K ±5% from J1-c to J2-s
		OPTICS/RR EAC ENABLE/COMMAND	OPTICS/RR CDU ZERO/COMMAND (EXT) OPTICS/RR EAC ENABLE/COMMAND		2K ±5% from J1-c to J2-T
	J4-Z	OPTICS CDU INHIBIT	OPTICS/RR EAC ENABLE/COMMAND (EXT) OPTICS CDU INHIBIT OPTICS/RR CDU ZERO TVC ENABLE G/N POWER B BUS	Depressed to off if illuminated	2K ±5% from J1-c to J2-CC
			NO CHANGE	Voltage to pin J4-Z removed	

TABLE II (Continued)

28±3 VDC INPUT		SWITCH ACTUATION	LAMP INDICATION (Illuminated unless otherwise specified)	CONDITIONS	OUTPUT AND RESISTANCE MEASUREMENTS
Hi	Lo				
		OPTICS/RR CDU FOLLOW	TVC ENABLE (EXT) OPTICS CDU INHIBIT (EXT) OPTICS/RR CDU FOLLOW MASTER RESET OPTICS/RR CDU ZERO (EXT)		
		OPTICS CDU INHIBIT	NO CHANGE		
		COARSE ALIGN/COMMAND	INERTIAL (EXT) COARSE ALIGN/COMMAND		2K ±5% from J1-c to J2-S 2K ±5% from J1-c to J2-r
		ISS EAC ENABLE/COMMAND	COARSE ALIGN/COMMAND (EXT) ISS EAC ENABLE/COMMAND		2K ±5% from J1-c to J2-r
J1-K	J4-Z		NO CHANGE		
J2-G			MASTER RESET (EXT)		
		S/C CONTROL OF SATURN/SIV B TAKEOVER	S/C CONTROL OF SATURN/SIV B TAKEOVER COMMAND SECTION OF ISS EAC ENABLE/COMMAND (EXT)		<1Ω from J1-X to J4-GG 60±6 ms after 2K ±5% from J1-c to J2-m, 2K ±5% shall exist from J1-c to J2-r
		S/C CONTROL OF SATURN/SIV B TAKEOVER	NO CHANGE		
		S/C CONTROL OF SATURN/SIV B TAKEOVER	S/C CONTROL OF SATURN/SIV B TAKEOVER (EXT) INERTIAL ISS EAC ENABLE (EXT)	Voltage to pin J1-K removed	
			NO CHANGE	Voltage to Pin J4-Z removed.	
		S/C CONTROL OF SATURN/SIV B TAKEOVER		Switch depressed and held	
		ISS CDU ZERO	ISS CDU ZERO: INERTIAL (EXT)		2K ±5% from J1-c to J2-R
		S/C CONTROL OF SATURN/SIV B TAKEOVER	NO CHANGE	Switch released	

TABLE II (Continued)

28±3 VDC INPUT		SWITCH ACTUATION	LAMP INDICATION (Illuminated unless otherwise specified)	CONDITIONS	OUTPUT AND RESISTANCE MEASUREMENTS
Hi	Lo				
J4-u	J4-t	GYRO TORQUE ENABLE/COMMAND	ISS CDU ZERO (EXT) GYRO TORQUE ENABLE/COMMAND MOMENTARY		28±3 vdc shall appear at J4-p (Hi) and J1-X (Lo) for 1.0±0.1 sec. 28±3 vdc shall appear at J4-q (Hi) and J1-X (Lo)
		ISS CDU ZERO	ISS CDU ZERO	Switch depressed and held	
		ISS CDU ZERO	ISS CDU ZERO (EXT)	Switch released	
		INERTIAL	MOMENTARY (EXT) GYRO TORQUE ENABLE/COMMAND (EXT) INERTIAL		
		ISS CDU ZERO	INERTIAL (EXT) ISS CDU ZERO		
		ISS CDU INHIBIT/COMMAND	ISS CDU INHIBIT/COMMAND ISS CDU ZERO (EXT)	ISS CDU INHIBIT illuminates in 5 seconds	5.0±0.5 sec after 28±3 vdc appears at J4-NN (Hi) and J1-X (Lo), 28±3 vdc shall disappear. 2K ±5% from J1-c to J2-s after 5 seconds.
		WHEEL RUN UP/WHEELS DISABLED	WHEELS DISABLED		
		WHEEL RUN UP/WHEELS DISABLED	WHEELS DISABLED (EXT)		
		INERTIAL	ISS CDU INHIBIT/COMMAND (EXT) INERTIAL		
	J4-MM	CONTINUOUS GYRO TORQUE/ENABLE	CONTINUOUS GYRO TORQUE/ENABLE GYRO TORQUE ENABLE		<1Ω from J4-v to J4-r <1Ω from J4-w to J4-s 28±3 vdc at J4-LL (Hi) and J1-X (Lo)
		CONTINUOUS GYRO TORQUE/ENABLE	CONTINUOUS GYRO TORQUE/ENABLE (EXT) GYRO TORQUE ENABLE (EXT)		
			MASTER RESET	Voltage to pin J2-G removed	
		COARSE ALIGN/COMMAND	COARSE ALIGN/COMMAND INERTIAL (EXT)		
J1-K J3-H			ISS EAC ENABLE		

TABLE II (Continued)

28±3 VDC INPUT		SWITCH ACTUATION	LAMP INDICATION (Illuminated unless otherwise specified)	CONDITIONS	OUTPUT AND RESISTANCE MEASUREMENTS
Hi	Lo				
		X IRIG CAGE/COMMAND	MASTER RESET (EXT) GYRO TORQUE ENABLE X IRIG CAGE/COMMAND		28±3 vdc at J4-m (Hi) and J1-X (Lo) in approximately 1 second
		X IRIG CAGE/COMMAND	X IRIG CAGE/COMMAND (EXT) MASTER RESET GYRO TORQUE ENABLE (EXT)		
		Y IRIG CAGE/COMMAND	MASTER RESET (EXT) GYRO TORQUE ENABLE Y IRIG CAGE/COMMAND		28±3 vdc at J4-j (Hi) and J1-X (Lo) in approximately 1 second
		Y IRIG CAGE/COMMAND	Y IRIG CAGE/COMMAND (EXT) GYRO TORQUE ENABLE (EXT) MASTER RESET		
		Z IRIG CAGE/COMMAND	Z IRIG CAGE/COMMAND GYRO TORQUE ENABLE MASTER RESET (EXT)		28±3 vdc at J4-h (Hi) and J1-X (Lo) in approximately 1 second
		Z IRIG CAGE/COMMAND	Z IRIG CAGE/COMMAND (EXT) GYRO TORQUE ENABLE (EXT) MASTER RESET		
		Z IRIG CAGE/COMMAND	Z IRIG CAGE/COMMAND GYRO TORQUE ENABLE MASTER RESET (EXT)		
		INERTIAL	COARSE ALIGN/COMMAND (EXT) INERTIAL IMS EAC ENABLE (EXT)		
		MASTER RESET	OPTICS/RR CDU FOLLOW (EXT) COARSE ALIGN/COMMAND Z IRIG CAGE/COMMAND (EXT) MASTER RESET INERTIAL (EXT) GYRO TORQUE ENABLE (EXT) IMS EAC ENABLE OPTICS IN COMPUTER/DAC OPERATE (EXT)	Switch depressed and held	28±3 vdc at J2-X (Hi) and J1-X (Lo)
		WHEEL RUN UP/WHEELS DISABLED	WHEELS DISABLED		

TABLE II (Continued)

28±3 VDC INPUT		SWITCH ACTUATION	LAMP INDICATION (Illuminated unless otherwise specified)	CONDITIONS	OUTPUT AND RESISTANCE MEASUREMENTS
Hi	Lo				
		WHEEL RUN UP/WHEELS DISABLED	WHEELS DISABLED (EXT)		
		MASTER RESET	OPTICS IN COMPUTER/DAC OPERATE OPTICS/RR CDU FOLLOW	Switch released	
			ISS EAC ENABLE (EXT)	Voltage removed from pin J1-K Voltage removed from pin J3-H	
		DISPLAY INERTIAL DATA	DISPLAY INERTIAL DATA OPTICS/RR EAC ENABLE OPTICS/RR CDU FOLLOW (EXT) MASTER RESET (EXT)		60±6 ms after 2K ±5% from J1-c to J2-PP, 2K ±5% from J1-c to J2-T
		DISPLAY INERTIAL DATA	DISPLAY INERTIAL DATA (EXT) OPTICS/RR EAC ENABLE (EXT) OPTICS/RR CDU FOLLOW MASTER RESET		
J3-F	J4-Z	GN&C AUTOPILOT CONTROL/TVC ENABLE	MASTER RESET (EXT) OPTICS/RR CDU FOLLOW (EXT) GN&C AUTOPILOT CONTROL/TVC ENABLE OPTICS/RR EAC ENABLE		2K ±5% from J1-c to J2-CC, 2K ±5% from J1-c to J2-T
*1		GN&C AUTOPILOT CONTROL/TVC ENABLE	MASTER RESET OPTICS/RR CDU FOLLOW GN&C AUTOPILOT CONTROL/TVC ENABLE (EXT) OPTICS/RR EAC ENABLE (EXT)		
J3-C J1-N	J1-X J2-E J2-h		PIPA LOOPS INHIBIT PIPA UP-MODE DUCOSYN EXCITATION SWITCHOVER OVERRIDE	Depressed to off if illuminated	
		PIPA LOOPS INHIBIT/COMMAND	COMMAND section of PIPA LOOPS INHIBIT/COMMAND		<1Ω from J3-D to J1-PP. 28±3 vdc at J2-F (Hi) and J1-X (Lo).
		PIPA UP-MODE/COMMAND	COMMAND section of PIPA UP-MODE/ COMMAND		28±3 vdc at J2-i (Hi) and J1-X (Lo)
		PIPA LOOPS INHIBIT/COMMAND	COMMAND section of PIPA LOOPS INHIBIT/COMMAND (EXT)		

TABLE II (Continued)

28±3 VDC INPUT		SWITCH ACTUATION	LAMP INDICATION (Illuminated unless otherwise specified)	CONDITIONS	OUTPUT AND RESISTANCE MEASUREMENTS
Hi	Lo				
		PIPA UP-MODE/COMMAND	NO CHANGE		
		PIPA LOOPS INHIBIT/COMMAND	COMMAND section of PIPA LOOPS INHIBIT/COMMAND		
*1		PIPA UP-MODE/COMMAND	COMMAND section of PIPA UP-MODE/ COMMAND (EXT)		
J1-K J1-W J2-J J2-N J2-Z J3-C J3-F J3-G J3-H J1-P	J1-X		MASTER RESET OIA ON MODING ENABLED OPTICS/RR CDU FOLLOW WHEEL RUN-UP OIA PILOT POWER COMMAND section of COARSE ALIGN/COMMAND	J2-Y jumpered to J2-e J2-M jumpered to J2-e J2-H jumpered to J2-a Illuminated for first 90 seconds	
		IG DRIVE INHIBIT	IG DRIVE INHIBIT	Switch depressed and held	28±3 vdc at J1-p (Hi) and J1-X (Lo) 28±3 vdc at J3-h (Hi) and J1-X (Lo)
		IG DRIVE INHIBIT		Switch released	28±3 vdc at J2-f (Hi) and J1-X (Lo) 8±2 vdc at J1-r (Hi) and J1-X (Lo) <1Ω from J1-X to J1-z
		MG DRIVE INHIBIT	MG DRIVE INHIBIT	Switch depressed and held	28±3 vdc at J1-t (Hi) and J1-X (Lo) 28±3 vdc at J3-j (Hi) and J1-X (Lo)
		MG DRIVE INHIBIT		Switch released	28±3 vdc at J2-d (Hi) and J1-X (Lo) 8±2 vdc at J1-u (Hi) and J1-X (Lo) <1Ω from J1-X to J1-AA
		OG DRIVE INHIBIT	OG DRIVE INHIBIT	Switch depressed and held	28±3 vdc at J1-w (Hi) and J1-X (Lo) 28±3 vdc at J3-i (Hi) and J1-X (Lo)
*1		OG DRIVE INHIBIT		Switch released	28±3 vdc at J2-b (Hi) and J1-X (Lo) 8±2 vdc at J1-x (Hi) and J1-X (Lo) <1Ω from J1-X to J1-BB
J3-C J2-Z	J1-X	MASTER RESET	IG DRIVE INHIBIT	J2-Y jumpered to J2-e	

TABLE II (Continued)

28±3 VDC INPUT		SWITCH ACTUATION	LAMP INDICATION (Illuminated unless otherwise specified)	CONDITIONS	OUTPUT AND RESISTANCE MEASUREMENTS
Hi	Lo				
		IG DRIVE INHIBIT	IG DRIVE INHIBIT (EXT)		
			NO CHANGE	Jumper from J2-Y to J2-e removed J2-M jumpered to J2-e Voltage to pin J2-Z removed	
J2-N		MASTER RESET	MG DRIVE INHIBIT		
		MG DRIVE INHIBIT	MG DRIVE INHIBIT (EXT)	Jumper from J2-M to J2-e removed J2-H jumpered to J2-a Voltage to pin J2-N removed	
J2-J		MASTER RESET	OG DRIVE INHIBIT		
*1		OG DRIVE INHIBIT	OG DRIVE INHIBIT (EXT)		
*3J1-K J1-P J1-W J2-N J2-Z J3-U	J1-X J1-e		OIA PILOT POWER OIA ON WHEEL RUN UP INERTIAL	J2-Y jumpered to J2-e J2-M jumpered to J2-e	28±3 vdc at J2-X (Hi) and J1-X (Lo) 28±3 vdc at J2-K (Hi) and J1-X (Lo)
*3		MASTER RESET	IG DRIVE INHIBIT MG DRIVE INHIBIT		
*2			INERTIAL (EXT) COMMAND section of ISS CDU INHIBIT/ COMMAND ISS CDU ZERO	Voltage removed from J1-K momentarily	2K ±5% from J1-e to J2-R
*2J1-a			MG DRIVE INHIBIT (EXT)	Voltage applied momentarily	
*3J1-r *1			ISS CDU ZERO (EXT) IG DRIVE INHIBIT (EXT) COMMAND section of ISS CDU INHIBIT/ COMMAND (EXT) INERTIAL	Voltage applied momentarily	

TABLE II (Continued)

28±3 VDC INPUT		SWITCH ACTUATION	LAMP INDICATION (Illuminated unless otherwise specified)	CONDITIONS	OUTPUT AND RESISTANCE MEASUREMENTS
Hi	Lo				
J3-F J1-W J3-c	J1-X		OIA ON RESET IG DUMP	Voltage applied to J3-F before J1-W	28±3 vdc at J3-i (Hi) and J1-X (Lo) 28±3 vdc at J3-j (Hi) and J1-X (Lo) 28±3 vdc at J3-h (Hi) and J1-X (Lo) 28±3 vdc at J3-q (Hi) and J1-X (Lo)
			RESET IG DUMP (EXT)	Voltage removed from J3-c	0±1 vdc at J3-q (Hi) and J1-X (Lo)
J3-d			RESET MG DUMP		28±3 vdc at J3-q (Hi) and J1-X (Lo)
			RESET MG DUMP (EXT)	Voltage removed from J3-d	0±1 vdc at J3-q (Hi) and J1-X (Lo)
J3-e			RESET OG DUMP		28±3 vdc at J3-q (Hi) and J1-X (Lo)
			RESET OG DUMP (EXT)	Voltage removed from J3-F Voltage removed from J3-e	0±1 vdc at J3-i (Hi) and J1-X (Lo) 0±1 vdc at J3-j (Hi) and J1-X (Lo) 0±1 vdc at J3-h (Hi) and J1-X (Lo) 28±3 vdc at J3-f (Hi) and J1-X (Lo) 28±3 vdc at J3-g (Hi) and J1-X (Lo)
*1 J3-F					28±3 vdc at J3-f (Hi) and J1-X (Lo)
J1-K J1-W J1-b J2-A J2-G J3-H J1-P J3-C J3-G	J1-X J1-e J3-w		WHEEL RUN UP OIA ON OIA PILOT POWER MODING ENABLED OPTICS/RR CDU FOLLOW COMMAND section of COARSE ALIGN/COMMAND	Illuminated for first 90 seconds J4-JJ jumpered to J2-p	<1Ω from J1-X to J1-MM
		IMU CAGE/COMMAND	IMU CAGE/COMMAND	Switch depressed and held	28±3 vdc at J2-HH (Hi) and J1-c (Lo)
			IMU CAGE COMMAND (EXT)	Voltage removed from J2-A	
			COMMAND section of IMU CAGE/COMMAND	Voltage removed from J1-K	
		IMU CAGE/COMMAND	COMMAND section of IMU CAGE/COMMAND (EXT)	Switch released	
J2-A		WHEEL RUN UP/WHEELS DISABLED	WHEELS DISABLED/WHEEL RUN UP (EXT)	If less than 90 sec since it illu.	28±3 vdc at J3-Z (Hi) and J1-X (Lo)

*1

TABLE II (Continued)

28±3 VDC INPUT		SWITCH ACTUATION	LAMP INDICATION (Illuminated unless otherwise specified)	CONDITIONS	OUTPUT AND RESISTANCE MEASUREMENTS
Hi	Lo				
J1-P J1-W J1-d J3-r	J1-X J4-Z		OIA PILOT POWER OIA ON OIA DUCOSYN POWER ON	J3-F jumpered to J1-g J3-P jumpered to J1-e	
		OPTICS POWER ON	OPTICS POWER ON		28±3 vdc at J3-J (Hi) and J1-X (Lo) <1Ω from J1-X to J1-E
		OPTICS POWER ON	OPTICS POWER ON (EXT)		
J1-K		OPTICS PWR ON	NO CHANGE		
	J2-BB	OPTICS PWR ON	OPTICS PWR ON MASTER RESET OPTICS/RR CDU FOLLOW		
		OPTICS PWR ON	OPTICS PWR ON (EXT) MASTER RESET (EXT) OPTICS/RR CDU FOLLOW (EXT)	Remove voltage from J1-K and J2-BB	
		CGC/LGC POWER ON	CGC/LGC POWER ON		28±3 vdc at J3-R (Hi) and J1-X (Lo) <1Ω from J1-X to J1-E
*1		CGC/LGC POWER ON	CGC/LGC POWER ON (EXT)		
J3-P J1-W J1-b J1-f J1-P	J1-X J1-e		OIA ON PROCEED section of PROCEED/ISS STANDBY OIA PILOT POWER	J1-G jumpered to J1-N J1-M jumpered to J3-W J2-V jumpered to J3-H	
		ISS STANDBY	PROCEED (EXT) ISS STANDBY	An external 28 vdc test lamp shall illuminated when connected to 28±3 vdc (Hi) and to J1-E (Lo). The lamp shall also illuminate when connected to 28±3 vdc (Hi) and to J4-Y (Lo).	For first 10±1 sec 28±3 vdc appears at J1-F (Hi) and J1-X (Lo). 28±3 vdc shall appear at J3-M (Hi) and J1-X (Lo) after 10±1 sec. <1Ω from J2-w to J3-y in 10 sec. <1Ω from J2-x to J3-x in 10 sec. 28±3 vdc at J3-K (Hi) and J1-X (Lo). 28±3 vdc at J1-y (Hi) and J1-X (Lo) for first 10 sec. <1Ω from J1-X to J1-D for first 10 seconds.
		INHIBIT COMPUTER POWER FAIL	INHIBIT COMPUTER POWER FAIL		2K±5% from J1-b to J4-FF
		INHIBIT COMPUTER POWER FAIL	INHIBIT COMPUTER POWER FAIL (EXT)		
		OIA ON/ISS POWER DISABLED	ISS STANDBY (EXT) PROCEED section of PROCEED/ISS STANDBY		
	J2-BB	ISS STANDBY	NO CHANGE	Voltage removed from J3-P	

TABLE II (Continued)

28±3 VDC INPUT		SWITCH ACTUATION	LAMP INDICATION (Illuminated unless otherwise specified)	CONDITIONS	OUTPUT AND RESISTANCE MEASUREMENTS
Hi	Lo				
J1-K	J3-w	ISS STANDBY	PROCEED (EXT) ISS STANDBY	Switch depressed and held	28±3 vdc at J3-HH (Hi) and J1-X (Lo)
			MASTER RESET	Switch released	
		DUCOSYN EXCITATION SWITCHOVER OVERRIDE	DUCOSYN EXCITATION SWITCHOVER OVERRIDE PROCEED section of PROCEED/ISS OPERATE	Illuminates in approximately 3 minutes	
		ISS OPERATE	PROCEED (EXT) ISS OPERATE WHEEL RUN UP MODING ENABLED INERTIAL OPTICS/RR CDU FOLLOW MASTER RESET (EXT)	 Illuminated for first 90 seconds Illuminated after 90 seconds Illuminated after 90 seconds	
J3-Z			WHEELS DISABLED		180±18 seconds after 28±3 vdc applied to J3-Z (Hi), 28±3 vdc shall appear at J2-A (Hi) and J1-X (Lo)
J2-p			IMU CAGE		
		WHEEL RUN UP/WHEEL DISABLED	COMMAND section of COARSE ALIGN/ COMMAND WHEEL RUN UP INERTIAL (EXT) MASTER RESET WHEELS DISABLED (EXT)	Voltage removed from J3-Z Illuminated for first 90 seconds	90±9 sec after wheel run up wheels disabled switch is actuated. 28±3 vdc appears at J3-G (Hi) and J1-X (Lo)
*1		ISS STANDBY	IMU CAGE (EXT) COMMAND section of COARSE ALIGN/ COMMAND (EXT) MODING ENABLED (EXT) OPTICS/RR CDU FOLLOW (EXT) ISS OPERATE (EXT)		
J1-P J3-J	J4-Z J2-BB J1-X		OIA PILOT POWER OPTICS/RR CDU FOLLOW MASTER RESET	J1-B jumpered to J1-C	<1Ω from J1-X to J1-LL

TABLE II (Continued)

28±3 VDC INPUT		SWITCH ACTUATION	LAMP INDICATION (Illuminated unless otherwise specified)	CONDITIONS	OUTPUT AND RESISTANCE MEASUREMENTS
Hi	Lo				
			OPTICS/RR CDU FOLLOW (EXT) MASTER RESET (EXT)	Voltage removed from J3-J and J2-BB	
J1-K J1-W J3-F J3-G			WHEEL RUN UP OIA ON OPTICS/RR CDU FOLLOW	Illuminated for first 90 seconds	
			OPTICS/RR CDU FOLLOW (EXT)	Voltage removed from J3-F	
		G/N POWER A BUS/G/N POWER B BUS	G/N POWER A BUS/G/N POWER B BUS		<1Ω from J1-X to J1-E
*1		400 CPS POWER ON	400 CPS POWER ON		28±3 vdc at J2-EE (Hi) and J1-X (Lo)
J1-f	J1-X		PROCEED section of PROCEED/ISS STANDBY	115±10 vac 60±6 cps applied to J1-U (Hi) and J1-Y (Lo)	
		OIA ON/ISS POWER DISABLED	ISS POWER DISABLED		
		POWER OFF	ISS POWER DISABLED (EXT)		

*1 Double lines indicate changed conditions for a new set of measurements.

*2 These operations must be run in 90 seconds.

4. QUALITY ASSURANCE PROVISIONS

4.1 PRODUCT PERFORMANCE AND CONFIGURATION REQUIREMENTS/QUALITY VERIFICATION CROSS REFERENCE INDEX

Test/Examination	Requirement	Method
DC Resistance	3.1.1	4.3.2
Lamp Indications and Outputs	3.1.2	4.3.3
Drawing Compliance	3.2.1	4.3.1

4.2 GENERAL. The contractor responsible for the manufacture of the assembly shall be responsible for the accomplishment of each test requirement herein.

4.2.1 Test Conditions

4.2.1.1 Environmental. Unless otherwise specified, the assembly shall be tested under the following ambient conditions:

a. Temperature: 25° ±10°C
b. Relative Humidity: 90% max
c. Barometric Pressure: 28 to 32 inches of Hg

4.2.2 Nonconforming Units. Failure of the assembly to pass any examinations or tests of this specification shall automatically classify the assembly as nonconforming. Each nonconforming assembly corrected by the contractor shall be reinspected. Reinspection may be limited to the test or examination which defined the nonconformance, or, when directed by the cognizant inspector, a complete retest and reexamination may be required. Nonconforming assemblies which have not been corrected will be considered for acceptance only upon formal application by the contractor to the cognizant NASA representative.

4.3 TESTS

4.3.1 Drawing Compliance. The assembly shall be visually examined for compliance with the requirements of Drawing 2900027. Particular attention shall be given to inspection for nicks, scratches, burrs, dents, encapsulant defects, contaminants, pin misalignment, and legibility and appearance of markings.

4.3.2 DC Resistance. The dc resistance test shall be performed in accordance with Table I.

4.3.3 Lamp Indications and Outputs. The test shall be performed in accordance with Table II.

5. PREPARATION FOR DELIVERY

5.1 GENERAL. Preparation for delivery shall be in accordance with Specification ND1002214.

6. NOTES. None.

ETP:lv

APOLLO G&N Specification
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PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

MONITOR PANEL ASSEMBLY

DRAWING NO. 2900031

Record of Revisions

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				MIT	NASA
4 MAY 66	A		ALL- INITIAL RELEASE	AR 5-11-66	ACM

This specification consists of page 1 to 37 inclusive.

APPROVALS	NASA/MSC	J. M. Walton 5-5-66 Geo Rose 5-11-66 MIT/IL	D Carpenter ACSP

3.1.15 G/N Voltage. With the equipment conditions as specified in 3.1.14 the G/N Voltage monitoring requirements shall be in accordance with the following:

EQUIPMENT CONDITION	REQUIREMENT
a. With the voltage present at J1-CC decreased to 21.5±0.5 vdc	G/N VOLTAGE PUSH RESET and G/N POWER MODES DISABLED indicators illuminated G/N VOLTAGE PUSH RESET, LOW indicator flashing
b. S9 momentarily in the "ALARM ENABLE" position	Alarm bell ringing ALARM INHIBITED indicator extinguished PUSH TO INHIB ALARM indicator illuminated while S9 is in the "ALARM ENABLE" position
c. 22.5±0.4 vdc present at J1-CC and the G/N VOLTAGE, PUSH RESET, LOW, HIGH indicator momentarily depressed	G/N POWER MODES DISABLED, G/N VOLTAGE PUSH RESET, and LOW indicators extinguished
d. With the voltage present at J1-CC increased to 35.5±0.5 vdc	G/N VOLTAGE PUSH RESET and G/N POWER MODES DISABLED indicators illuminated G/N VOLTAGE PUSH RESET, HIGH indicators flashing
e. 31.5±0.4 vdc present at J1-CC and the G/N VOLTAGE, PUSH RESET, LOW, HIGH indicator momentarily depressed	G/N POWER MODES DISABLED, G/N VOLTAGE PUSH RESET, and G/N VOLTAGE PUSH RESET, HIGH indicators extinguished

3.1.16 G/N Voltage Verification. With the initial MPL conditions as specified in 3.1.14, except conditions 3.1.14, k and m shall not be present, J1-JJ connected to ground, and the ISS TEST CONFIG indicator extinguished the requirements shall be as follows:

EQUIPMENT CONDITION	REQUIREMENT
a. 28 vdc present at J1-AA	G/N VOLTAGE PUSH RESET indicator illuminated G/N POWER MODES DISABLED indicator illuminated G/N VOLTAGE PUSH RESET, HIGH indicator flashing 28±4 vdc present between J1-1 and J1-FF

EQUIPMENT CONDITIONS	REQUIREMENT
b. No voltage present at J1-AA, 28 vdc present at J1-BB and the G/N VOLTAGE PUSH RESET, LOW, HIGH, indicator momentarily depressed	G/N VOLTAGE PUSH RESET indicator illuminated G/N POWER MODES DISABLED indicator illuminated G/N VOLTAGE PUSH RESET, LOW indicator flashing 28±4 vdc present between J1-i and J1-FF

3.1.17 **Prime Power Verification.** With initial equipment conditions as specified in 3.1.14, except conditions 3.1.14.k and m. shall not be present, J1-JJ connected to ground, and the ISS TEST CONFIG indicator extinguished requirements shall be as follows:

EQUIPMENT CONDITIONS	REQUIREMENT
a. 28 vdc present at J1-w (+)	PRIME POWER PUSH RESET indicator illuminated PRIME POWER PUSH RESET, LOW indicator flashing 28±4 vdc present between J1-i and J1-FF
b. No voltage present at J1-w, 28 vdc present at J1-v (+) and the PRIME POWER PUSH RESET, LOW, HIGH indicator momentarily depressed	PRIME POWER PUSH RESET indicator illuminated PRIME POWER PUSH RESET, LOW indicator flashing 28±4 vdc present between J1-i and J1-FF
c. No voltage present at J1-v, 28 vdc present at J1-u and the PRIME POWER PUSH RESET, LOW, HIGH indicator momentarily depressed	PRIME POWER PUSH RESET indicator illuminated PRIME POWER PUSH RESET, LOW indicator flashing 28±4 vdc present between J1-i and J1-FF

3.1.18 **Ducosyn Excitation Verification.** With initial MPL conditions as specified in 3.1.14, except the conditions specified in 3.1.14.f, k, and m shall not be present, J1-JJ connected to ground, and the ISS TEST CONFIG indicator extinguished, the ducosyn excitation verification shall be in accordance with the following:

EQUIPMENT CONDITION	REQUIREMENT
a. 28 vdc present at J1-y	DUCOSYN EXC PUSH RESET indicator illuminated FREQ FAIL indicator flashing 1.7±0.1 vac present at A3TP-1 (Hi) and A3TP-4 (Lo) by adjusting A5R4
b. DUCOSYN EXC PUSH RESET indicator momentarily depressed	DUCOSYN EXC PUSH RESET indicator illuminated FREQ FAIL indicator flashing 28±4 vdc present at J1-i and J1-FF

EQUIPMENT CONDITION	REQUIREMENT
a. 28 vdc present at J1-c (+) and J1-S (+)	BLOCK I SERIES 100, and ALARM INHIBITED indicators illuminated COOLANT SUPPLY FAIL indicator flashing
b. No voltage present at J1-S	Same REQUIREMENT as in a.
c. S9 momentarily in the "ALARM ENABLE" position	Alarm shall ring, ALARM INHIBITED indicator extinguished, PUSH TO INHIB ALARM illuminated while S9 is in the "ALARM ENABLE" position.
d. 28 vdc present at J2-t (+)	ALARM INHIBITED and GIMBAL LOCK CAUTION indicators illuminated, COLDPLATE TEMP FAIL indicator flashing. COOLANT SUPPLY FAIL extinguished.
e. 28 vac present at J2-a (+)	ALARM INHIBITED and GIMBAL LOCK CAUTION indicators illuminated
f. No voltage present at J2-a (+) and 28 vdc present at J1-n (+)	ALARM INHIBITED and GIMBAL LOCK CAUTION indicators illuminated
g. EQUIPMENT CONDITION in f. no longer present, 28 vdc present at J1-KK (+), S9 in the "ALARM ENABLE" position, and the PUSH TO INHIB ALARM, ALARM INHIBITED indicator momentarily depressed	BLOCK I SERIES 100, ALARM INHIBITED, -28 VDC FAIL PUSH TO RESET, and WHEEL POWER FAIL PUSH TO RESET indicators illuminated, COOLANT SUPPLY FAIL indicator flashing
h. 28 vdc present at J2-t (+)	BLOCK I SERIES 100 indicator extinguished GIMBAL LOCK CAUTION indicator illuminated and COLDPLATE TEMP FAIL indicator flashing. Alarm bell ringing, the ALARM INHIBITED indicator extinguished and the PUSH TO INHIB ALARM indicator illuminated 180±25 seconds after the voltage is present at J2-t
i. S9 in the "ALARM DISABLE" position and the PUSH TO INHIB ALARM, ALARM INHIBITED indicator momentarily depressed	PUSH TO INHIB ALARM indicator extinguished ALARM INHIBITED indicator illuminated G/N POWER MODES DISABLED indicator illuminated 220±30 sec after the PUSH TO INHIB ALARM, ALARM INHIBITED indicator is released
j. PUSH TO INHIB ALARM, ALARM INHIBITED indicator depressed, released, and then depressed and held	G/N POWER MODES DISABLED indicator extinguished and illuminated again 40±5 sec after the PUSH TO INHIB ALARM, ALARM INHIBITED indicator is depressed and held

EQUIPMENT CONDITION	REQUIREMENT
k. S9 in the "ALARM ENABLE" position and the PUSH TO INHIB ALARM, ALARM INHIBITED indicator momentarily depressed.	BLOCK I SERIES 100, indicator illuminated COOLANT SUPPLY FAIL indicator flashing
m. 28 vdc present at J2-e (+)	BLOCK I SERIES 100 indicator extinguished. COLD PLATE TEMP FAIL indicator flashing Alarm bell ringing, ALARM INHIBITED indicator extinguished, and the PUSH TO INHIB ALARM indicator illuminated 180±25 seconds after the voltage is present at J2-e
n. 28 vdc removed from J2-e (+) and 28 vdc present at J2-f (+)	Alarm bell ringing, ALARM INHIBITED indicator extinguished, and the PUSH TO INHIB ALARM indicator illuminated 180±25 seconds after the voltage is applied to J2-f.

3.1.29 Wheel Power Fail. With the MPL in the OIA On Mode and in the operating condition specified in 3.1.24 except 3.1.24.k, and 28 vac, 800 cps present at J3-h (Hi) and J3-i (Lo), the BLOCK I SERIES 100, and ALARM INHIBITED indicators illuminated, the additional requirements shall be as follows:

EQUIPMENT CONDITION	REQUIREMENT
a. 28 vdc present at J1-KK (+)	-28 VDC FAIL PUSH RESET indicator illuminated
b. Voltage at J3-h (Hi) and J3-i (Lo) decreased to 0 vac	WHEEL POWER FAIL PUSH TO RESET indicator extinguished above 16 vac and illuminated below 14 vac
c. No voltage present at J1-KK	WHEEL POWER FAIL PUSH TO RESET indicator still illuminated
d. WHEEL POWER FAIL PUSH indicator momentarily depressed	WHEEL POWER FAIL PUSH TO RESET indicator extinguished
e. Same EQUIPMENT CONDITION as in a., and 28 vdc present at J2-t	WHEEL POWER FAIL PUSH TO RESET and GIMBAL LOCK CAUTION indicators illuminated BLOCK I SERIES 100 indicator extinguished COLDPLATE TEMP FAIL indicator flashing
f. Ground applied to J2-EE	WHEEL POWER FAIL PUSH TO RESET indicator extinguished G/N TEST CONFIG indicator illuminated

4.3.17 G/N Voltage. With the MPL in the OIA On Mode, the inputs specified in 4.2.1.3 except 4.2.1.3.e and m applied, 28 vdc applied to pin J1-Z (+) and grd connected to pin J2-JJ (-), the BLOCK I SERIES 100, ISS TEST CONFIG, and ALARM INHIBITED indicators shall illuminate and the test shall be performed as follows:

a. With the voltage at pin J1-CC decreased, the G/N VOLTAGE PUSH RESET and G/N POWER MODES DISABLED indicators shall illuminate and the G/N VOLTAGE PUSH RESET, LOW indicator shall flash at 21.5±0.5 vdc. With S9 momentarily set to the "ALARM ENABLE" position, the bell shall ring, the ALARM INHIBITED indicator shall extinguish and the PUSH TO INHIB ALARM indicator shall illuminate while S9 is in the "ALARM ENABLE" position.

b. With the voltage at pin J1-CC set to 22.5±0.4 vdc and then the G/N VOLTAGE, PUSH RESET, LOW, HIGH indicator momentarily depressed, the G/N POWER MODES DISABLED, G/N VOLTAGE PUSH RESET, and LOW indicators shall extinguish.

c. With the voltage at pin J1-CC increased, the G/N VOLTAGE PUSH RESET and the G/N POWER MODES DISABLED indicators shall illuminate and the G/N VOLTAGE PUSH RESET, HIGH indicator shall flash at 35.5±0.5 vdc.

d. With the voltage at pin J1-CC set at 31.5±0.4 vdc and then the G/N VOLTAGE, PUSH RESET, LOW, HIGH indicator momentarily depressed, the G/N POWER MODES DISABLED, G/N VOLTAGE PUSH RESET, and HIGH indicators shall extinguish.

4.3.18 G/N Voltage Verification. With the MPL in the OIA On Mode, the inputs specified in 4.2.1.3 except 4.2.1.3.e and m applied, and grd connected to J1-JJ, the BLOCK I SERIES 100, and ALARM INHIBITED indicators shall illuminate and the test shall be performed as follows:

a. With 28 vdc applied to pin J1-AA, the G/N VOLTAGE PUSH RESET indicator shall illuminate, the G/N VOLTAGE PUSH RESET, HIGH indicator shall flash, the G/N POWER MODES DISABLED indicator shall illuminate, and the voltage measured between pins J1-i and J1-FF shall be 28±4 vdc.

b. With the input to pin J1-AA removed, 28 vdc applied to J1-BB and the G/N VOLTAGE PUSH RESET, LOW, HIGH indicator momentarily depressed, the G/N VOLTAGE PUSH RESET indicator shall illuminate, the G/N VOLTAGE PUSH RESET, LOW indicator shall flash, the G/N POWER MODES DISABLED indicator shall illuminate, and the voltage measured between pins J1-i and J1-FF shall be 28±4 vdc.

4.3.29 IMU Fail.. With the MPL in the ISS On Mode and the inputs specified in 4.2.1.3 except 4.2.1.3.e applied, the BLOCK I SERIES 100, ALARM INHIBITED, -28 VDC FAIL PUSH TO RESET, and WHEEL POWER FAIL PUSH TO RESET indicators shall illuminate and the test shall be performed as follows:

a. With 28 vdc applied to pin J3-q (+), the IMU FAIL indicator shall illuminate.

b. With the input to pin J3-q removed, a 102.4K pps input signal applied to pins J3-n (Hi) and J3-p (Lo) through a series resistance of 500±25 ohms and a shunt capacitance of 1600±320 mmfd (across pins J3-n and J3-p), and the input signal increased from 0 to 6V pp, the IMU FAIL indicator shall extinguish below 1.0V pp and illuminate above 2.0V pp.

4.3.30 Coolant Supply, Coldplate, and 40- and 180- Second Time Delays. With the MPL in the OIA and ISS On Modes and with the inputs specified in 4.2.1.3 except 4.2.1.3.e, k, and m applied, the test shall be performed as follows:

a. With the input specified in 4.2.1.3.k applied and 28 vdc applied to pin J1-S (+), the BLOCK I SERIES 100, and ALARM INHIBITED indicators shall illuminate and the COOLANT SUPPLY FAIL indicator shall flash.

b. With the input specified in 4.2.1.3.k and the input to pin J1-S removed, the BLOCK I SERIES 100, and ALARM INHIBITED indicators shall illuminate and the COOLANT SUPPLY FAIL indicator shall flash. With S9 momentarily set to the ALARM ENABLE position, the bell shall ring, the ALARM INHIBITED indicator shall extinguish, and the PUSH TO INHIB ALARM indicator shall illuminate.while S9 is in the "ALARM ENABLE" position.

c. With the input specified in 4.2.1.3.k applied and 28 vdc applied to pin J2-t (+), the ALARM INHIBITED and GIMBAL LOCK CAUTION indicator shall illuminate and the COLDPLATE TEMP FAIL indicator shall flash.

d. With the input specified in 4.2.1.3.k applied and 28 vdc applied to pins J2-t (+) and J2-a (+), the ALARM INHIBITED and GIMBAL LOCK CAUTION indicators shall illuminate.

e. With the input specified in 4.2.1.3.k applied and 28 vdc applied to pins J2-t (+) and J1-n (+), the ALARM INHIBITED and GIMBAL LOCK CAUTION indicators shall illuminate.

f. With the input specified in 4.2.1.3.k and the input to pins J1-n and J2-t removed, the input specified in 4.2.1.3.m applied, S9 set to the "ALARM ENABLE" position, and the PUSH TO INHIB ALARM, ALARM INHIBITED indicator momentarily depressed, the BLOCK I SERIES 100, ALARM INHIBITED, -28 VDC FAIL PUSH TO RESET, and WHEEL POWER FAIL PUSH TO RESET indicators shall illuminate, the COOLANT SUPPLY FAIL indicator shall flash, and the test shall be performed as follows:

(1) With 28 vdc applied to pin J2-t (+), the BLOCK I SERIES 100 indicator shall extinguish, the GIMBAL LOCK CAUTION indicator shall illuminate and the COLDPLATE TEMP FAIL indicator shall flash. The alarm shall ring, the ALARM INHIBITED indicator shall extinguish and the PUSH TO INHIB ALARM indicator shall illuminate 180±25 sec after the voltage is applied to pin J2-t.

(2) With S9 set to the "ALARM DISABLE" position and then the PUSH TO INHIB ALARM, ALARM INHIBITED indicator momentarily depressed, the PUSH TO INHIB ALARM indicator shall extinguish, the ALARM INHIBITED indicator shall illuminate and 220±30 sec after the PUSH TO INHIB ALARM, ALARM INHIBITED indicator is released, the G/N POWER MODES DISABLED indicator shall illuminate.

(3) With the PUSH TO INHIB ALARM, ALARM INHIBITED indicator depressed, released, and then depressed and held, the G/N POWER MODES DISABLED indicator shall extinguish and shall illuminate again 40±5 sec after the PUSH TO INHIB ALARM, ALARM INHIBITED indicator is depressed and held.

g. With S9 in the "ALARM ENABLE" position, the PUSH TO INHIB ALARM, ALARM INHIBITED INDICATOR momentarily depressed, the BLOCK I SERIES 100 and ALARM INHIBITED indicators illuminated, and the COOLANT SUPPLY FAIL lamp flashing, the test shall be as follows:

(1) With 28 vdc applied to pin J2-e (+) the BLOCK I SERIES 100 indicator shall extinguish, the GIMBAL LOCK CAUTION indicator shall illuminate, and the COLDPLATE TEMP FAIL indicator shall flash. The ALARM INHIBITED indicator shall extinguish, the alarm shall ring, and the PUSH TO INHIB ALARM indicator shall illuminate 180±25 seconds after the voltage is applied to pin J2-e.

(2) With 28 vdc removed from J2-e (+) and then applied to J2-f (+), the BLOCK I SERIES 100 indicator shall extinguish, the GIMBAL LOCK CAUTION indicator shall illuminate, and the COLDPLATE TEMP FAIL indicator shall flash. The ALARM INHIBITED indicator shall extinguish, the alarm shall ring, and the PUSH TO INHIB ALARM indicator shall illuminate 180±25 seconds after the voltage is applied to pin J2-f.

4.3.31 Wheel Power Fail. With the MPL in the OIA On and ISS On Modes, the inputs specified in 4.2.1.3 except 4.2.1.3.e and m applied, and 28 vac at 800 cps applied to pins J3-h (Hi) and J3-i (Lo), the BLOCK I SERIES 100, and ALARM INHIBITED indicators shall illuminate and the test shall be performed as follows:

a. With the input specified in 4.2.1.3.m applied the -28 VDC FAIL PUSH RESET indicator shall illuminate. Then with the voltage at pins J3-h (Hi) and J3-i (Lo) decreased to 0 vac, the WHEEL POWER FAIL PUSH RESET indicator shall extinguish above 16 vac and illuminate below 14 vac.

b. With the input in 4.2.1.3.m removed, the WHEEL POWER FAIL PUSH TO RESET indicator shall remain illuminated.

c. With the WHEEL POWER FAIL PUSH TO RESET indicator momentarily depressed, the WHEEL POWER FAIL PUSH TO RESET indicator shall extinguish.

d. With 28 vdc applied to pin J2-t and the input specified in 4.2.1.3.m, the WHEEL POWER FAIL PUSH TO RESET and the GIMBAL LOCK CAUTION indicators shall illuminate, the BLOCK I SERIES 100 indicator shall extinguish and the COLDPLATE TEMP FAIL indicator shall flash.

e. With grd applied to pin J2-EE the WHEEL PUSH TO RESET indicator shall extinguish and the G/N TEST CONFIG indicator shall illuminate.

4.3.32 Minus 28 vdc Fail. With the MPL in the OIA On and ISS On Modes, the inputs specified in 4.2.1.3 except 4.2.1.3.e and m applied, and 28 vdc from a separate isolated source applied to pins J2-d (+) and J2-c (-), the BLOCK I SERIES 100, ALARM INHIBITED indicators shall illuminate and the test shall be performed as follows:

a. With the input specified in 4.2.1.3.m applied the WHEEL POWER FAIL PUSH TO RESET indicator shall illuminate. Then with voltage at the pins J2-d and J2-c removed, the -28 VDC FAIL PUSH TO RESET lamp shall extinguish before the input is removed and illuminate after the input is removed.

b. With the input specified in 4.2.1.3.m removed, the -28 VDC FAIL PUSH TO RESET indicator shall remain illuminated.

c. With the -28 VDC FAIL PUSH TO RESET indicator momentarily depressed, the -28 VDC FAIL PUSH TO RESET indicator shall extinguish.

5. PREPARATION FOR DELIVERY

5.1 GENERAL. Preparation for delivery shall be in accordance with Specification ND1002214.

6. NOTES. None.

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PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

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Record of Revisions

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EQUIPMENT CONDITIONS	REQUIREMENT
a. Ground present at J3-Y	GIMBAL LOCK CAUTION indicator illuminated
b. Ground to J3-Y removed and 28 vdc present at J2-t	BLOCK I SERIES 100 indicator extinguished COLDPLATE TEMP FAIL indicator flashing
c. Voltage at J3-W (Hi) and J3-X (Lo) decreased	GIMBAL LOCK CAUTION indicator shall be extinguished above 14.5 vac and shall be illuminated below 10.5 vac

3.1.23 Star Presence. With the MPL in the operating condition specified in 3.1.14, except the conditions specified in 3.1.14.k and m. not present, the ISS TEST CONFIG indicator extinguished, the requirements shall be as follows:

EQUIPMENT CONDITION	REQUIREMENT
a. 28 vdc present at J3-JJ (+)	STAR PRESENCE indicator illuminated
b. No voltage present at J3-JJ, a 102.4K pps signal present at J3-NN (Hi) and J3-PP (Lo) through a series resistance of 500±25 ohms and a shunt capacitance of 1600±320 mmfd (across pins J3-NN and J3-PP); the 102.4K pps signal increased from 0 to 6V pp	STAR PRESENCE indicator shall be extinguished below 1.0V pp and shall be illuminated above 2.0V pp.

3.1.24 Error Detect and 5-sec Time Delay. With the MPL in the operating conditions listed below and ground present at J3-KK, 28 vdc shall appear between J3-N (+) and J3-P (-) 5.0±0.5 seconds after the presence of 28 vdc at J1-KK; and the BLOCK I SERIES 100, ERROR DETECT, ALARM INHIBITED, -28 VDC FAIL PUSH TO RESET, and WHEEL POWER FAIL PUSH TO RESET indicators shall illuminate.

a. 28 vdc present at pins J1-EE (+) and J1-FF (-).
b. 115 vac present at pins J1-GG (Hi) and J1-HH (Lo)
c. 27.5 vdc present at pins J1-CC (+) and J1-DD (-)
d. 115 vac present at pins J1-LL (Hi), J1-MM (Hi), J1-NN (Hi) and J1-PP (Lo)
e. 115 vac neutral connected to pin J1-p (Lo)
f. 28 vdc present at pin J1-g (+)
g. 115 vac present at pin J1-V (Hi)
h. 28 vdc present at pin J2-W (+)
i. 28 vdc momentarily present at pin J2-Z (+)
k. 28 vdc present at pin J1-KK (+)
m. MPL in the ISS On Mode
n. 28 vdc present at pin J1-c

3.1.25 ISS CDU Fail. With the MPL in the operating conditions specified in 3.1.24 and the BLOCK I SERIES 100, ALARM INHIBITED, -28 VDC FAIL PUSH TO RESET and WHEEL POWER FAIL PUSH TO RESET indicators illuminated, the requirements shall be as follows:

EQUIPMENT CONDITION	REQUIREMENT
a. 28 vdc present at J2-x (+)	ISS CDU FAIL indicator illuminated
b. No voltage present at J2-x (+) and a 102.4K pps signal present at J2-y (Hi) and J2-z (Lo) through a series resistance of 500±25 ohms and a shunt capacitance of 1600±320 mmfd (across J2-y and J2-z) and the 102.4K pps signal increased from 0 to 6V pp.	ISS CDU FAIL indicator shall be extinguished below 1.0V pp and shall be illuminated above 2.0V pp

3.1.26 Accel Fail. With the MPL in the in the operating conditions specified in 3.1.24 and the BLOCK I SERIES 100, ALARM INHIBITED, - 28 VDC FAIL PUSH TO RESET and WHEEL POWER FAIL PUSH TO RESET indicators illuminated, the following requirement shall exist. With 102.4K pps present at J2-u (Hi) and J2-v (Lo), through a series resistance of 500±25 ohms and a shunt capacitance of 1600±320 mmfd (across J2-u and J2-v) and the 102.4K pps signal increased from 0 to 6V pp, the ACCEL FAIL indicator shall be extinguished below 1.0V pp and shall be illuminated above 2.0V pp.

3.1.27 IMU Fail. With the MPL in operating conditions specified in 3.1.24, and the BLOCK I SERIES 100, ALARM INHIBITED, -28 VDC FAIL PUSH TO RESET, and WHEEL POWER FAIL PUSH TO RESET indicators illuminated, the requirements shall be as follows:

EQUIPMENT CONDITION	REQUIREMENT
a. 28 vdc present at J3-q (+)	IMU FAIL shall be illuminated
b. No voltage present at J3-q, 102.4K pps present at J3-n (Hi) and J3-p (Lo), through a series resistance of 500±25 ohms and a shunt capacitance of 1600±320 mmfd (across J3-n and J3-p) and the 102.4K pps signal increased from 0 to 6V pp	IMU FAIL shall be extinguished below 1.0V pp and shall be illuminated above 2.0V pp

3.1.28 Coolant Supply Coldplate, and 40- and 180- Second Time Delays. With the MPL in the OIA On Mode and in the operating conditions specified in 3.1.24, except the condition specified in 3.1.24.k and a shall not be present, the requirements shall be as follows:

EQUIPMENT CONDITION	REQUIREMENT
k. S9 in the "ALARM ENABLE" position and the PUSH TO INHIB ALARM, ALARM INHIBITED indicator momentarily depressed.	BLOCK I SERIES 100, indicator illuminated COOLANT SUPPLY FAIL indicator flashing
m. 28 vdc present at J2-e (+)	BLOCK I SERIES 100 indicator extinguished. COLD PLATE TEMP FAIL indicator flashing Alarm bell ringing, ALARM INHIBITED indicator extinguished, and the PUSH TO INHIB ALARM indicator illuminated 180±25 seconds after the voltage is present at J2-e
n. 28 vdc removed from J2-e (+) and 28 vdc present at J2-f (+)	Alarm bell ringing, ALARM INHIBITED indicator extinguished, and the PUSH TO INHIB ALARM indicator illuminated 180±25 seconds after the voltage is applied to J2-f.

3.1.29 **Wheel Power Fail.** With the MPL in the OIA On Mode and in the operating condition specified in 3.1.24 except 3.1.24.k, and 28 vac, 800 cps present at J3-h (Hi) and J3-i (Lo), the BLOCK I SERIES 100, and ALARM INHIBITED indicators illuminated, the additional requirements shall be as follows:

EQUIPMENT CONDITION	REQUIREMENT
a. 28 vdc present at J1-KK (+)	-28 VDC FAIL PUSH RESET indicator illuminated
b. Voltage at J3-h (Hi) and J3-i (Lo) decreased to 0 vac	WHEEL POWER FAIL PUSH TO RESET indicator shall be extinguished above 16 vac and shall be illuminated below 14 vac
c. No voltage present at J1-KK	WHEEL POWER FAIL PUSH TO RESET indicator still illuminated
d. WHEEL POWER FAIL PUSH indicator momentarily depressed	WHEEL POWER FAIL PUSH TO RESET indicator extinguished
e. Same EQUIPMENT CONDITION as in a., and 28 vdc present at J2-t	WHEEL POWER FAIL PUSH TO RESET and GIMBAL LOCK CAUTION indicators illuminated BLOCK I SERIES 100 indicator extinguished COLDPLATE TEMP FAIL indicator flashing
f. Ground applied to J2-EE	WHEEL POWER FAIL PUSH TO RESET indicator extinguished G/N TEST CONFIG indicator illuminated

b. With the grd to J3-Y removed and 28 vdc applied to J2-t, the BLOCK I SERIES 100 indicator shall extinguish, the ALARM INHIBITED indicator shall illuminate and the COLDPLATE TEMP FAIL indicator shall flash. With the voltage at pins J3-W (Hi) and J3-X (Lo) decreased, the GIMBAL LOCK CAUTION indicator shall be extinguished above 14.5 vac and shall be illuminated below 10.5 vac.

4.3.25 Star Presence. With the MPL in the OIA On Mode and the inputs specified in 4.2.1.3 except 4.2.1.3.e and m applied, the BLOCK I SERIES 100, and ALARM INHIBITED indicators shall illuminate and the test shall be performed as follows:

a. With 28 vdc applied to pin J3-JJ (+), the STAR PRESENCE indicator shall illuminate.

b. With the input to pin J3-JJ removed, a 102.4K pps input signal applied to pins J3-NN (Hi) and J3-PP (Lo) through a series resistance of 500±25 ohms and a shunt capacitance of 1600±320 mmfd (across pins J3-NN and J3-PP), and the input signal increased from 0 to 6V pp, the STAR PRESENCE indicator shall be extinguished below 1.0V pp and shall be illuminated above 2.0V pp.

4.3.26 Error Detect and 5-sec Time Delay. With the MPL in the ISS On Mode, the inputs specified in 4.2.1.3 except 4.2.1.3.e applied, and grd connected to J3-KK, 28±4 vdc shall appear between pins J3-N (+) and J3-P (-) 5.0±0.5 sec after the input specified in 4.2.1.3.m is applied and the BLOCK I SERIES 100, ERROR DETECT, ALARM INHIBITED, -28 VDC FAIL PUSH TO RESET and WHEEL POWER FAIL PUSH TO RESET indicators shall illuminate.

4.3.27 ISS CDU Fail. With the MPL in the ISS On Mode and the inputs specified in 4.2.1.3 except 4.2.1.3.e applied, the BLOCK I SERIES 100, ALARM INHIBITED, -28 VDC FAIL PUSH TO RESET and WHEEL POWER FAIL PUSH TO RESET indicators shall illuminate and the test shall be performed as follows:

a. With 28 vdc applied to pin J2-x (+), the ISS CDU FAIL indicator shall illuminate.

b. With the input to pin J2-x removed, a 102.4K pps input signal applied to J2-y (Hi) and J2-z (Lo) through a series resistance of 500±25 ohms and a shunt capacitance of 1600±320 mmfd (across J2-y and J2-z), and the input signal increased from 0 to 6V pp, the ISS CDU Fail indicator shall be extinguished below 1.0V pp and shall be illuminated above 2.0V pp.

4.3.28 Accel Fail. With the MPL in the ISS ON MODE, the inputs specified in 4.2.1.3 except 4.2.1.3.e applied, the BLOCK I SERIES 100, ALARM INHIBITED, -28 VDC FAIL PUSH TO RESET and WHEEL POWER FAIL PUSH TO RESET indicators shall illuminate and the test shall be performed as follows: With a 102.4K pps input signal applied to pins J2-u (Hi) and J2-v (Lo) through a series resistance of 500±25 ohms and a shunt capacitance of 1600±320 mmfd (across J2-u and J2-v), and the input signal increased from 0 to 6V pp, the ACCEL FAIL indicator shall be extinguished below 1.0V pp and shall be illuminated above 2.0V pp.

4.3.29 IMU Fail. With the MPL in the ISS On Mode and the inputs specified in 4.2.1.3 except 4.2.1.3.e applied, the BLOCK I SERIES 100, ALARM INHIBITED, -28 VDC FAIL PUSH TO RESET, and WHEEL POWER FAIL PUSH TO RESET indicators shall illuminate and the test shall be performed as follows:

a. With 28 vdc applied to pin J3-q (+), the IMU FAIL indicator shall illuminate.

b. With the input to pin J3-q removed, a 102.4K pps input signal applied to pins J3-n (Hi) and J3-p (Lo) through a series resistance of 500±25 ohms and a shunt capacitance of 1600±320 mmfd (across pins J3-n and J3-p), and the input signal increased from 0 to 6V pp, the IMU FAIL indicator shall be extinguished below 1.0V pp and shall be illuminated above 2.0V pp.

4.3.30 Coolant Supply, Coldplate, and 40- and 180- Second Time Delays. With the MPL in the OIA and ISS On Modes and with the inputs specified in 4.2.1.3 except 4.2.1.3.e, k, and m applied, the test shall be performed as follows:

a. With the input specified in 4.2.1.3.k applied and 28 vdc applied to pin J1-S (+), the BLOCK I SERIES 100, and ALARM INHIBITED indicators shall illuminate and the COOLANT SUPPLY FAIL indicator shall flash.

b. With the input specified in 4.2.1.3.k and the input to pin J1-S removed, the BLOCK I SERIES 100, and ALARM INHIBITED indicators shall illuminate and the COOLANT SUPPLY FAIL indicator shall flash. With S9 momentarily set to the ALARM ENABLE position, the bell shall ring, the ALARM INHIBITED indicator shall extinguish, and the PUSH TO INHIB ALARM indicator shall illuminate.while S9 is in the "ALARM ENABLE" position.

c. With the input specified in 4.2.1.3.k applied and 28 vdc applied to pin J2-t (+), the ALARM INHIBITED and GIMBAL LOCK CAUTION indicator shall illuminate and the COLDPLATE TEMP FAIL indicator shall flash.

d. With the input specified in 4.2.1.3.k applied and 28 vdc applied to pins J2-t (+) and J2-a (+), the ALARM INHIBITED and GIMBAL LOCK CAUTION indicators shall illuminate.

e. With the input specified in 4.2.1.3.k applied and 28 vdc applied to pins J2-t (+) and J1-n (+), the ALARM INHIBITED and GIMBAL LOCK CAUTION indicators shall illuminate.

f. With the input specified in 4.2.1.3.k and the input to pins J1-n and J2-t removed, the input specified in 4.2.1.3.m applied, S9 set to the "ALARM ENABLE" position, and the PUSH TO INHIB ALARM, ALARM INHIBITED indicator momentarily depressed, the BLOCK I SERIES 100, ALARM INHIBITED, -28 VDC FAIL PUSH TO RESET, and WHEEL POWER FAIL PUSH TO RESET indicators shall illuminate, the COOLANT SUPPLY FAIL indicator shall flash, and the test shall be performed as follows:

(1) With 28 vdc applied to pin J2-t (+), the BLOCK I SERIES 100 indicator shall extinguish, the GIMBAL LOCK CAUTION indicator shall illuminate and the COLDPLATE TEMP FAIL indicator shall flash. The alarm shall ring, the ALARM INHIBITED indicator shall extinguish and the PUSH TO INHIB ALARM indicator shall illuminate 180±25 sec after the voltage is applied to pin J2-t.

(2) With S9 set to the "ALARM DISABLE" position and then the PUSH TO INHIB ALARM, ALARM INHIBITED indicator momentarily depressed, the PUSH TO INHIB ALARM indicator shall extinguish, the ALARM INHIBITED indicator shall illuminate and 220±30 sec after the PUSH TO INHIB ALARM, ALARM INHIBITED indicator is released, the G/N POWER MODES DISABLED indicator shall illuminate.

(3) With the PUSH TO INHIB ALARM, ALARM INHIBITED indicator depressed, released, and then depressed and held, the G/N POWER MODES DISABLED indicator shall extinguish and shall illuminate again 40±5 sec after the PUSH TO INHIB ALARM, ALARM INHIBITED indicator is depressed and held.

g. With S9 in the "ALARM ENABLE" position, the PUSH TO INHIB ALARM, ALARM INHIBITED INDICATOR momentarily depressed, the BLOCK I SERIES 100 and ALARM INHIBITED indicators illuminated, and the COOLANT SUPPLY FAIL lamp flashing, the test shall be as follows:

(1) With 28 vdc applied to pin J2-e (+) the BLOCK I SERIES 100 indicator shall extinguish, the GIMBAL LOCK CAUTION indicator shall illuminate, and the COLDPLATE TEMP FAIL indicator shall flash. The ALARM INHIBITED indicator shall extinguish, the alarm shall ring, and the PUSH TO INHIB ALARM indicator shall illuminate 180±25 seconds after the voltage is applied to pin J2-e.

(2) With 28 vdc removed from J2-e (+) and then applied to J2-f (+), the BLOCK I SERIES 100 indicator shall extinguish, the GIMBAL LOCK CAUTION indicator shall illuminate, and the COLDPLATE TEMP FAIL indicator shall flash. The ALARM INHIBITED indicator shall extinguish, the alarm shall ring, and the PUSH TO INHIB ALARM indicator shall illuminate 180±25 seconds after the voltage is applied to pin J2-f.

4.3.31 Wheel Power Fail. With the MPL in the OIA On and ISS On Modes, the inputs specified in 4.2.1.3 except 4.2.1.3.e and m applied, and 28 vac at 800 cps applied to pins J3-h (Hi) and J3-i (Lo), the BLOCK I SERIES 100, and ALARM INHIBITED indicators shall illuminate and the test shall be performed as follows:

a. With the input specified in 4.2.1.3.m applied the -28 VDC FAIL PUSH RESET indicator shall illuminate. Then with the voltage at pins J3-h (Hi) and J3-i (Lo) decreased to 0 vac, the WHEEL POWER FAIL PUSH RESET indicator shall be extinguished above 16 vac and shall be illuminated below 14 vac.

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PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

BUFFER ASSEMBLY, ELECTRONIC

DRAWING NO. 2901405

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA
4 MAY 66	A		ALL INITIAL RELEASE	5-11-66	

This specification consists of page 1 to 5 inclusive.

APPROVALS	NASA/MSC	5-5-66 J. M. Watson 5-11-66 MIT/IL	ACSP

1. SCOPE

1.1 PURPOSE. This specification establishes the detail requirements for complete identification and acceptance of the Electronic Buffer Assembly, Part No. 2901405-011, hereafter referred to as the assembly.

2. APPLICABLE DOCUMENTS

2.1 EFFECTIVE ISSUES. The following documents form a part of this specification to the extent specified herein. Unless otherwise specified, Military Standards and Specifications shall be the issue in effect on the date of request for proposal or invitation to bid.

SPECIFICATIONS

APOLLO G&N

ND1002214	General Specification for Preservation, Packaging, Packing and Container Marking of APOLLO Guidance and Navigation Major Assemblies, Assemblies, Subassemblies, Parts and Associated Ground Support Equipment

DRAWINGS

APOLLO G&N

2901405	Buffer Assembly, Electronic

(Copies of specifications, standards, drawings, bulletins, and publications required by suppliers in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

2.2 CONFLICTING REQUIREMENTS. In event of a conflict between requirements, the following order of precedence shall apply. The contractor shall also notify MIT/IL APOLLO Management of the conflict.

a. The contract
b. This specification
c. Documents listed in this section

APOLLO G&N Specification
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PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

DISTRIBUTION BOX ASSEMBLY

DRAWING NO. 2900024

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA
4-MAY-66	A		ALL, INITIAL RELEASE	5-11-66	

This specification consists of page 1 to 16 inclusive.

APPROVALS	NASA/MSC	J. M. Watson 5-6-66 5-11-66 MIT/IL	ACSP

3. REQUIREMENTS

3.1 PERFORMANCE

3.1.1 Stepper Switch. A resistance of less than one ohm shall exist between the points specified in Table I for each of the stepper switch positions listed.

3.1.2 Amplifiers. Amplifier outputs shall be nominally 1 v/v and 5.6 v/v, as specified in Table II.

3.1.3 Relays, The voltage and resistance values shall be as specified in Table III for the listed relay operations.

3.1.4 Transformer. The transformer outputs shall be 5.5±0.5 vac and 65±5 vac with 115±10 vac, 400±20 cps applied to the transformer primary.

3.1.5 Dimmer Control Resistance. Dimmer control resistance shall be 9K ±90 ohms.

3.1.6 Temperature Indicator Operation. The temperature meter shall indicate a temperature deviation of 20 degrees at full scale.

3.1.7 Limit Cycle Load. With inputs of 4.90±0.05 and 0.430±0.005 and a 28±1 vac, 800±40 cps reference, the outputs shall be a 115±25 mvac, 800±40 cps signal read across a 15K ohm load that switches in phase (from 0° to 180°) at a rate of 200±10 times a second.

3.1.8 Ground Isolation. The resistance between chassis ground, shield ground and power ground shall be 100K ohms minimum.

3.1.9 Continuity. A resistance of less than 1.0 ohm shall exist between points on external connectors having common network numbers as defined on Drawing 2901473.

3.2 PRODUCT CONFIGURATION

3.2.1 Drawings. The configuration of the assembly shall be in accordance with Drawing 2900024 and all drawings and engineering data referenced thereon.

4.3.4 Stepper Switch. With the recommended test setup as shown in Figure 1, continuity with a resistance of less than 1 ohm shall exist between the pins specified in Table I.

4.3.5 Amplifiers. The amplifiers of the assembly shall be tested in accordance with the requirements specified in Table II.

4.3.6 Relays. The relays of the assembly shall be tested in accordance with the requirements specified in Table III. All test voltages shall be removed at the completion of Sections A, B, C, D, E, and F, respectively.

4.3.7 Transformer. With 115±10 vac, 400±20 cps applied to J27-L (Hi) and J27-N (Lo), the voltage measured at J33-q (Hi) and J33-r (Lo) shall be 65±5 vac and at J29-c (Hi) and J29-d (Lo) the voltage shall be 5.5±0.5 vac.

4.3.8 Dimmer Control Resistance. With R4 adjusted as necessary, the resistance from J19-53 to J19-54 shall be 9K±90 ohms. With R5 adjusted as necessary, the resistance from J29-n to J29-p shall be 9K±90 ohms. The resistance between J64-a and J34-D shall be 10K±2K ohms.

4.3.9 Temperature Indicator Operation. With 28±1 vdc applied to J1-Y (Hi) and J1-Z (Lo) and the temperature indicator switch set to the "20° CAL" position, the indicating meter shall read a nominal value of +20 degrees and the READ 20 DEGREE SCALE lamp shall illuminate. (Upon completion of this test, the temperature switch shall be returned to position "1".)

4.3.10 Limit Cycle Load. With the conditions specified below established, the output voltage between J16-19 (Hi) and J2-KK (Lo) shall be a 155±25 mv ac, 800±40 cps signal which switches phase (from 0° to 180°) at a rate of 200±10 times per second. Under these same conditions the output voltage between J16-22 (Hi) and J16-20 (Lo) shall be 4.9±0.1 vac.

a. A 15K ohm ±2 percent resistor connected between J16-19 (Hi) and J2-KK (Lo).

b. +28±1 vdc applied between J67-c (Hi) and J67-d (Lo) and between J16-M (Hi), E1 (Lo), and J66-Z (Lo).

c. 28±1 vac, 800±40 cps reference applied between J1-a (Hi) and J1-b (Lo).

d. 0.430±0.005 vac, 800±40 cps at 180° ±5° (with respect to the reference) applied between J2-JJ (Hi) and J2-KK (Lo).

e. 4.90±0.05 vac, 800±40 cps at 0° ±5° (with respect to the reference) applied between J2-MM (Hi) and J2-NN (Lo).

5. PREPARATION FOR DELIVERY

5.1 GENERAL. Preparation for delivery shall be in accordance with Specification ND1002214.

6. NOTES. None.

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PROCUREMENT SPECIFICATION
PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS
OPTICS INERTIAL TEST SET
DRAWING NO. 2900022

Record of Revisions

Date	Revision Letter	TDRR No.	Pages Revised	Approvals	
				MIT	NASA
[illegible]	A	32123	1-9 INITIAL RELEASE		

This specification consists of page 1 to 9 inclusive.

APPROVALS	NASA/MSC	J. M. Watson 10-14-66	MIT/IL	ACSP

1. SCOPE

1.1 PURPOSE. This specification establishes the detail requirements for complete identification and acceptance of all units of the Optics Inertial Test Set, Part No. 2900022-041.

2. APPLICABLE DOCUMENTS

2.1 Same as basic specification.

2.2 Same as basic specification.

3. REQUIREMENTS

3.1 Same as basic specification.

3.1.1 Same as basic specification.

3.1.2 and all its subparagraphs - Same as basic specification except added "LORS indicator shall be illuminated." to paragraph 3.1.2.7.

4. QUALITY ASSURANCE PROVISIONS

4.1 Same as basic specification.

4.1.1 Same as basic specification.

4.1.2 Same as basic specification.

4.2 Same as basic specification.

4.2.1 Same as basic specification.

4.2.2 through 4.2.2.3.3.r Same as basic specification.

4.2.2.3.3.s Same as basic specification with addition of:

(6) LORS J30-15 to J30-16 to J30-17 (OIA) [LORS indicator shall be illuminated when Pilot Power is on and when the system is not in the G&N and OSS configuration.]

4.2.2.3.3.t through 4.2.2.8.2 Same as basic specification.

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PROCUREMENT SPECIFICATION

CONTROLLER, TEMPERATURE, LIFTING

Record of Revisions

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				ccb ~~MIT~~	NASA
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This specification consists of page 1 to 5 inclusive.

APPROVALS	NASA/MSC	J. M. Watson 11-17-66	John E. Miller MIT/IL	ACSP

ADDENDUM NOTICE

This specification has been prepared as an addendum to:

Specification No. PS2900063
Revision —
Release Date 5·3·66

FOR

CONTROLLER, TEMPERATURE, LIFTING

Used With

The APOLLO G&N System

The exact content of Specification PS2900063 used as the basic document for this addendum is the revision referenced above plus the following specification change notices to Specification PS2900063.

1. SCOPE

1.1 PURPOSE. This specification establishes the detail requirements for complete identification and acceptance of the Controller, Temperature, Lifting, hereafter called the Controller, Part Number 2900063-021.

2. APPLICABLE DOCUMENTS

2.1 Same as basic specification.

2.2 Same as basic specification.

3. REQUIREMENTS

3.1 Same as basic specification.

3.1.1 Same as basic specification.

3.1.2 Same as basic specification.

3.1.3 Hot and Cold Alarm. The controller shall indicate, aurally and visually, "IMU-cold" and "IMU-hot" conditions as follows:

a. Cold Alarm: The IMU-cold lamp shall begin flashing, the alarm bell on the PTC shall begin ringing, and the flasher on the Battery Power Supply and Flasher shall begin flashing, when the indicating sensor resistance is increased to 2750±5 ohms.

b. Hot Alarm: The IMU hot lamp shall begin flashing, the alarm bell on the PTC shall begin ringing, and the flasher on the Battery Power Supply and Flasher shall begin flashing, when the indicating sensor resistance is decreased to 2210±5 ohms.

3.1.4 Same as basic specification.

3.2 Same as basic specification.

3.2.1 Same as basic specification.

4. QUALITY ASSURANCE PROVISIONS

4.1 Same as basic specification

4.2 Same as basic specification.

4.2.1 Same as basic specification.

4.2.1.1 Same as basic specification.

4.2.1.2 Same as basic specification

4.2.1.3 Same as basic specification.

4.2.1.4 Same as basic specification.

4.2.2 Same as basic specification.

4.3 Same as basic specification.

4.3.1 Same as basic specification.

4.3.2 Same as basic specification.

4.3.3 Same as basic specification.

4.3.4 Hot and Cold Alarm. The hot and cold alarm test shall be performed as follows:

a. Cold Alarm: With the indicating sensor resistance increased to 2750±5 ohms, the IMU-COLD lamp shall begin flashing, the alarm bell on the PTC shall begin ringing, and the flasher on the Battery Power Supply and Flasher shall begin flashing. With the ALARM INHIBITED (SYSTEM RESET) switch depressed, the alarm bell shall cease ringing and the IMU-COLD lamp and the flasher shall continue flashing. With the indicating sensor resistance decreased to 2500±5 ohms and the ALARM INHIBITED (SYSTEM RESET) switch again depressed, the IMU COLD lamp and the flasher shall cease flashing.

b. Hot Alarm: With the indicating sensor resistance decreased to 2210±5 ohms, the IMU-HOT lamp shall begin flashing, the alarm bell on the PTC shall begin ringing, and the flasher on the Battery Power Supply and Flasher shall begin flashing. With the ALARM INHIBITED (SYSTEM RESET) switch depressed, the alarm bell shall cease ringing and the IMU-HOT lamp and the flasher shall continue flashing. With the indicating sensor resistance increased to 2500±5 ohms and the ALARM INHIBITED (SYSTEM RESET) switch again depressed, the IMU-HOT lamp and the flasher shall cease flashing.

Figure 1 Same as basic specification.

4.3.5 Same as basic specification.

5. PREPARATION FOR DELIVERY

5.1 Same as basic specification.

6. NOTES

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Class A Release

PROCUREMENT SPECIFICATION

PRODUCT CONFIGURATION AND ACCEPTANCE TEST REQUIREMENTS

CONTROLLER, TEMPERATURE, PORTABLE

DRAWING NO. 2900060

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APPROVALS	NASA/MSC	J. M. Watson 11-17-66	John E Miller MIT/IL	ACSP

ADDENDUM NOTICE

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FOR

CONTROLLER, TEMPERATURE, PORTABLE

Used With

The APOLLO G&N System

The exact content of Specification PS2900060 used as the basic document for this addendum is the revision referenced above plus the following specification change notices to Specification PS2900060.

1. SCOPE

1.1 PURPOSE. This specification establishes the detail requirements for complete identification and acceptance of the Controller, Temperature, Portable, hereafter called the PTC, Part Number 2900060-021.

2. APPLICABLE DOCUMENTS

2.1 Same as basic specification.

2.2 Same as basic specification.

3. REQUIREMENTS

3.1 Same as basic specification.

3.1.1 Same as basic specification.

3.1.2 Same as basic specification.

TABLE I

TEMPERATURE METER CALIBRATION

DEPRESSED CALIBRATION SWITCH	TEMPERATURE METER INDICATION (°F)
120°	120.0±0.5
125°	125.00±0.25
130°	130.00±0.25
138°	138.0±0.5
140°	139.5±0.5

TABLE II

TEMPERATURE INDICATION

FROM	TO	RESISTANCE (ohms) ±0.1%	TEMPERATURE METER INDICATION (°F)
J4-C, J4-P J4-K and J4-T (all interconnected)	J4-G ↕ J4-G	2964	120.0±0.5
		2722.4	125.00±0.25
		2201.3	138.0±0.5
		2133.5	139.5±0.5

3.1.3 Same as basic specification.

3.1.3.1 Same as basic specification.

3.1.3.2 Hot. The hot temperature alarm operation shall be in accordance with the following requirements.

	EQUIPMENT CONDITION	OPERATION
a.	2230 to 2220 ohms present between J4-C, J4-P, J4-K and J4-T (all interconnected) and J4-G	Alarm bell ringing IMU HOT flashing Continuity between J3-A and J3-B
b.	2270 ohms maximum present between J4-C, J4-P, J4-K and J4-T (all interconnected) and J4-G	IMU HOT extinguished Continuity between J3-B and J3-C
c.	2254.1 ohms present between J4-C, J4-P, J4-K and J4-T, (all interconnected) and J4-G, momentarily turn power selector switch to OFF	No permanent temp alarm shall result

3.1.3.3 Same as basic specification.

3.1.4 Same as basic specification except change 3.1.4.f as follows:

"f. With an input of 25.2 vdc, the output shall be a minimum of 60 watts."

3.1.5 Same as basic specification except change 3.1.5.a as follows:

a.	115 vac present at J2-M and J2-J, PTC at one-half power output, 138° calibration switch depressed and held.	Output power shall drop to zero.

3.1.6 Same as basic specification.